DESIGN AND MODELING OF MB-OFDM UWB WITH DIGITAL DOWN CONVERTER AND DIGITAL UP CONVERTER FOR POWER LINE COMMUNICATION IN THE FREQUENCY BAND OF 50 MHZ TO 578 MHZ

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ABSTRACT

Over the last few years Power Line Communication has gained importance for high speed data communication. One of the major concerns in PLC is noise and high data rate, several schemes have been adopted to minimize noise over PLCs and improve data rate. One of the promising approach is the use of Multi Band (MB) – Orthogonal Frequency Division Multiplexing (OFDM) Ultra Wide Band (UWB) to achieve date rates over 200 Mbps. One of the approaches is to integrate MBOFDM UWB with Digital Down Converter (DDC) for power line communication. In this work, MBOFDM UWB system is integrated with DDC on the transmitter and DUC is integrated at the receiver to achieve higher data rate. The integrated system modeled using Matlab and Simulink achieves BER of 10^{-3} and THD of 1.2. Rate 2/3 Convolutional encoder, scrambler, bit interleave, GMSK modulator and IFFT have been used generate MBOFDM, time-frequency kernel with frequency translation achieves UWB. DDC consisting of CIC and CFIR are used to downlink the UWB signal as compatible with PLC.

Keywords: *MBOFDM, UWB, PLC, Integrated System, Down Converter, High Data Rate*

1. INTRODUCTION

Power line communication (PLC) is a promising technique for information transmission using existing power lines. PLC technologies can be used in an inside-building low voltage environment, a short-distance medium voltage environment, or a long-distance high voltage environment. Mixed high voltage, medium-voltage, and low-voltage power supply networks could be bridged to form very large networks for communications, as alternative telecommunication networks. In October 2004, the U.S. FCC adopted rules to facilitate the deployment of "Access BPL (Broadband over Power Line)", i.e., use of BPL to deliver broadband service to homes and businesses. Several competing organizations have developed specifications, including the HomePlug Powerline Alliance, Universal Powerline Association and HD-PLC Alliance. In October 2009, the ITU-T approved Recommendation G.hn/G.9960 as a standard for supporting high-speed home networking over power lines, phone lines and coaxial cables [1].

In January 2010, IEEE published its P1901 Draft Standard for Broadband over Power Line Networks: Medium Access Control and Physical Layer Specifications [2]**.** The great advantage of PLC is that the power lines exist in every home and every room. There are still lots of challenges for implementation in reality. Since the power line network has originally been designed for electricity distribution, rather than for data transfer, the power line as communication channel has various noise and disturbance characteristics, resulting in an unreliable channel. Improving the transmission rate over the power-line network has been studied extensively in recent times. Most of these studies are based on an operating frequency of less than 30 MHz [3] [4]. The HomePlug AV system developed by the HomePlug Powerline Alliance has employed adaptive orthogonal frequency-division multiplexing (OFDM) over a bandwidth of 26 MHz, ranging from 2 to 28 MHz, to achieve a physical layer data rate of up to 200 Mb/s [5]. However, meeting an ever increasing demand of higher data-transmission rates for applications, such as high-definition video streaming and Internet protocol television (IPTV), makes it insufficient. Ultra wideband (UWB) is gaining popularity in modern communication

technologies. It can provide very high data rates using a very wide frequency range of 500 MHz. It also offers a number of other advantages including low-interference to coexisting systems as well as robustness against multipath and simple implementation [6]. Strict radiation limits and availability of unlicensed spectrum worldwide have enhanced its usage for commercial as well as domestic applications [7] [8]. The wireless mode of this technology suffers from short transmission distances and signal attenuations while passing through the walls. The wired UWB can effectively overcome these drawbacks as well as the problem of limited transmission rates of the power lines. It is therefore, a viable approach for in-home power-line networks guaranteeing high data rates. Encouraging results on UWB pulse transmission have been obtained at frequencies below 100 MHz [9]. Impulse modulations and receiver algorithms for multiuser power-line communication (PLC) have been discussed by Tonello [10]. Chen *et al.* have studied the UWB communication over an indoor PLC channel covering a very wide frequency spectrum of 50 MHz–1 GHz [11]–[13]. These studies indicate that the power line provides a promising communication channel in the 50–578 MHz frequency range. It has been shown that this 528-MHz bandwidth can enable data transmission at rates of up to a gigabit per second even when the available signal power is very low [11] [12]. The physical-layer (PHY) data transmission has been simulated using the WiMedia multiband orthogonal frequency-division multiplexing (MB-OFDM) standard for the UWB wireless personal-area network (WPAN). It has resulted in the transmission data rate of up to 200 Mb/s. MB-OFDM speed is limited by FFT and IFFT, in order to improve the speed FFT can be replaced by NCO and DWT. Use of many other techniques such as NCO-OFDM and wavelet OFDM in multiband OFDM for power line communication has not been explored to its best. MB-OFDM signals uses eight different PHY data rates including 53.3, 80, 106.6, 160, 200, 320, 400, and 480 Mb/s. OFDM signal is transmitted in the RF range of 3168–3696 MHz (with a center frequency of 3432 MHz on channel). Indoor LV cables prefer a frequency range up to 578 MHz; therefore, it is necessary to convert the RF signal into a UWB power-line frequency range of 50–578 MHz. This has been achieved by designing the frequency down converter and the frequency up converter circuits. However, these down converters and up converters are external to the MB-OFDM and are to be integrated with MB-OFDM system. In this paper we analyze

performances of FFT, DWT and MB-OFDM. Further, for broad band communication, UWB-multiband OFDM is used, in this work, the performance analysis of UWB multiband OFDM for various modulation schemes are analyzed. A novel architecture for MB-OFDM for PLC is designed and developed that can be used over power line achieving higher data rate. Section II discusses OFDM architecture, section III discusses MB-OFDM architecture, section IV discusses software reference model design of MB-OFDM for power line communications and Section V is results and discussion and section VI is conclusion.

2. OFDM ARCHITECTURE

The OFDM transmitter section is illustrated in Figure 1. The MIMO-OFDM [14] section is grouped into two stages of data processing, the digital backend and digital front end. The digital backend module performs modulation such as QPSK or QAM, the output of modulator is space time encoded. In the digital front end module, the space time encoded data is transformed from frequency to time and is cyclic prefixed. The output of digital front end module is given to RF section for up conversion from IF to RF. The OFDM signal thus generated is then passed through a DAC before feeding it to the RF frontend section of the transmitter. It is then amplified to the required power levels to be transmitted. The transmitted signal is assumed to travel through a Gaussian noise channel, at the receiver the transmitted signal along with the noise is considered for demodulation.

At the receiver (Figure 2), the incoming signal is first processed using RF section and then is converted to digital signal using analog to digital converter. At the RF section of the receiver consists of a Low Noise Amplifiers (LNA), RF mixer and RF filter. The LNA amplifies the signal with minimum noise and thus improves SNR of the received signal. Analog-to-Digital converters, MIMO-OFDM receiver section, de-interleavers, decoder and the un-scrambler are the major building blocks at the receiver. The received OFDM signal is first passed through the low noise amplifier (LNA) and then to the Analog-to-digital section. The digital data is then fed to the MIMO-OFDM receiver section. The receiver section captures the incoming data and performs time to frequency conversion and the sub carriers obtained are demodulated using MIMO blocks that performs channel estimation and inverse space time coding. The modulated data is de-mapped, it is then de-

interleaved. The de-interleaved data is then passed through the Viterbi decoder and then to the un-scrambler to recover the system input.

The OFDM signal is first de-serialized and then fed to the cyclic prefix removal system. After the cyclic prefix is attenuated from the OFDM signal, it is fed to the FFT section which de-maps the data from each of the subcarriers. This is then fed to the demodulator to recover the original data. The limitation of MIMO-OFDM systems is the increases in complexity of the receiver module as higher modulation schemes are used. In order to overcome the limitations of FFT based OFDM model, in this chapter NCO based OFDM module is proposed.

3. ARCHITECTURE FOR A MULTIBAND OFDM SYSTEM

One approach to design a UWB system based on OFDM is to combine the modulation technique with a multibanding approach [15], which divides the spectrum into several sub-bands, whose bandwidth is approximately 500 MHz [16], [17]. The transmitted OFDM symbols are time-interleaved across the subbands. An advantage of this approach is that the average transmitted power is the same as a system designed to operate over the entire bandwidth. Other advantages of multibanding include processing the information over much smaller bandwidth (approximately 500 MHz), which reduces power consumption and lowers cost, improving spectral flexibility and worldwide compliance. An example of a multiband OFDM TX and RX [18], [19] is shown in Figure 3 and Figure 4. The TX and RX architectures for a multiband OFDM system are very similar to that of a conventional wireless OFDM system. The main difference is that the multiband OFDM system uses a time–frequency kernel to specify the center frequency for the transmission of each OFDM symbol. An example of how the OFDM symbols are transmitted in a multiband OFDM is shown in Figure 5.

Figure 5 shows one realization of a time–frequency code, where the first OFDM symbol is transmitted on sub-band 1, and the second OFDM symbol is transmitted on sub-band 3, the third OFDM symbol is transmitted on sub-band 2, and fourth OFDM symbol is transmitted on sub-band 1, and so on. In practice, the time–frequency code can be quite different and much longer in length. The time–frequency codes are used not only to provide frequency diversity in the system, but also to provide multiple accesses. From Figure 5, it is also apparent that a guard interval (9.5 ns) is appended to each OFDM symbol and that a CP is inserted before each OFDM symbol. The guard interval ensures that only a single RF transmit and RF RX chain are needed for all channel environments and all data rates and that there is sufficient time for the TX and RX to switch between the different center frequencies.

4. MBOFDM UWB FOR POWERLINE COMMUNICATIONS

MBOFDM UWB signals are very complex and hence generation of signals also leads to complexity. MBOFDM UWB generation has two parts, the first part generates MBOFDM UWB the second part down converts the generated signal to 50-578 MHz using discrete components of digital down converters. As the down converter is external to MBOFDM UWB flexibility in system adaptability is affected. The 128 subcarrier OFDM system covers a very wide frequency band while the power-line channel exhibits frequency-selective fading. It causes degradation of system performance. The existing MB-OFDM UWB system does not support adaptive modulation and power control. In this work an integrated system that integrates MBOFDM UWB with digital down converter is designed and modeled for PLCs. Figure 6 shows the proposed MBOFDM UWB system with digital down converter and up converter at the transmitter and receiver. The UWB signals generated with carrier frequencies fc = [3939 3978 4017 4056 3900 4094 7878 7956 8034 8112 7800 8190] MHz are down converted to frequencies f_{plc} = [53.3, 80, 106.6, 160, 200, 320, 400, 480, 528] MHz. It has been shown that this 528-MHz bandwidth can enable data transmission at rates of up to a gigabit per second even when the available signal power is very low [11], [12]. In this work, the MBOFDM UWB signals are down converted to 528 MHz using the direct digital synthesizer that generates the local oscillator signal to translate the centre frequency fc to f_{plc}. The input data is channel encoded, punctured, mapped using GMSK and modulated using IFFT to produce OFDM signal which is multiplied by time frequency kernel(fc) to generate UWB signal which is down converted using direct digital synthesizer (LO) to produce fplc for transmission over power line. On the receiver side, the digital up converter along with direct digital synthesizer is used to up convert the data to UWB and is demodulated using FFT, demodulation, depuncture and Viterbi decoder

to produce output data. The received data is used to compute Bit Error Rate (BER) to evaluate performance of MBOFDM UWB system. The UWB frequency of fc (3939 MHz) is converter to fplc (528 MHz) by using the LO (4467 MHz) by using the expressions $f_{plc} = f_c \times LO = f_c + LO \ and \ f_c - LO$ The lower side band fc-LO is filtered using the band pass filter and is transmitted over PLC. At the receiver the lower side band signal is up converted using LO generated using the DDS. Figure 6 Proposed MBOFDM UWB with digital down converter and up converter for PLCs The upper side band is filtered and is taken through the UWB system to obtain the output data. Next section discusses the design and modeling of proposed MBOFDM UWB system with Digital Down Converter (DDC) and D Digital Up Converter (DUC) for PLC.

5. DESIGN AND MODELLING OF MB OFDM UWB SYSTEM FOR PLC

The MB OFDM UWB system consists of a data Scrambler, Convolution Encoder, puncture, IFFT, GMSK Modulation, DAC, Channel, LPF, ADC, demodulation, Viterbi Decoder, Deinerleaver, and Descrambler. The DDC, DUC and DDS are interfaced to generate the UWB signals for PLC system.

5.1 Data Scrambler

Scrambler shall be employed to support cryptography. The stream of downlink packets shall be randomized by modulo-2 addition of the data with the output of the pseudo-random binary sequence (PRBS) generator as illustrated in Figure 7 to decrease the Hamming distance between two strings of bits. Scrambler is used to uniformly redistribute the zeros and ones bits over the data input. The scrambler scheme, recommended by the IEEE 802.15 standard is presented on Figure 7. For the pseudo random binary sequence (PRBS) generator is

$$g(D) = 1 + D_{14} + D_{15}$$

The initialization sequence,

$$x_{init} = \begin{bmatrix} x_{n-1}^i - x_{n-2}^i - x_{n-3}^i - x_{n-4}^i - x_{n-5}^i - x_{n-6}^i - x_{n-7}^i - x_{n-8}^i \\ -x_{n-9}^i - x_{n-10}^i - x_{n-11}^i - x_{n-12}^i - x_{n-13}^i - x_{n-14}^i - x_{n-15}^i \end{bmatrix}$$

where xin-k represents the binary initial value at the output of the kth delay element. The scrambled data bits vn, are obtained from unscrambled input bits sn, by XORing $v_0 = s_0 \oplus x_0$, where sn represents the unscrambled data bits. The side-stream de-scrambler at the receiver shall be initialized with the same initialization vector, xinit, used in the transmitter

scrambler. The initialization vector is determined from the seed identifier as given in Table 1.

Table 1: Scrambler Seed Selection

Seed Identifier	Seed Value
0,0	0011 1111 1111 111
0,1	0111 1111 1111 111
1,0	1011 1111 1111 111
1,1	1111 1111 1111 111

5.2 Forward Error Correction Coding And Interleaving

The convolutional encoder is one type of Linear Error Control Codes used to encode data so that errors introduced due to noise in the channel can be corrected by the decoder. Two important characteristics of a convolutional encoder are its rate and constraint length. If k data bits are shifted in for every n encoded bits shifted out, the rate of the code equals k/n. If the maximum degree of the generator polynomials are m, then the constraint length of the code equals k(m+1). Figure 9 (a) shows the convolutional encoder and figure 9 (b) shows the Viterbi decoder architecture for hard decision logic.

The encoder's constraint length is a vector of length 2 because the encoder has two inputs. The elements of this vector indicate the number of bits stored in each shift register, including the current input bits. Counting memory spaces in each shift register in the diagram and adding one for the current inputs leads to a constraint length of [5 4]. To determine the code generator parameter as a 2-by-3 matrix of octal numbers, use the element in the ith row and jth column to indicate how the ith input contributes to the jth output. For example, to compute the element in the second row and third column, the leftmost and two rightmost elements in the second shift register of the diagram feed into the sum that forms the third output. Capture this information as the binary number 1011, which is equivalent to the octal number 13. The full value of the code generator matrix is [23 35 0; 0 5 13]. Figure 10 shows the convolutional encoder and Viterbi Decoder output of first 20 bits.

5.3 Bit Interleaving

The coded and padded bit stream shall be interleaved prior to modulation to provide robustness against burst errors. The bit interleaving operation is performed in two stages, first symbol interleaving, to permit the bits across 6 consecutive MB OFDM symbols. Secondly, the intra-symbol tone interleaving, that permits the bits across the data subcarriers. Within an MB OFDM symbol,

exploits frequency diversity across subcarriers and provides robustness against narrow-band interferers.

5.4 IFFT

The MB OFDM symbols are generated by an IFFT operation with 128 points one advantage of IFFT is it saved the number of bank modulator. The idea behind IFFT is to generate orthogonally between MBOFDM symbols by multiplying different symbol with different frequency carrier, then sum those signals into one signal to transmit it to the channel. Figure 11 shows the OFDM using IFFT. Input symbols from mapper $[C_1, C_2, C_3 \ldots\ldots C_N]$ that consists of phase-frequency information are multiplied by orthogonal carriers of frequencies f_1 to f_N and are combined to form OFDM signal. At the receiver orthogonal carriers are used to extract symbols from the received OFDM signal. Sub-carriers modulation is performed after the IFFT process. In this work Gaussian Minimum Shift Key modulation is used, the advantage of GMSK over others modulation technique is that it has phase continuity. In MB approach, the spectrum is divided into 14 bands (each with a bandwidth equal to 528 MHz), and devices are allowed to statically or dynamically select which bands to use for transmission. The entire spectrum is divided into 4 distinct groups. Other groups have been reserved for future use. Figure 5 shows time-frequency coding for the MBOFDM system, where the first OFDM symbol is transmitted on sub-band 1, the second OFDM symbol is transmitted on sub-band 3, the third OFDM symbol is transmitted on sub-band 2, the fourth OFDM symbol is transmitted on sub-band 1, and so on [13].The Time Frequency Kernel to switch the center frequencies between three bands as shown in Figure 5. The receiver consists of LPF, ADC, Demodulation FFT, Deinterleaver, Viterbi decoder and descrambler. Figure 13 shows the MBOFDM UWB channel output and the filtered channel output at the receiver. And also shows the power spectral density of input signal, the input consists of DC component and hence the PSD is at its peak at zero frequency. Figure 14 shows Power spectral density of the input data which means the power of the signal before transmitting it. The observation shows that the spectrum lies from 0dB to -20 dB. Figure 14 The power spectral density of the output of the transmitter which is limited between-15db and-42 db as IEEE 802.15 standard to prevent interfere with others devices because UWB use unlicensed spectrum so that why it has less power compare to others devices by taking the PSD of the output.

The PSD of all harmonics is less than 15dB compared with the message signal. The normalized frequency is plotted against power spectral magnitude. The input signal is modulated using multiband OFDM technique and is transmitted to Noisy Channel. The received signal is demodulated and message is extracted. The output message demodulated and is compared with input PSD. From the comparison results shown it is found that the PSD resemble in both cases, thus ensuring the reconstruction capabilities of MIMO OFDM. Figure 15 shows the SNR vs BER performances of MBOFDM UWB. For SNR between -10 dB to 5 dB, BER is varying between $9e10^{-3}$ to $3e10^{-3}$ thus the BER remains constant for SNR 15dB variation.

5.5 Design of DDC and DUC For MBOFDM UWB

Power Line Communication or Power Line Carrier (PLC), also known as Power line Digital Subscriber Line (PDSL), mains communication, Power Line Telecom (PLT), Power Line Networking (PLN), or Broadband over Power Lines (BPL) are systems for carrying data on a conductor also used for electric power transmission. Electrical power is transmitted over high voltage transmission lines, distributed over medium voltage, and used inside buildings at lower voltages. Power line communications can be applied at each stage. Most PLC technologies limit themselves to one set of wires (for example, premises wiring), but some can cross between two levels (for example, both the distribution network and premises wiring). Typically the transformer prevents propagating the signal so multiple PLC technologies are bridged to form very large networks. The block diagram of the DUC core is shown in Figure 16. The baseband signal is translated to desired channel using the DDS and mixer comprising the multipliers. The sample rate is adjusted to match the channel bandwidth. This is performed by the multistage multi-rate filter consisting of cascaded integrator comb filter interpolator. The full precision output of one stage is carried forward for processing by next stage. This will generate more number of bits at the output. Hence the full precision results of one stage would be reduced before it is processed. This is done by using Bias-free convergent rounding. This will be inserted after each CIC filters and mixer.

The input to the DUC is an AF composite signal ranging in frequency from 50-578 MHz. The composite signal comprises of Speech, Data, Tele-protection and Pilot. The 8-bit sampled composite digitized input signal is fed to the series of two

stages CIC interpolation filters. A CIC filter up-samples the output by a factor of 8. The up-sampled signal is now given to the multiplier as the first input. Variable DDS is used to generate carrier frequencies in the range of 4460 – 5100 MHz is given as a second input to the multiplier. This multiplier output is the up-converted signal. This DUC output is given as an input for DDC. The block diagram of the DDC Core is shown in Figure 17. The desired channel is translated to baseband using the digital mixer comprising the multipliers and a direct digital synthesizer (DDS).

The sample rate of the signal is then adjusted to match the channel bandwidth. This is performed using a multi-stage multi-rate filter consisting of the cascaded integrator comb (CIC) filter decimator The full precision of a processing stage, i, may be carried forward for processing by stage i+1. Typically this would not be the case, and the full precision result of one stage would be reduced before it is processed by a subsequent stage. Bias-free convergent rounding is employed for this process. Figure 18 shows the MATLAB modeling of Digital Up Converter and the blocks are used to model. The output of sine wave block is taken as input for CIC interpolation filter. The block parameters of CIC interpolation are Interpolation factor of 8, Differential delay (M) of 1, number of sections of 3. The magnitude and phase response of CIC interpolation FIR filter is shown in Figure 18.

Compensation filter is a type of FIR filter used to compensate for loses in CIC filter in the typical interpolation filtering applications a reasonably flat pass band and narrow transition region filter performance is required. These desirable properties are not provided by the CIC filters alone, with their drooping pass band gains. The magnitude and phase response of CIC interpolation FIR filter is shown in Figure 20. The decimal values at the output of DDC in Simulink are taken. For these values, FFT (Fast Fourier Transformation) is calculated. X = [1529, 4012, 5859, 6784, 6688, 5573, 3598, 1050, -1688, -4171, -5988, -6912, -6816, -5701, -3726, -1179]. FFT is calculated in MATLAB by using

$$Y = FFT(X)$$

This is expressed in dB by

$$Z = 20 \times \log_{10}(abs(y))$$

and the plot of Z is showing in Figure 21.

SNR is calculated by using

$$SNR_{dB} = A_{signal,dB} - A_{noise,dB}$$ From figure 5-15,

$$SNR = V_2 - V_1 = (250 - 125)dB = 125dB$$

From Figure 21, THD is calculated by

$$THD = \sqrt{(V_1^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2) \div V_2} = 1.281$$

From the THD value it is found that the harmonic component is not very dominant in the UWB system over PLC. The major challenges are the down conversion of 3939 MHz centre frequency to 528 MHz component as per PLC requirement. The down conversion leads to harmonics and sub components that need to be filtered using suitable filters that introduce minimum harmonics. On the other hand at the receiver side, the digital up converter need to up convert the signal from 528 MHz to 3939 MHz, which again introduces harmonics and sub components. The challenges in down conversion and up conversion are addressed in this paper by optimum design of CIC filters and PFIR filters. The frequency band for PLC between 50 MHz to 578 MHz need to be reconfigurable, hence there is need for reconfigurable DDC which need to be designed as LO module.

6. CONCLUSION

In this paper, MBOFDM UWB system is integrated with digital down converter at the transmitter and digital up converter at the receiver to design an integrated system that can be used to transmit data over power line. The designed system supports data rate in the range of 50Mbps to 500Mbps, the input data is translated to UWB frequency in the range between 3939 MHz to 8190 MHz and is further down converted to the range 50 MHz to 578 MHz for power line requirement. The system is modeled using Matlab and Simulink, the interfaced system is simulated for various test cases of input data. BER performance is estimated and is found to be 10^{-3}. The digital up converter and down converter are designed using CIC and PFIR filters to minimize harmonic distortion, THD is found to be of 1.2. The design is suitable for power line communication; FPGA implementation of the proposed system would provide detailed information on hardware complexities and feasibility for real time applications.

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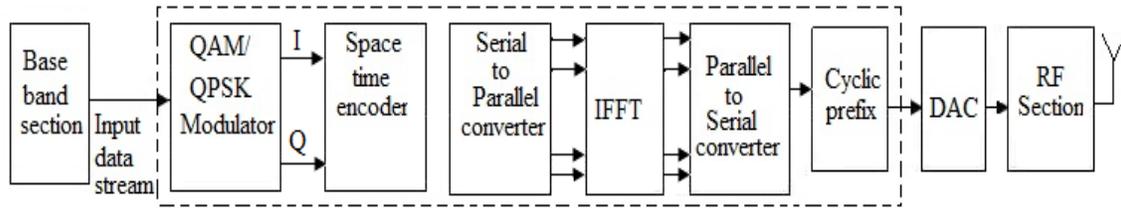
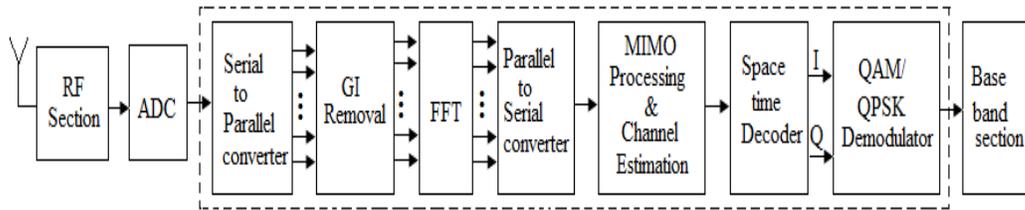\

Figure 1: OFDM Transmitter Using IFFT

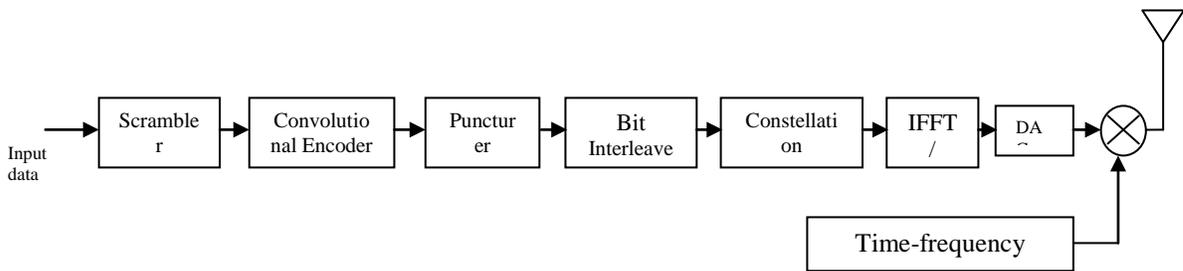*Figure 2: OFDM Receiver Using FFT*

Figure 3: Example TX Architecture for a Multiband OFDM System
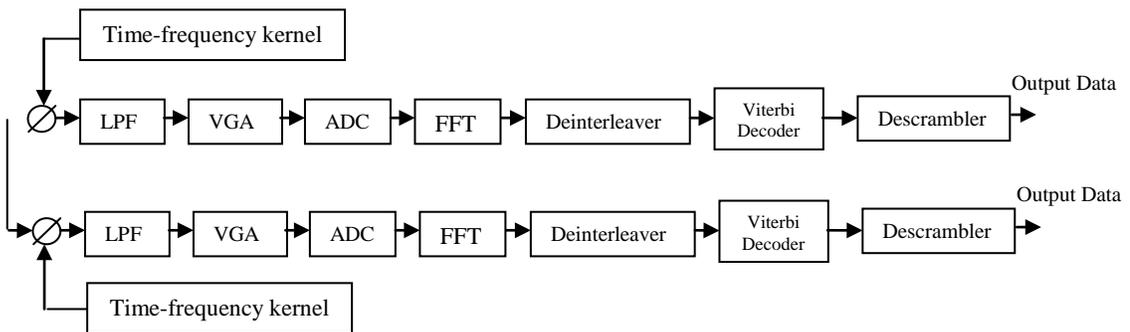

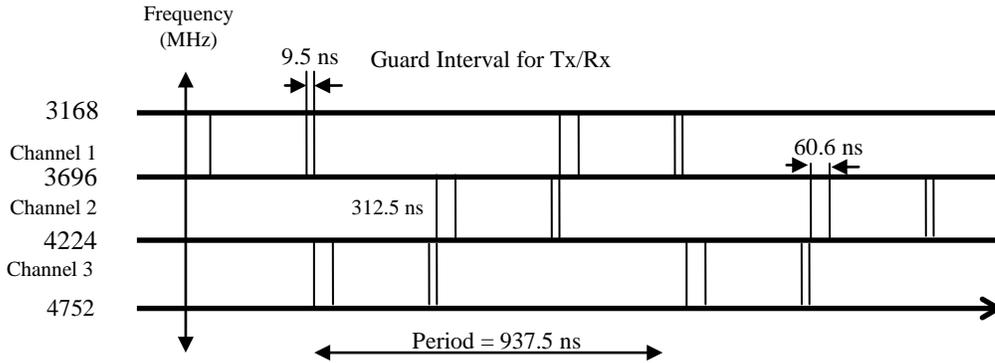*Figure 4: Example RX Architecture for a Multiband OFDM System*

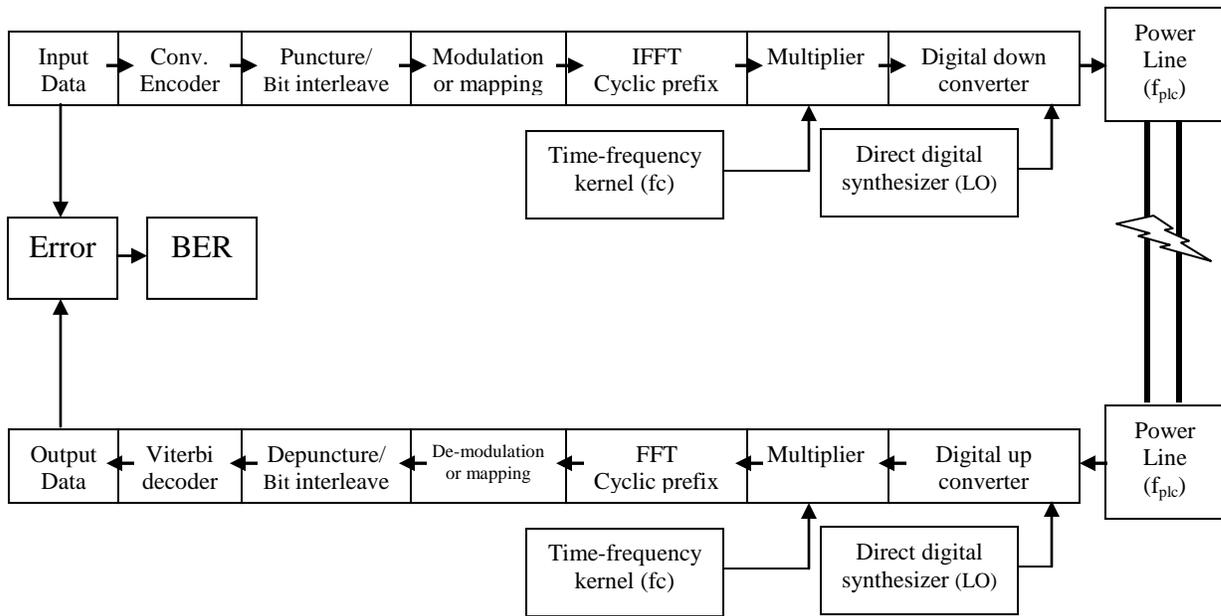*Figure 5: Example of Time-Frequency Coding For the Multiband OFDM System*

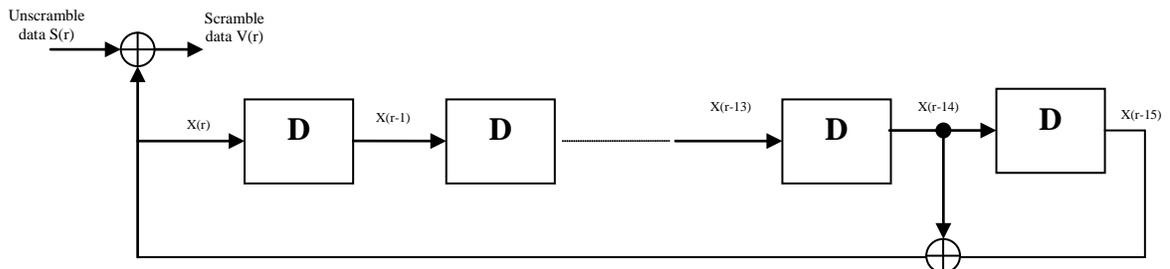*Figure 6: Proposed MBOFDM UWB with digital down converter and up converter for PLCs*

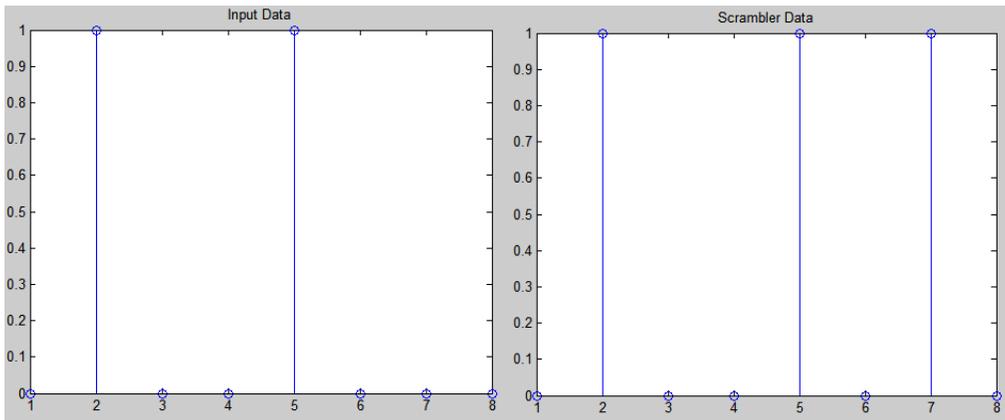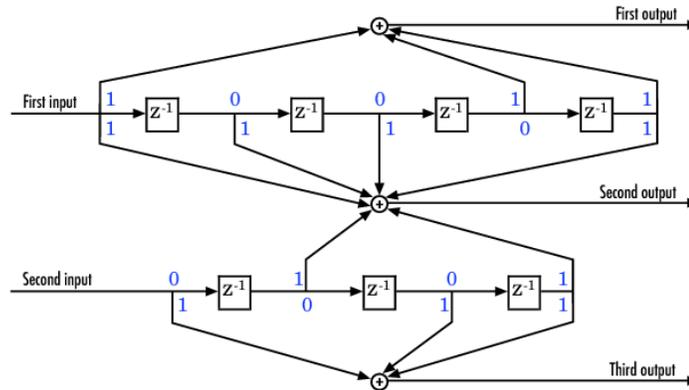*Figure 7: Realization of the Randomizer Linear Feedback Shift Registers [9]*

Figure 8: Input Data and Scrambled Output Data

Figure 9 (a) Convolution Encoder with a Rate 3/2
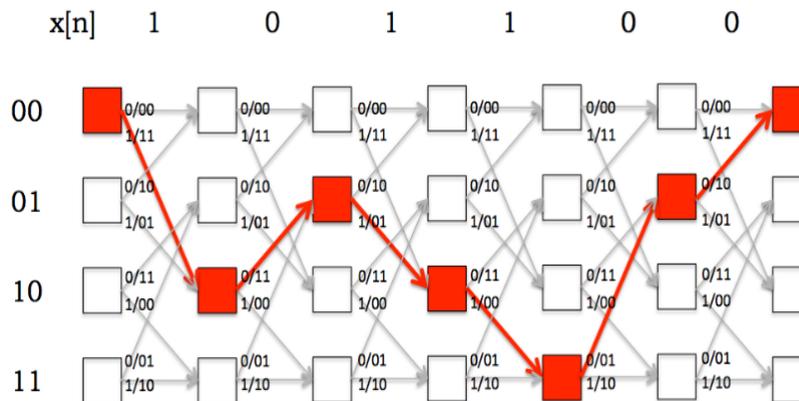
Figure 9 (b) Hard Decision Viterbi Decoder [20]
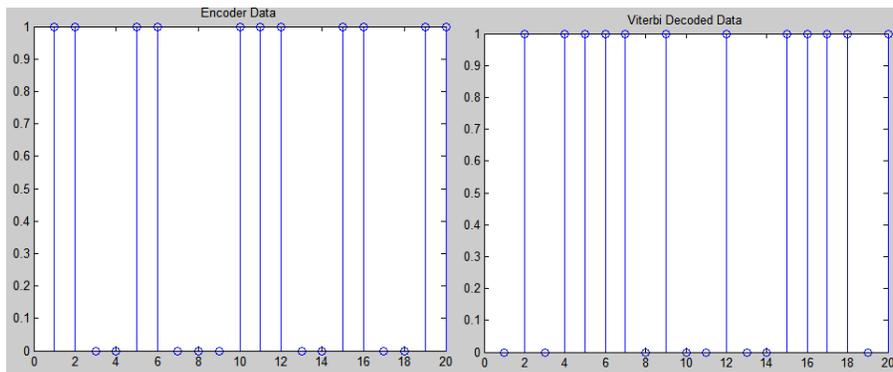
Figure 10: Convolution Encoder and Viterbi Decoder Output
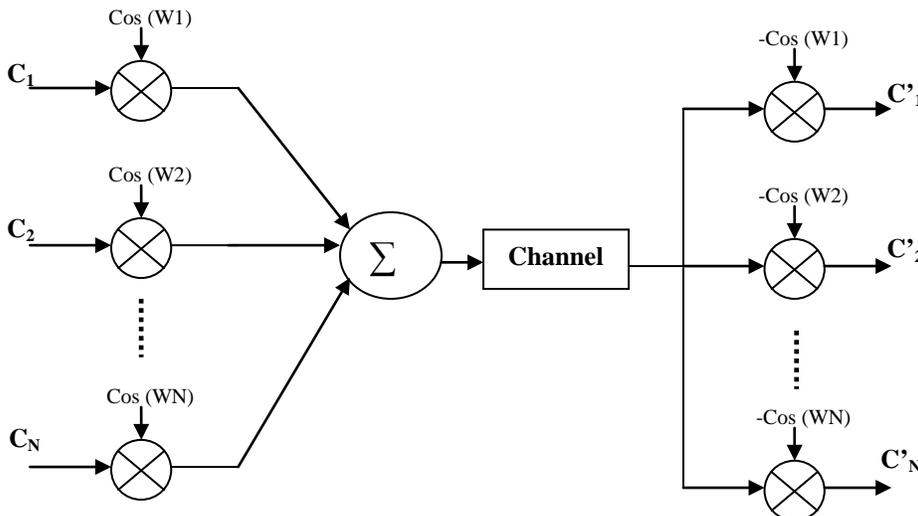
Figure 11: Multi Carrier Modulation Using IFFT
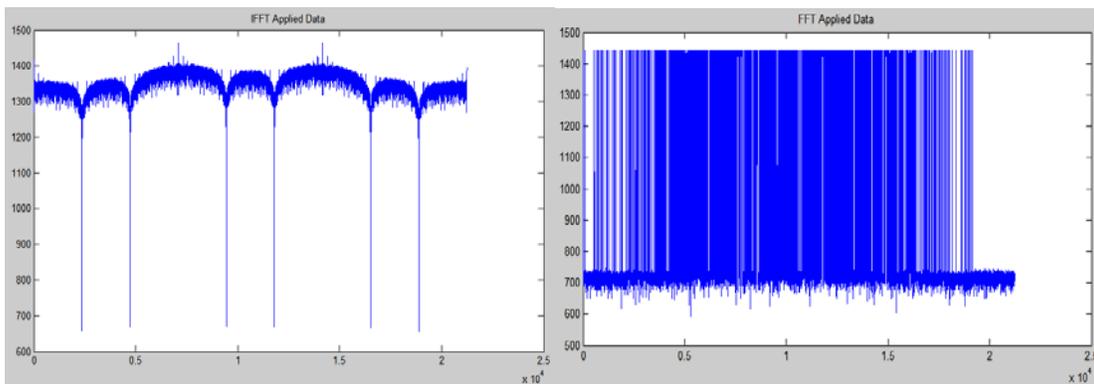
Figure 12: IFFT and FFT Output
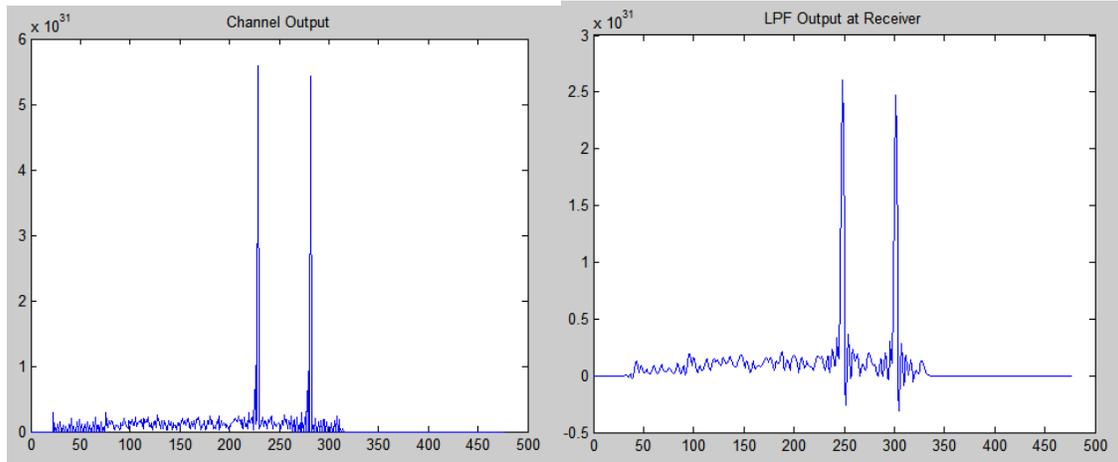
Figure 13: Channel Output and LPF Output at the Receiver
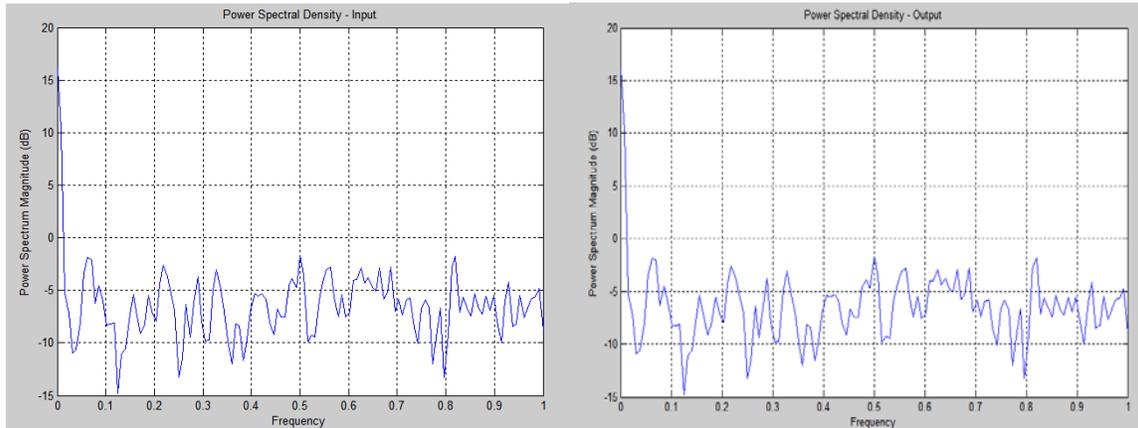
Figure 14: Power Spectral Density Of Input And Output Data
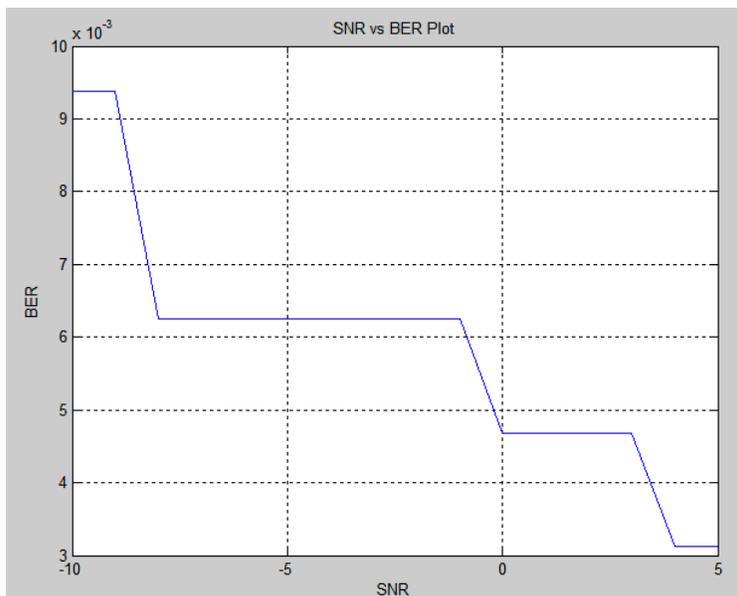
Figure 15: BER Vs SNR for MBOFDM UWB
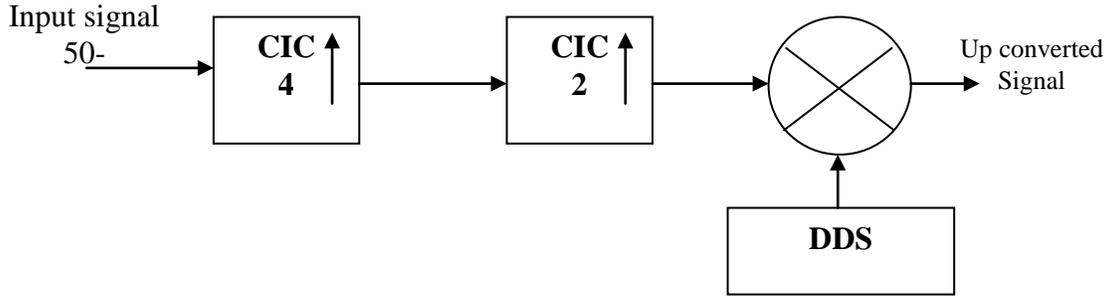
Figure 16: DUC Block Diagram [21]
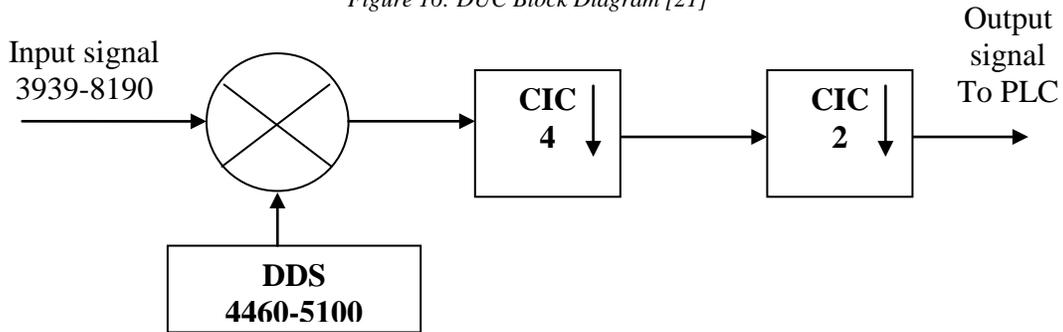
Figure 17: DDC Block Diagram [21]
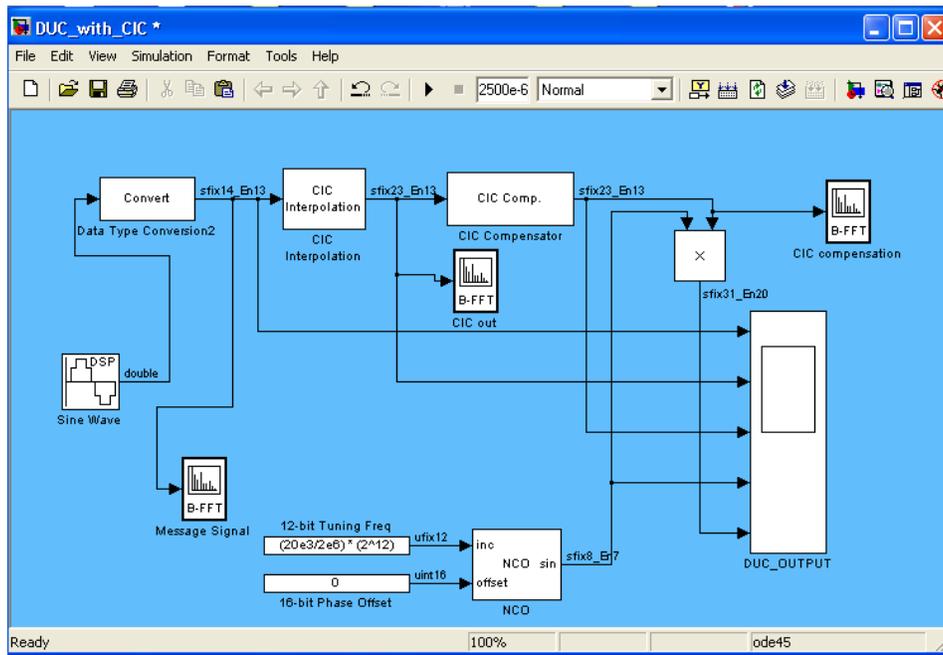
Figure 18: MATLAB Modeling Of DUC
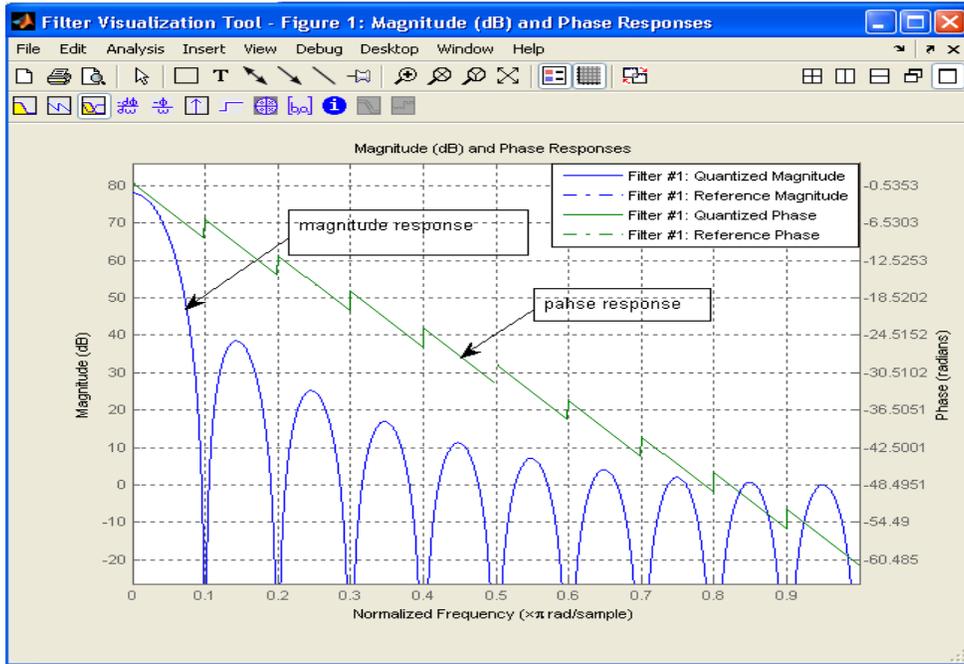
Figure 19: Magnitude And Phase Response Of CIC Interpolation Filter
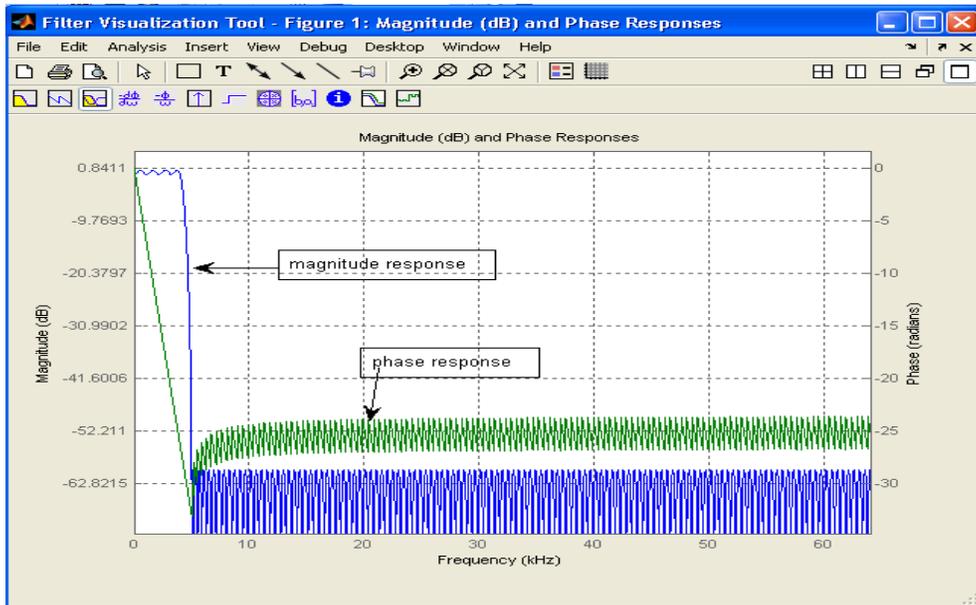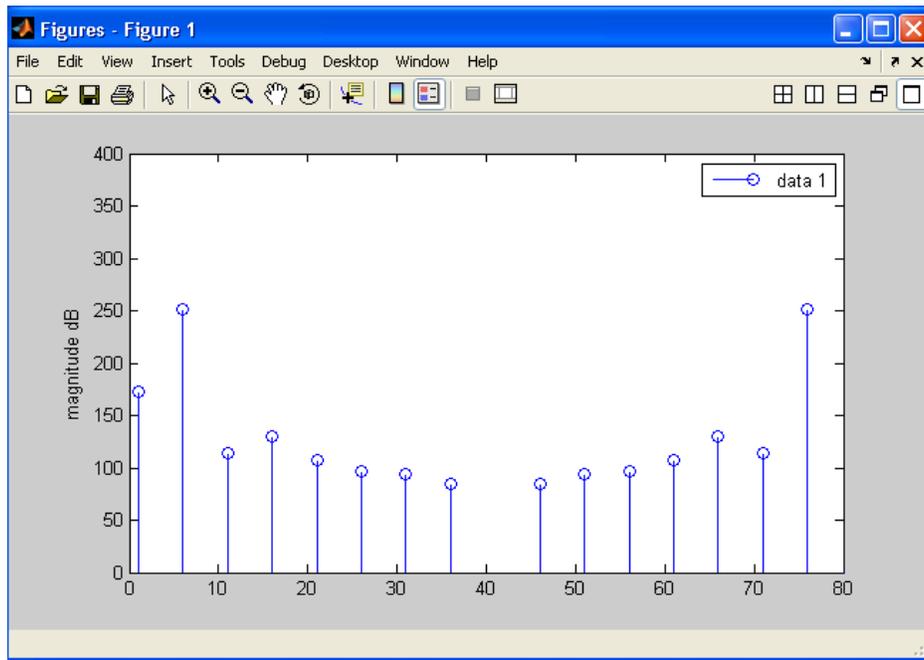

Figure 20: Magnitude and Phase Response of CIC Compensation Filter

Figure 21: FFT Spectrum of PLC Output