Journal of Theoretical and Applied Information Technology
30th September 2013. Vol. 55 No.3

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

EMBEDDED CONTROLLED FIVE LEVEL INVERTER BASED DYNAMIC VOLTAGE RESTORER

[1]S.LEELA, [2]S.S.DASH

[1] Assistant Professor, Dept.of Electrical & Electronics Engineering, Sastra University, Tamilnadu, India.

[2] Professor, Department of Electrical & Electronics Engineering, SRM University, Tamilnadu, India.

E-mail: [1]ss.leela@yahoo.com , [2]munu_dash_2K@yahoo.com

ABSTRACT

This paper deals with the simulation and implementation of five level inverter based Dynamic Voltage Restorer(DVR). The control of DVR that injects a voltage in series with a distribution feeder is presented. DVR is a power electronic controller that can protect sensitive loads from disturbances in supply system. DVR can regulate the voltage at the load. The simulation results of five level inverter based DVR are presented. The spectrum for the output voltage is also presented. Laboratory model is developed and the experimental results are compared with the simulation studies.

Keywords: *Dynamic Voltage Restorer(DVR), Matlab simulink, Series Compensation, Five level inverter.*

1. INTRODUCTION

The Figure 1 shows the series connection of a dynamic voltage restorer (DVR) between the utility source and loads, through a coupling transformer. During normal operating conditions, the DVR can be switched offline [1] or controlled to compensate for any injected harmonic voltages in the utility grid [2]. Upon the occurrence of a voltage sag (decrease in v_{PCC}), the DVR is commanded to inject a voltage v_o such that the magnitude of v_L ($=v_{PCC} + v_o$) remains essentially constant throughout the sag period. However, the phase of v_L can either be shifted or remain unchanged, depending on the compensation techniques adopted.

Conventionally, the series voltage v_o is injected through a coupling transformer, whose main functions are to provide voltage boosting ($v_o/v_o' > 1$) and electrical isolation between the phases. Usage of a transformer, however, has the disadvantage of making the DVR bulky and costly, the other disadvantages, as summarized in [1]. To overcome these disadvantages, [1] has proposed the series/parallel connection of semiconductor switches, or H-bridges, to develop high voltage DVR (HVDVR), which can be connected directly to the utility grid without a coupling transformer.

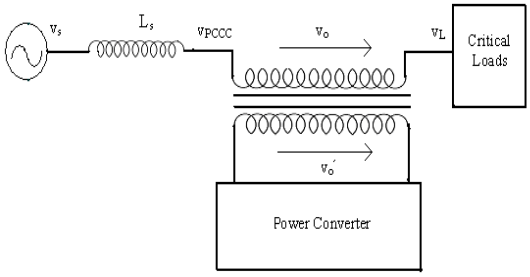


Figure 1 : System Configuration With Dynamic Voltage Restoration

This paper begins by analyzing different topological possibilities for implementing the HVDVR with the main aim of designing a reliable custom power conditioner. The next letter next presents an open-loop control scheme with Posicast compensator[3] incorporated for damping transient voltage oscillations at the instant of voltage injection (an issue which has not been actively investigated for DVR). The Posicast-based open-loop control is subsequently improved by adding a parallel multifeedback-loop control path to give two-degrees-of-freedom in control tuning. This feedback path uses the P+resonant compensator [4] to force the steady-state voltage error to zero, hence, enhancing the DVR load voltage regulation performance. Active harmonic elimination techniques are described [5]. All principles presented have been verified in

Journal of Theoretical and Applied Information Technology
30th September 2013. Vol. 55 No.3

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

Matlab/Simulink simulation using a cascaded five-level and a binary seven- level inverter.

2. CASCADED H-BRIDGE MULTI-LEVEL BOOST INVERTER WITH OUT INDUCTORS

The five level inverter is shown in Figure 2. To see how the system works, a simplified single phase topology is shown in Figure 3. The output voltage v_1 of this leg of the bottom inverter (with respect to the ground) is either $+V_{dc}/2$ (S_5 closed) or $-V_{dc}/2$ (S_6 closed). This leg is connected in series with a full H-bridge, which, in turn, is supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S_1 and S_4 closed), 0 (S_1 and S_2 closed or S_3 and S_4 closed), or $-V_{dc}/2$ (S_2 and S_3 closed). An example output waveform from this topology is shown in Fig.4a. When the output voltage $v = v_1 + v_2$ is required to be zero, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ or $v_1 = -V_{dc}/2$ and $v_2 = +V_{dc}/2$.

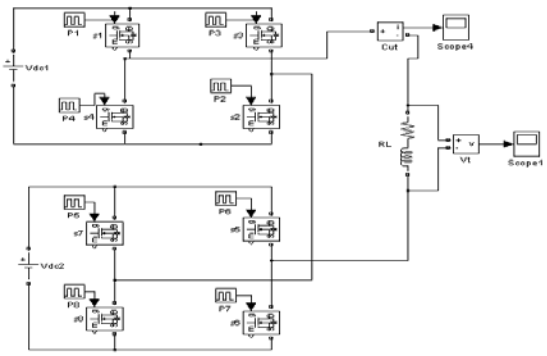


Figure 2 : Five Level Inverter

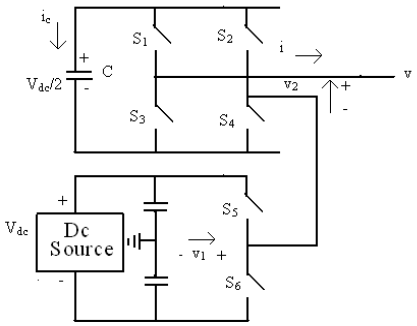
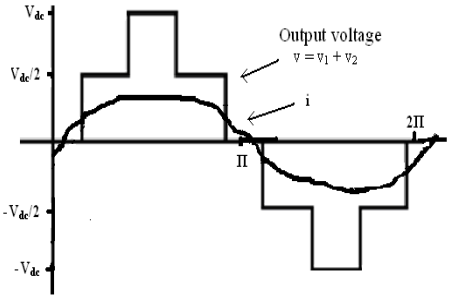
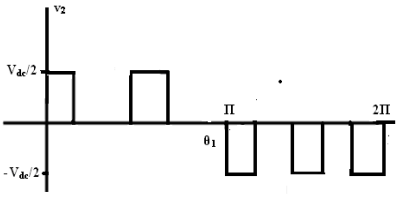


Figure 3 : Single Phase Of The Proposed Dc-Ac Cascaded H-Bridge Multilevel Boost Inverter

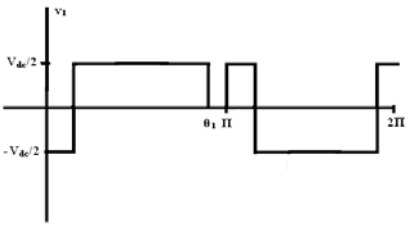
Additional capacitor's voltage regulation control detail is shown in Figure 4. To explain how the capacitor is kept charged, consider the interval $\theta_1 \leq \theta \leq \Pi$, the output voltage in Figure 4a is zero, and the current $i > 0$. If S_1 and S_4 are closed (so that $v_2 = +V_{dc}/2$) and S_6 is closed (so that $v_1 = -V_{dc}/2$), then the capacitor is discharging [$i_c = -i < 0$; see Figure 4b], and $v = v_1 + v_2 = 0$. On the other hand, if S_2 and S_3 are closed (so that $v_2 = -V_{dc}/2$) and S_5 is also closed (so that $v_1 = +V_{dc}/2$), then



a : Overall Output Voltage And Load Current.



b : Output Of Inverter 1



c : Output Of Inverter 2

Figure 4 : Capacitor Voltage Regulation With Capacitor Charging And Discharging

the capacitor is charging [$i_c = i > 0$; see Figure 4c], and $v = v_1 + v_2 = 0$. The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charging and discharging of the capacitor. Consequently, the method consists of monitoring the output current

Journal of Theoretical and Applied Information Technology
30th September 2013. Vol. 55 No.3

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

and the capacitor voltage, so that during periods of zero voltage output, either the switches S_1, S_4 and S_6 are closed or the switches S_2, S_3 and S_5 are closed, depending on whether it is necessary to charge or discharge the capacitor. It is this flexibility in choosing how to make the output voltage zero is exploited to regulate the capacitor voltage.

The goal of using fundamental frequency switching modulation control is to output a five-level voltage waveform, with a sinusoidal load current waveform, as shown in Figure 4a. If the capacitor's voltage is higher than $V_{dc}/2$, switches S_5 and S_6 are used to control the output voltage waveform, v_1, and the switches S_1, S_2, S_3 and S_4 are used to control the output voltage waveform v_2, shown in Figure 4b. The highlighted part of the waveform in Figure 4b is the capacitor discharging period, during which the inverter's output voltage is 0 V.

If the capacitor's voltage is lower than $V_{dc}/2$, the switches S_5 and S_6 are controlled to obtain output voltage waveform v_1, and switches S_1, S_2, S_3 and S_4 are controlled to obtain output voltage waveform v_2. Therefore, the capacitors' voltage can be regulated by alternating the capacitor's charging and discharging control, when the inverter output is 0 V.

This method of regulating the capacitor voltage depends on the voltage and current not being in phase. That is, one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current. In other words, the highest output Ac voltage of the inverter depends on the displacement power factor of the load. The above literature does not deal with five level inverter based DVR. This paper presents the concept of five level inverter based DVR.

3. SIMULATION RESULTS

Digital simulation is done using the blocks of Matlab simulink and the results are presented here. Five level inverter system with RL load is shown in Figure 5a. The five level inverter output voltage is shown in Figure 5b.The five level inverter output current is shown in Figure 5c. DVR using five level inverter is shown in Figure 6a. The voltage across external, load-1 and load-2 are shown in Figure 6b. FFT analysis for the output voltage is shown in Figure 6c. The THD value is 3.65%.

DVR system with LC filter is shown in Figure 7a. The voltage across external, load-1 and load-2 are shown in Figure 7b. FFT analysis for the output voltage is shown in Figure 7c. The THD reduces to 0.72%. Thus the harmonics are reduced from 3.65% to 0.72%.

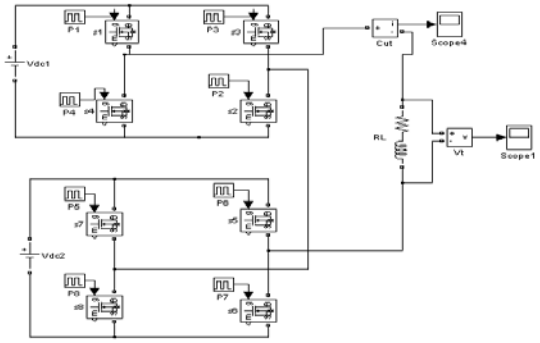


Figure 5a : Five Level Inverter With RL Load

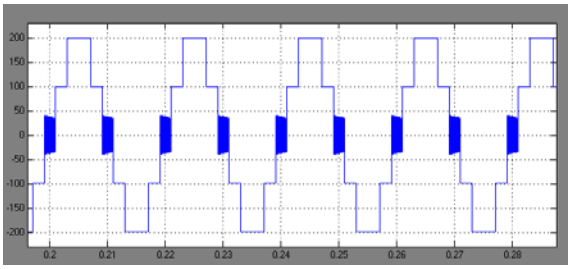


Figure 5b : Output Voltage Of Five Level Inverter

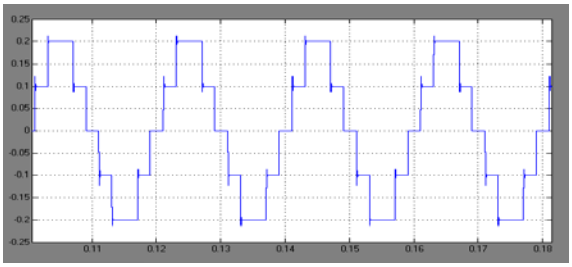


Figure 5c : Output Current Of Five Level Inverter

Journal of Theoretical and Applied Information Technology
30th September 2013. Vol. 55 No.3

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

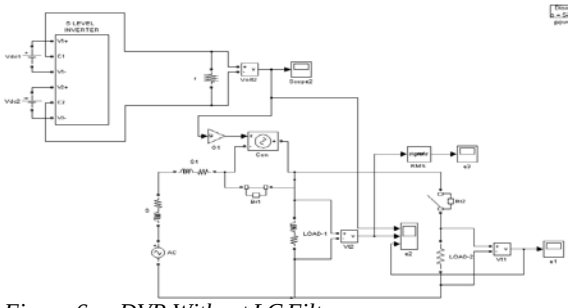


Figure 6a : DVR Without LC Filter

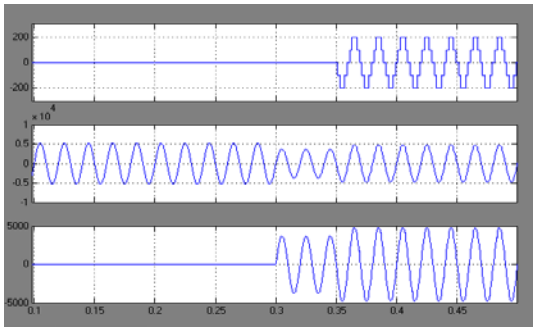


Figure 6b : Voltage Across External, Load-1 And Load-2

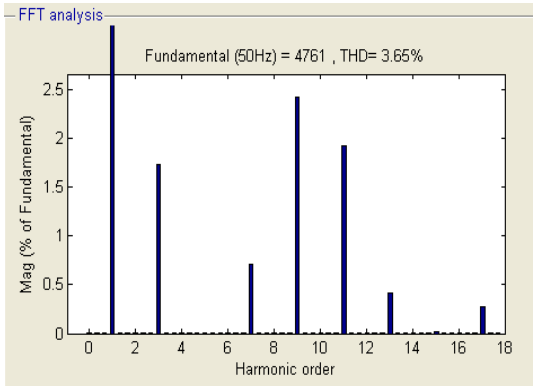


Figure 6c : FFT Analysis For Voltage

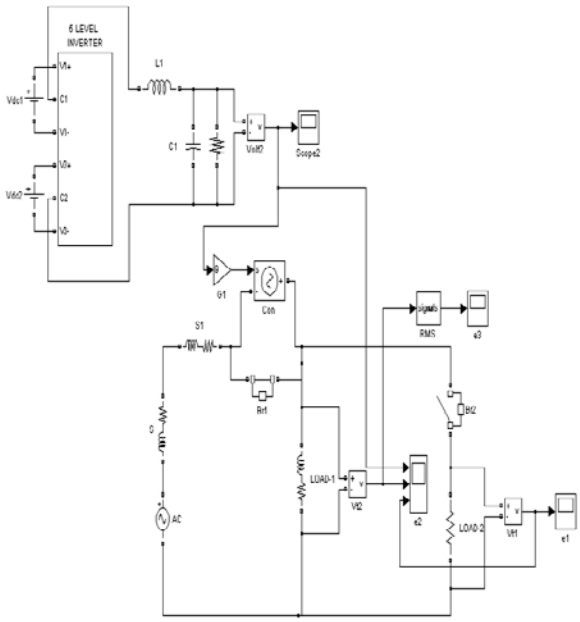


Figure 7a : DVR With LC Filter

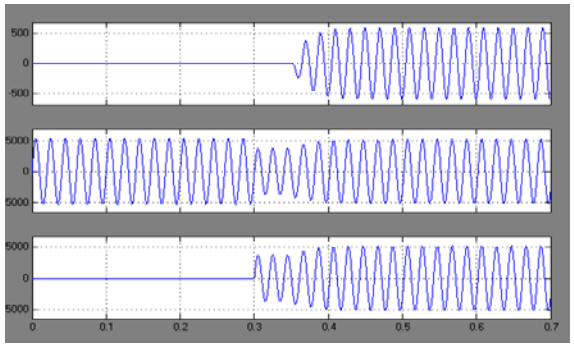


Figure 7b : Voltage Across External, Load-1 And Load-2

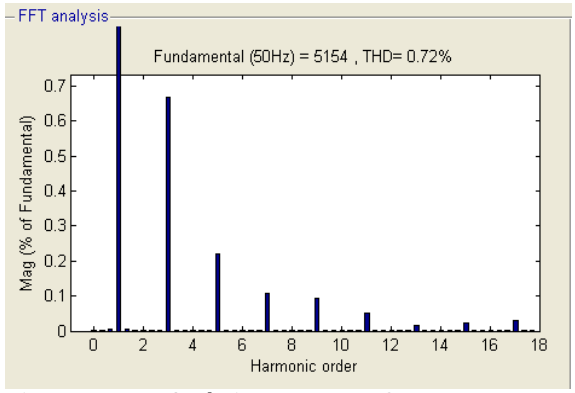


Figure 7c : FFT Analysis For Inverter Output

4. EXPERIMENTAL RESULTS

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

Laboratory model of DVR system is fabricated and tested in the laboratory. The driving pulses required by the inverter are produced by using Atmel microcontroller. These pulses are amplified using driver amplifier. The hardware layout is shown in Figure 8a. DC input voltage is shown in Figure 8b. Driving pulses applied to the inverter is shown in Figure 8c. The output of DVR system without filter is shown in Figure 8d. The output of DVR system with filter is shown in Figure 8e. It can be seen that the output is nearly sinusoidal.

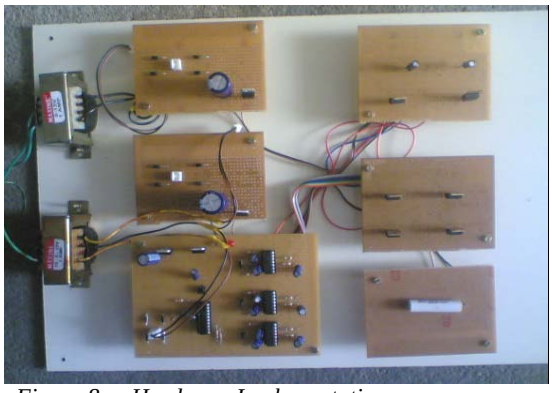


Figure 8a : Hardware Implementation

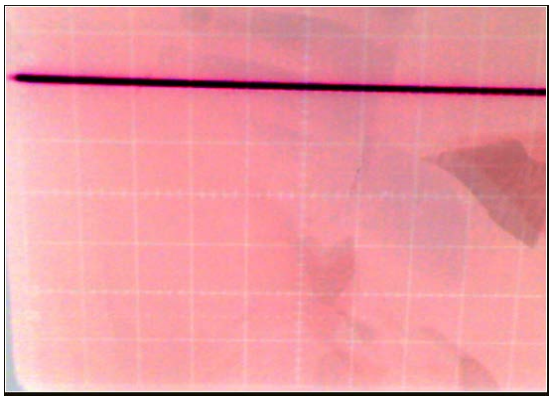


Figure 8b : DC Input Voltage

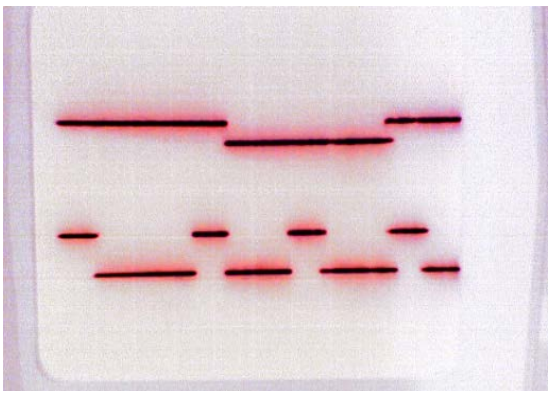


Figure 8c : Driving Pulses Of MOSFETS

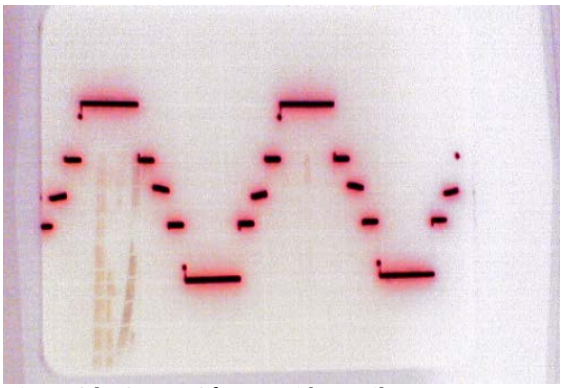


Figure 8d : Output Of DVR Without Filter

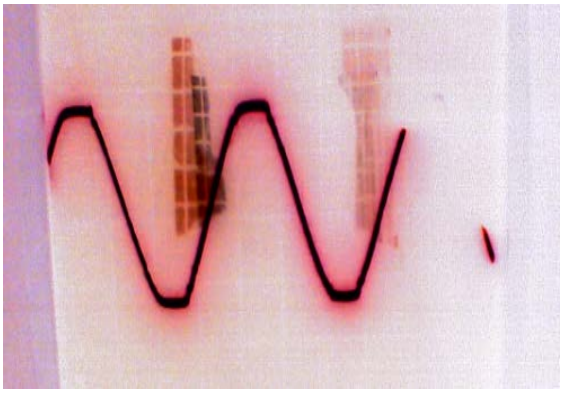


Figure 8e : Output Of DVR With Filter

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

5. CONCLUSION

This paper presents circuit modelling and simulation of DVR using cascaded five level inverter. This paper demonstrates the capability of DVR to improve the voltage quality. DVR structure is studied and the corresponding results are presented. The heating is reduced since the harmonics in the output of cascaded inverter are less.

The simulation is based on the assumption of balanced load and single phase circuit model. Five level inverter is a viable alternative since it has reduced harmonics. The experimental results are similar to the simulation results.

REFERENCES:

[1] B. H. Li, S. S. Cho, D. M. Vilathgamuwa, "Transformerless dynamic voltage restorer," *Proc.Instit.Elec.Eng.Gener.Transm.Distrib.*, Vol.149, May 2002, pp.263-273.

[2] M. J. Newman, D. G. Holmes, J. G. Nielsen and F. Blaabjerg, "A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level," in *Conf. Rec.IEEE-IAS Annu. Meet.*, 2003, pp.1228-1235.

[3] J.Y.Hung, " Feeedback control with Posicast," *IEEE Trans. Ind. Electron.*, Vol.50, Feb.2003, pp.94-99.

[4] D. N. Zmood, D. G. Holmes and G. Bode, "Frequency domain analysis of three phase linear current regulators," *IEEE Trans. Ind. Applicat.*, Vol.37, March/April 2001, pp.601-610.

[5] Z. Du, L. M. Tolbert and J .N. Chaisson, "Active harmonic elimination for multilevel inverters,"*IEEE Trans. Power Electrn.*,Vol.21, No.2, March 2006, pp.459-469.