Journal of Theoretical and Applied Information Technology
20th July 2013. Vol. 53 No.2

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

A DESIGN OF ANALOG VOLTAGE-MODE MULTIPLIER FOR UHF RFID PASSIVE IN 0.18UM CMOS PROCESS

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ABSTRACT

In this paper a "Low Voltage, Low Power, High Speed and High Linearity-CMOS Analog Multiplier for Modem ASK is proposed". The multiplier circuit is implemented in 180nm CMOS technology. It can be operated even at low Supply voltage VDD=0.9V. Band width of operation is about 4.10MHz, which is suitable for high frequency/high speed applications. This device modulates an analog carrier signal to encode digital information, and also demodulates such a carrier signal to decode the transmitted information. The goal is to produce a signal that can be transmitted easily and decoded to reproduce the original digital data.

Keywords: *Modulator ASK; ASK demodulator; Multiplier; Physical design; radio frequency identification (RFID).*

1. INTRODUCTION

Analog multiplier, Figure 1 is an important basic building block in communication systems like analog signal processing systems; for example frequency mixers, variable gain amplifiers, adaptive filters, phase-locked loop, amplitude modulators, frequency doublers, rectifiers and demodulators etc. It is necessary to design an analog multiplier circuit which is suitable for low power, low voltage and high speed applications with better linearity.

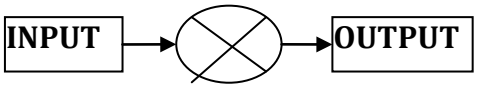

Figure 1.Basic Multiplier Symbol

Depending on the input/output, analog multipliers can be classified as, Voltage Mode Multipliers [1] and Current Mode Multipliers [2].

And also depending on the circuit configuration it can be classified as:

- Single balanced (2-quadrant), and
- Double balanced (4-quadrant) multipliers.

Quadrant based classification of multipliers is as follows:

- One-quadrant multipliers: Inputs are of the same phase
- Two quadrant multipliers: Opposite voltage can be added to either of the input
- Four quadrant multipliers: Opposite voltage can be added to both the inputs

2. FOUR-QUADRANT MULTIPLIERS USING SERIES CONNECTED TRANSISTORS

A voltage mode four quadrant analog multiplier based on a basic NMOS differential amplifier[1] can produce the output signal in voltage form can be constructed using four one-quadrant multipliers or by using two two-quadrant multipliers as shown in Figure. 2.

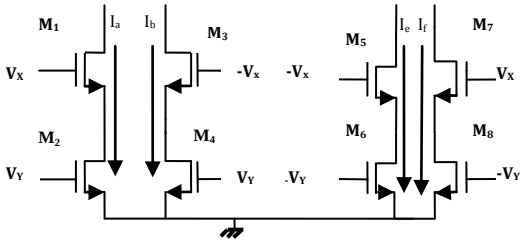

Figure 2.Four-Quadrant Multiplier

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$$I_a = \sqrt{I_{d_1}} * \sqrt{I_{d_2}} \quad (2.1)$$

$$I_b = \sqrt{I_{d_3}} * \sqrt{I_{d_4}} \quad (2.2)$$

$$I_{total_1} = I_a - I_b \quad (2.3)$$

$$I_a = k(v_{gs_1} - v_{th})(v_{gs_2} - v_{th}) \quad (2.4)$$

$$I_a = k(v_x - v_0 - v_{th})(v_y - v_{th}) \quad (2.5)$$

$$I_a = k(v_x - a)(v_y - b) \quad (2.6)$$

$$I_b = k(v_{gs_3} - v_{th})(v_{gs_4} - v_{th}) \quad (2.7)$$

$$I_b = k(-v_x - v_0 - v_{th})(v_y - v_{th}) \quad (2.8)$$

$$I_b = k(-v_x - a)(v_y - b) \quad (2.9)$$

$$I_{total_1} = 2kv_x(v_y - b) \quad (2.10)$$

$$I_e = \sqrt{I_{d_5}} * \sqrt{I_{d_6}} \quad (2.11)$$

$$I_f = \sqrt{I_{d_7}} * \sqrt{I_{d_8}} \quad (2.12)$$

$$I_{total_2} = I_e - I_f \quad (2.13)$$

$$I_e = k(v_{gs_5} - v_{th})(v_{gs_6} - v_{th}) \quad (2.14)$$

$$I_e = k(-v_x - v_0 - v_{th})(-v_y - v_{th}) \quad (2.15)$$

$$I_e = k(-v_x - a)(-v_y - b) \quad (2.16)$$

$$I_f = k(v_{gs_7} - v_{th})(v_{gs_8} - v_{th}) \quad (2.17)$$

$$I_f = k(v_x - v_0 - v_{th})(-v_y - v_{th}) \quad (2.18)$$

$$I_f = k(v_x - a)(-v_y - b) \quad (2.19)$$

$$I_{total_2} = -2kv_x(-v_y - b) \quad (2.20)$$

$$I_{total} = I_{total_1} + I_{total_2} \quad (2.21)$$

$$I_{total} = 4kv_x v_y \quad (2.22)$$

The above equation (2.22) shows the output of four-quadrant multiplier which is independent of threshold voltage and depends on aspect ratio (W/L) of the transistors. In the following section let us analyze the basic voltage mode multiplier using the four-quadrant multiplier with series connected transistors.

3. BASIC VOLTAGE MODE MULTIPLIER

Figure 3 shows the basic voltage mode multiplier structure which is constructed using four quadrant multiplier [5-6] with series connected transistors.

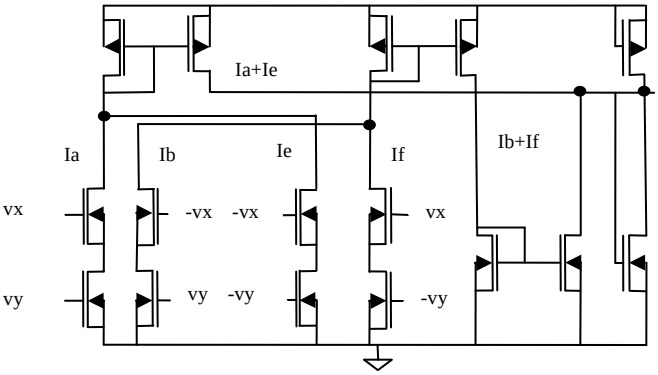

Figure 3.Basic Voltage Mode Multiplier Structure

Since it has to operate in all the quadrants, output of Vx*Vy and –Vx*-Vy are cross connected to get the total current Itotal1 and similarly the output of –Vx *Vy and Vx*-Vy are cross connected to get the total current Itoatl2.

4. SIMULATION RESULTS

The simulation results of schematic design for basic multiplier are presented. Different Analysis is performed to check the performance of the multiplier. Vx and –Vx 500mv, 1GHZ, Vy and –Vy 500mv, 10GHZ .the power consumed by the basic multiplier is 430.44µW

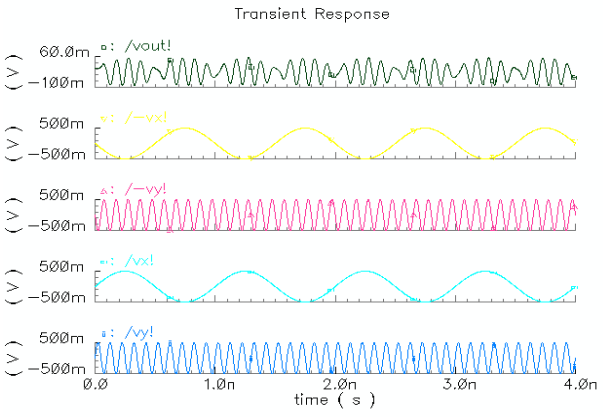

Figure4. Transient Analysis Of Basic Multiplier

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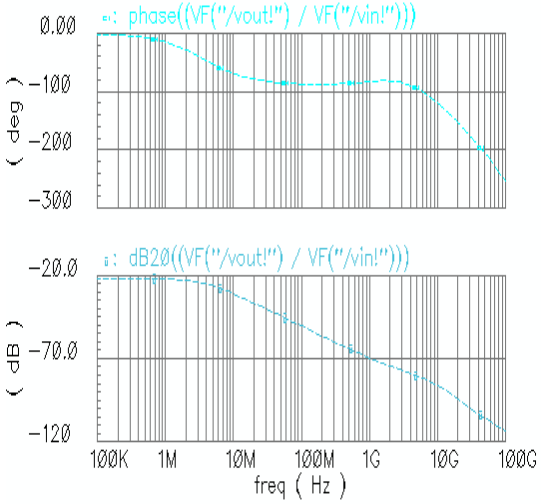

Figure 5. Ac Analysis Of Basic Multiplier

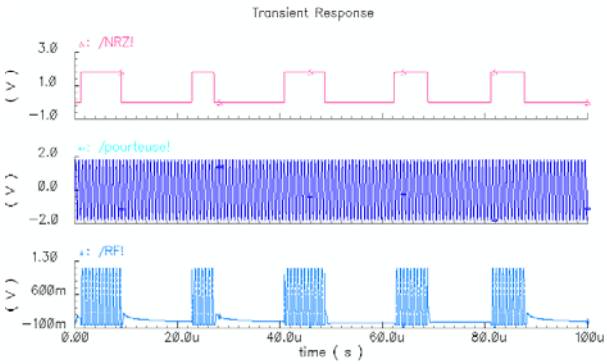

Figure 6. Signal Modulate In Ask

5. MULTIPLIER AS DEMODULATOR

Multiplier can be used as an ASK demodulator in

The new structure proposed as shown in Figure 7.

Figure 8 shows the output of proposed ASK demodulator circuit.

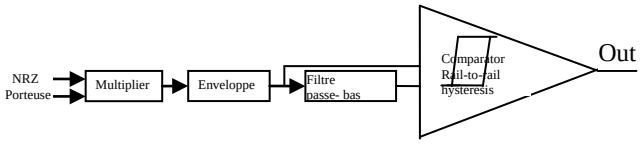

Figure 7.The Proposed ASK Demodulator

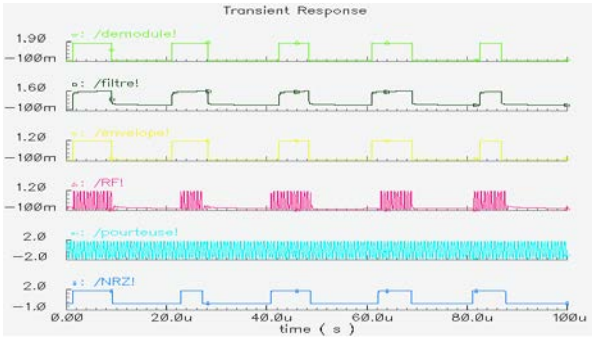

Figure 8. Outputs Of ASK Demodulator

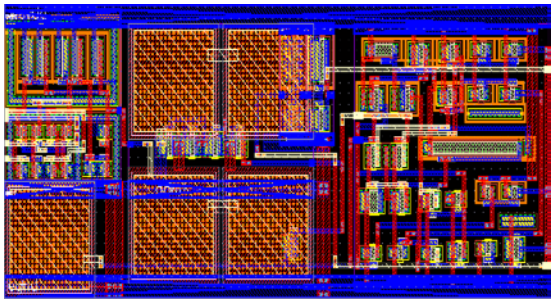

Figure 9. Layout Of The Ask Demodulator

6. CONCLUSION

In this paper a "Low Voltage, Low Power, High Speed and High Linearity-CMOS Analog Multiplier for Modem ASK is proposed". The multiplier circuit is implemented in 180nm CMOS technology with minimum transistor sizes (W/L=400nm/180nm). It can be operated even at low Supply voltage VDD=0.9V. Band width of operation is about 4.10MHz, which is suitable for high frequency/high speed applications.

7. ACKNOWLEDGMENT

This work was supported by: the National Center of Research Scientifique and Technique (CNRST Maroc) under the TIC R&D program.

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ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

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