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A 10-BIT 50-MS/S LOW-POWER PIPELINE ADC FOR WIMAX/LTE

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ABSTRACT

A low-power 10-bit 50-MS/s pipeline analog-to-digital converter (ADC) is described in this paper. The downscaling along the pipeline chain decreases the power and area consumption without sacrificing the performance of this converter, and a low power on-chip reference circuit is also helping to reduce power consumption. To improve sampling accuracy of the sub-ADC and minimize the offset of comparator, Digital Error Logic (DEL) is used. The ADC is implemented in a standard 0.13-µm CMOS technology and occupies an active die area of 0.6 mm^2. The differential and integral nonlinearity of the ADC are less than 0.27 LSB and 0.63 LSB, respectively. The ADC achieves 8.84 effective number of bits at full sampling rate with a 1-MHz input and consumes 50-mW from a 2.5-V supply.

Keywords: *Pipeline ADC, Transceiver, switched capacitor, WiMAX/LTE*

1. INTRODUCTION

The new generation of wireless-LAN based on the IEEE 802.11a/g standards imposes a significant challenge to circuit designers. The wide signal bandwidth demands a high sampling rate for ADCs used in the WiMAX and LTE system [1]. In WiMAX system, the ADC's power consumption is considerably big, thus the ADC power consumption should be kept low in order to extend the battery life in the portable wireless devices. In typical transceiver, 10-bit are needed in order to avoid an bit-error rate due to ADC's quantization [2]. As a key part of the transceiver baseband, the ADC is the most challenging building block.

In this paper, a 10-bit low-power pipeline ADC is presented. Section II describes the ADC's architecture and details the CMOS designs of the building blocks. Section III presents the measured results, and Section IV draws the main conclusions.

2. ADC ARCHITECTURES AND DESIGN CONSIDERATIONS

The block diagram of the proposed 10b pipeline ADC is illustrated in Fig. 1. The proposed ADC consists of a Sample-and-Hold circuit(S/H), eight cascading 1.5-bit stage and a 2-bit Flash ADC. The block of non-overlapping clock, current and reference generator is needed and Digital Error Logic (DEL) is used to correct the offset of the comparator.

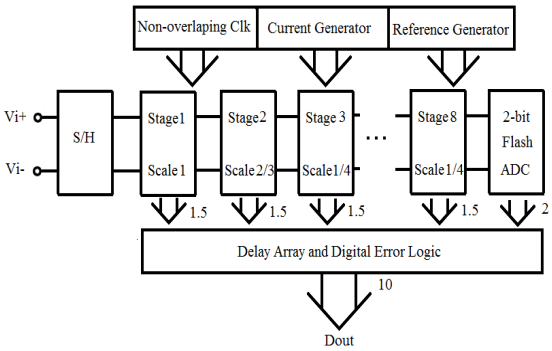

Figure 1: Block diagram of the pipelined ADC

In the S/H, the bootstrapped switch is used to minimize the distortion [3]. Sub-ADC is composed of two switched-capacitor comparator with high accuracy and low offset. Multiplying Digital-to-Analog Converter attains the 2X gain in each stage, the first stage has the highest specifications with respect to noise, incomplete settling and distortion. Furthermore, large sampling capacitors and high bias currents are necessary to keep the noise low and incomplete settling within the specifications [4]. The downscaling factor is 2/3 for the second stage, and equals to 1/4 for the other stages. Layout area and power consumption

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are optimized using this method with only a small degradation in the performance of the converter compared to an unscaled pipeline chain. The digital output of each stage is passed to the delay array and the DEL which can effectively correct the comparator offset.

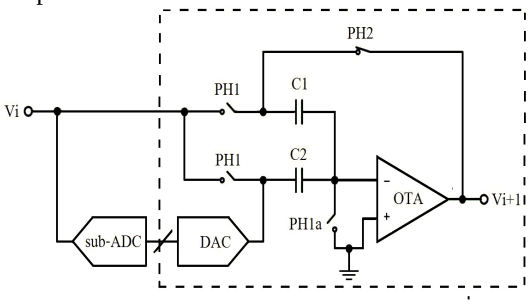

Figure 2: Circuit diagram of the pipeline stage

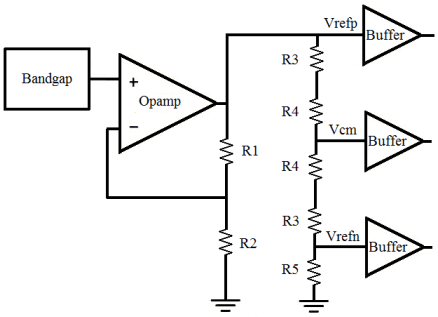

Figure 3: Schematic of the reference circuit

The circuit diagram of the stage is illustrated in Fig. 2. The sub-ADC converts the analog signal to relative digital signal. The DAC converts the digital signal to analog signal. The switch should be carefully designed to low the Ron and charge feedthrough. From the simulations, the spurious free dynamic range (SFDR) is relative to the Ron of switch. To achieve the sampling rate of 50 MHz, the unity-gain bandwidth of the OTA is designed to be above 500 MHz with 1.6 pF load to minimize the settling time. In the stage2, the scale factor is 2/3, the sampling capacitor (C1) and the feedback capacitor (C2) can be reduced to about 2/3 of the C1 and C2 in the stage1. The PH1 and PH2 is the sampling phase and amplifying phase respectively.

Each stage includes two comparators to compose the 1.5-bit sub-ADC. The switched-capacitor comparator is used to lower the feedback noise and offset. Because the 1.5-b/s pipeline architecture greatly relaxes the offset tolerance of the comparator, the comparator with minimum size devices is used. The comparison threshold is determined by the size ratio of the sampling capacitors, which is 1 : 1 in this design [2].

The reference of the ADC is in-chip in this design for little pins [7]. The in-chip reference schematic is shown in Fig. 3. The bandgap output is connected with the positive input of the op-amp. Vrefp is proportional to the ratio of the R1 and R2. The Vrefp and Vrefn are buffered to the all stages. The buffer used class-AB drives the large capacitive load because of the high current efficiency.

3. MEASURED RESULTS

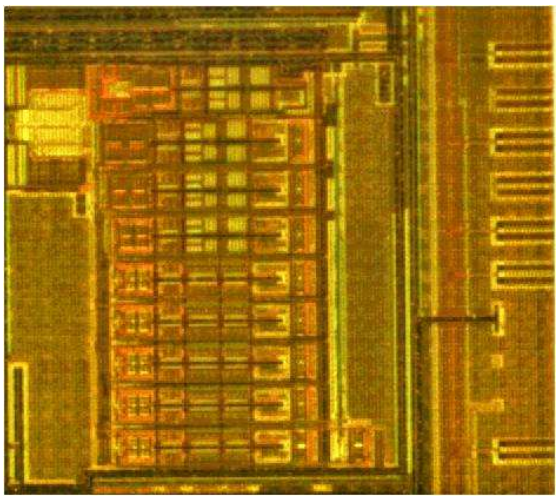

Figure 4: Die photograph

The proposed ADC was implemented in 0.13 µm single-poly eight-metal CMOS. The capacitors have a Metal-Insulator-Metal architecture. The ADC core dissipates 50 mW at 2.5 V and 50 MS/s and occupies an active die area of about 0.6mm^2.

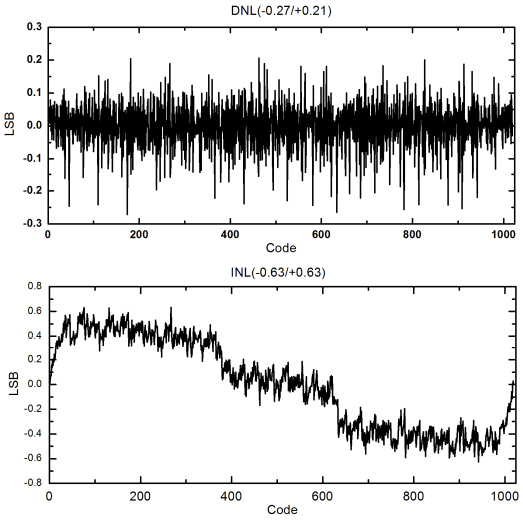

Figure 5: DNL and INL (Fs=12.5 M,Fin=1 KHz)

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The die micrograph of the ADC is shown in Fig.4. Fig.5 illustrates the static performance of the sampling signal at 12.5 MHz (Fs) and of the input signal at 1 KHz (Fin). Differential nonlinearity (DNL) / Integrated Nonlinearity are -0.27/+0.21 LSB and ±0.63 LSB respectively. From the results, the matching of the C1 and C2 is critical. Fig.6 illustrates FFT results of 50 MHz sampling results with 1 MHz input sin signal. In Fig.7, SFDR and signal-to-noise ratio (SNR) is illustrated with different input signal. Fig.8 illustrates the dynamic performance with the dependence on sampling frequency. SFDR can reach 74 dB with the Fs of 12.5 MHz and the input signal of 4.93 MHz.

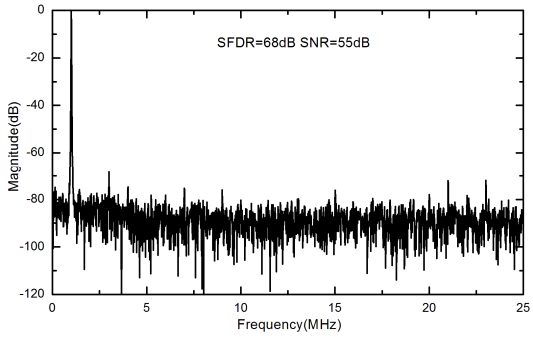

Figure 6: Measured FFT spectrum with 1-MHz input @ 50 MS/s

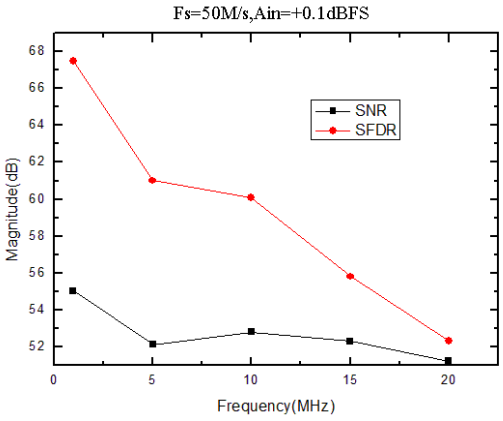

Figure 7: Measured ADC dynamic parameter versus different Fin

Table 1 shows the comparison of performance on several ADCs with similar resolution.

4. CONCLUSION

A 10-b 50-MS/s pipelined ADC with low power consumption and small area has been described. Using a stage scaling method, both the power dissipation and area of the ADC can be reduced significantly. The DEL is used to improve the sampling accuracy of the sub-ADC and lessen the comparator offset. The ADC is implemented in a 0.13 µm CMOS technology, occupies a die area of 0.6 mm^2 and consumes a 50-mW at 50 MS/s from a 2.5-V supply.

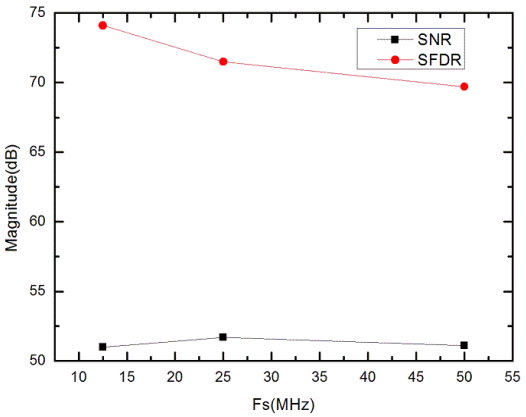

Figure 8: SFDR and SNDR versus Fs with 4.93-MHz input @ 50 MS/s

Table 1: Comparison with published 10-bit ADC.

Reference	[6]	[7]	This work
Supply(V)	1.5	3.0	2.5
Power(mW)	28	97	50
Input-swing	NA	2.4Vp-p	2.2Vp-p
SFDR(dB)	NA	69@40MHz	68@40MHz
SNR(dB)	56@40MHz	58@40MHz	55@40MHz
DNL(LSB)	-0.5/+0.5	-0.17/+0.21	-0.27/+0.21
INL(LSB)	-3.1/+3.1	-0.54/+0.56	-0.63/+0.63
Area(mm2)	0.27	1.4	0.6
Sample Rate	80MHz	100MHz	50MHz
Technology	0.13µm	0.25µm	0.13µm

5. ACKNOLEDGMENT

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REFRENCES:

[1] J. Arias, V. Boccuzzi, L. Quintanilla, L. Enriquez, D. Bisbal, M.Banu, and J. Barbolla, "Low Pipeline ADC for Wireless LANs", *IEEE J.Solid-Sstate Circuits*, Vol.39, pp.13381-1340, August 2004.

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

[2] H.J Wu, Z.P Li, H.B Zhang, and Y.P Wang, "A 12-bit 50MS/s Low Power ADC for WiMAX", *IEEE ICMAMT*, Vol.1, pp.11-14, March 2010.

[3] A.M. Abo and P.R. Gary, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter", *IEEE J.Solid-State Circuits*, Vol. 34, pp. 599-606, May 1999.

[4] Terje Nortvedt Anderson, Bjornar hernes, Atle briskemyr, Frode Telsto, Johnny Bjornsen, Thomas E. Bonnerud, and Oystein Moldsvor, "A cost-efficient high-speed 12-bit pipeline ADC in 0.18µm digital CMOS" , *IEEE J.Solid-Sstate Circuits*, vol. 34, pp.599-606, May 1999.

[5] Yun Chiu, Paul R. Gray, and Borivoje Nikolic, "A 14-b 12MS/s CMOS pipeline ADC over 100-dB SFDR" , *IEEE J.Solid-State Circuits*, vol. 39, pp.2139-2141, December 2004.

[6] P. Bogner, "A 28mW 10b 80MS/s Pipelined ADC in 0.13 µm CMOS" , *Proc. of the ISCAS 2004 Conf.*, pp. 17–20, 2004.

[7] Nan Wang, Ping Zhou, "A 10-bit 100-MS/s CMOS IP With Emphasis on layout Matching" , *IEEE Asian Conference of Solid-State Circuits*, vol. 12, pp.335-358, Nov 2006.