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MODELING AND SIMULATION OF OPERATIONAL AMPLIFIER USING VERILOG -AMS

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ABSTRACT

This paper puts forward a method of building a macro model of operational amplifier. And then it describes the way on how to use the Verilog-AMS language with the Cadence Virtuoso AMS simulator as a simulation tool in the behavior level. In order to verify the correctness of the behavior descriptions, the paper simulates the described op-amp in a basic integral operation. The result shows the macro model has appropriate accuracy while needs more less simulation time. The high-level model described by Verilog-AMS has advantages in not only reducing simulation time but also simplifying the simulation process. The method that uses macro model for simulation of the more complex system will become wide spread in system design in the future.

Keywords: *Verilog-AMS, Operational Amplifier(Op-amp), Macro Model, Power Consumption.*

1. INTRODUCTION

Op-amp (Operational amplifier) is one of the most important circuit in IC (Integrated Circuit) design. In the ideal situation, Op-amp has characteristics such as infinite differential voltage gain, zero output resistance and infinite input resistance. Yet in the reality, the op-amps are variety in structure, and each has its own characteristics. In circuit level it is reflected in the difference of circuit structure and performance.

Op-amp model has many forms. According to analyzing accuracy, it can be divided into ideal op-amp model, non-ideal op-amp model and op-amp macro model, etc. According to the function, the model can be divided into dc model, ac small signal model, large signal model and noise model [1], etc. When we design an Op-amp in system level, macro model got a very wide range of applications because of it does not involve specific transistors in the circuit and can simplify the simulation process to acquire the basic performance of circuit.

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This paper puts forward a different macro model of op-amp which described by Verilog-AMS. To verify the correctness of the macro model, the Verilog-AMS (Analog & Mixed Signal) is defined as a superset of Verilog-HDL and Verilog-A (Fig.1) [2]-[5]. Verilog-HDL is used to describe the digital circuit, it can undertake various levels of logical design, also it can be undertaken in digital system logic synthesis, simulations and time-series analysis, etc. In the previous paper of related works[6][7], the Verilog-AMS is only used focus on the mix-signal design. Yet we will make a in-depth research on how to building a model for a complex analog block such as the op-amp in a structure level. The results show that the Verilog-A can describes analog circuits from the structural level, behavior level in simulation. Therefore, Verilog-AMS has very powerful ability to describe mixed signal circuits. In section 2, the summary of the Verilog-AMS is presented. Its basic functions are described. In section 3, a macro model of an op-amp is built. The method of building a simple and a complex model for an op-amp is put forward. And the correctness of the complex model of the op-amp is verified. In section 4, this complex model is used in an integrating circuit. The results show that the simulation time is reduced and the process is simplified. The section 5 is the conclusion of the paper.

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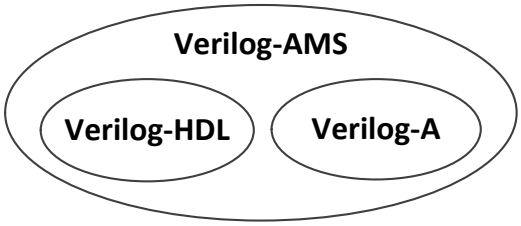

Fig.1. The relationship between Verilog-AMS, Verilog-A and Verilog-HDL

2. SUMMARY OF VERILOG-AMS

Verilog-AMS provides a single language and a single simulator that is shared between block designer and system designer and between analog designer and digital designer [2]. Therefore, it has a big impact on the design of mixed-signal system. Verilog-AMS can also provide an easy and single design flow, which can naturally support analog, digital and mixed-signal block. And in that circumstance, different designers that are responsible for analog, digital and mixed-signal design can work together more harmonious and communicate with each other more smoothly.

Verilog-AMS can be applied in five main aspects as below:

(1) To model components

The basic functions are such as describing the based devices, modeling the function block (A/D, filter, S/H etc.). The ability to add models to a circuit simulator such as Cadence Virtuoso AMS dramatically increases it range, and makes it immensely more powerful.

(2) To create a testbench

A testbench is used as a stimulus usually consisted by ideal component and provides a platform for circuit verification. When a designer wants to verify an A/D convert, a D/A convert as the stimulus is essential. Naturally, Verilog-AMS is used to solve the problem.

(3) To accelerate the speed of simulation

As the design is getting more and more complex, designers have to spend increasingly time to verify and simulate the design. Verilog-AMS describes circuit in behavioral level will be simulated faster than that of in transistor level.

(4) Can verify the mixed-signal system

Verilog-AMS can combine the simulation of analog, digital and mixed-signal design. It is extremely useful for verifying the mixed-signal system.

(5) Support the top-down design flow

Top-down design means first to divide the design to different blocks, and then realize blocks in high level. When verified in this paper the parameter titles should be written in uppercase and lowercase letters instead of all uppercase. Avoid writing long sentence as a paper title. Avoid writing long formulas with subscripts in the title; short formulas are fine (e.g., "θ1/θ2").

Full names of authors are preferred in the author field (given names followed by surname), but are not required. Separate a comma among authors; put a space between authors' initials, as well as an "and" between the last two, as shown in the authors' line.

3. MACRO MODEL DESCRIBED BY VERILOG-AMS

When we want to design an op-amp, we should definite the spec of it, such as power consumption, gain, PM and so on. Among those parameters, power consumption of the op-amp is mainly determined by Iq (static current), usually when we count it in a circuit power consumption, it must also add the load current. And we can use the power consumption to define the Iq of each part needed.

An abstract should have about 100 words and cover four points: statement of problem, methods of solutions, results and conclusion or discussion of the importance of the results.

3.1 Simple Macro Model of Op-amp and Described by Verilog-AMS

Gain, namely magnification is one of main indexes in op-amp. Simple model can only consider its gain and ignore other performance parameters. Based on these we can establish a Thevenin form of an Opamp model as shown in Fig.2.

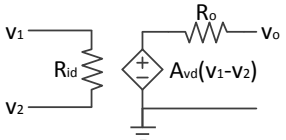

Fig.2. Thevenin form of op-amp model

And Fig.3 is the Norton form of op-amp model:

From these two models we can get that the output of the op-amp is: $V_0 = A_{vd}(V_1 - V_2)$.

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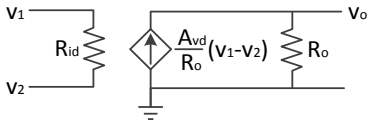

Fig.3.Norton form of op-amp model

And the description by Verilog-AMS is as below:

```
electrical out,inp,inn;
parameter real gain=1e5;
analog begin
  V(out)<+gain*V(inp,inn);
end
```

Use Cadence Virtuoso AMS simulator to simulate this model described by Verilog-AMS and obtain the result is as below:

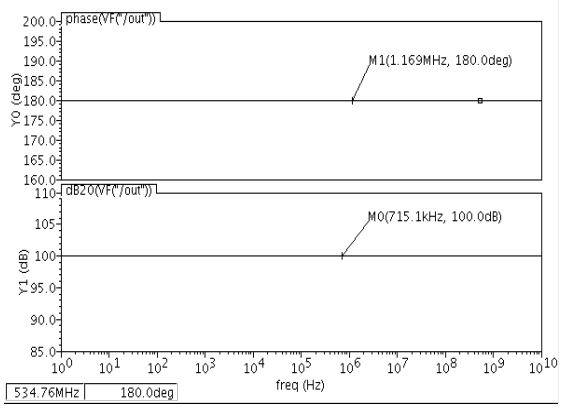

Fig.4. Simulation result of a simple op-amp model

From Fig.4, it can be seen that the op-amp gain is 100dB (20log105), phase tolerance is 180°, namely the bandwidth is infinite. It has the same characteristics with the model in Fig.2 and Fig.3.

3.2 Complex Macro Model of Op-amp and Described by Verilog-AMS

The complexity of the op-amp model depends on how to use the characteristics to establish the model [1]. When we design an op-amp with transistors, the power consumption, gain, bandwidth, slew rate are very important parameters that must be concerned. And these parameters will decide whether the op-amp can work properly in the system. Therefore, when we establish a model, these parameters must to be considered carefully. Then we can establish the op-amp frequency characteristic model. Besides the gain, it also contains the op-amp offset voltage and current, bandwidth and slew rate.

Unity-gain bandwidth is the frequency when op-amp open-loop gain is equals to 1, shorted by GBW.

$$GBW = \frac{g_m}{2\pi C_1} \quad (1)$$

Which gm is the transconductance of the op-amp and C1 is the capacitance that generated the dominant pole [8]. And slew rate SR stands for the adaptive capacity of op-amp to signal change rate, it unit is V/us.

$$SR = \left| dV_o / dt \right|_{\max} \quad (2)$$

It is common to set the output poles for secondary primary pole. Then the dominant pole will be generated in internal circuit. We can utilize R1 and C1 (Fig.5) to establish the dominant pole model in frequency response. If set R1=R0, the model can simulate output resistance like the case that the following figure shows [1].

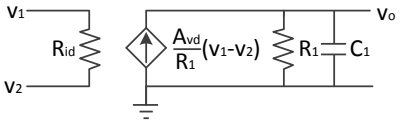

Fig.5. op-amp macro model with the frequency response

And the transition function is as below:

$$H(s) = \frac{A_{vd} / R_1 C_1}{s + 1 / C_1} \quad (3)$$

The output impedance (use R1 to simulate output resistance) is a frequency function in the macro model of Fig.5. If we want the output impedance keep constant, we need to do a further improvement like Fig.6. It adds a node and uses an additional controlled source to isolate the relationship between output impedance and voltage gain frequency response. The additional controlled source will work as a buffer to isolate the op-amp with the following stages. For the reason of the mismatch in the layout and the circuit design，the offset effect must be included. So the offset voltage and offset current also be added into the model.

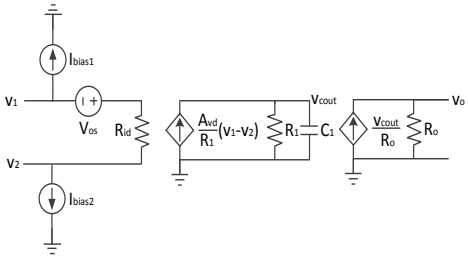

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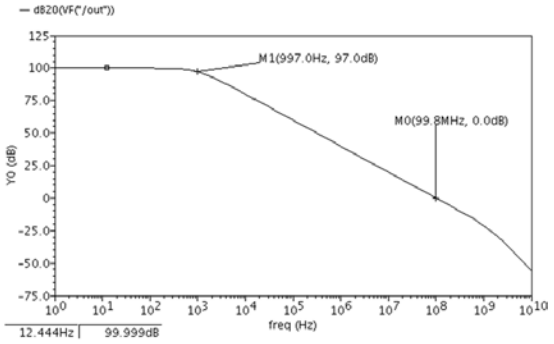
Fig.6. Op-amp macro model with the frequency response and constant output impedance

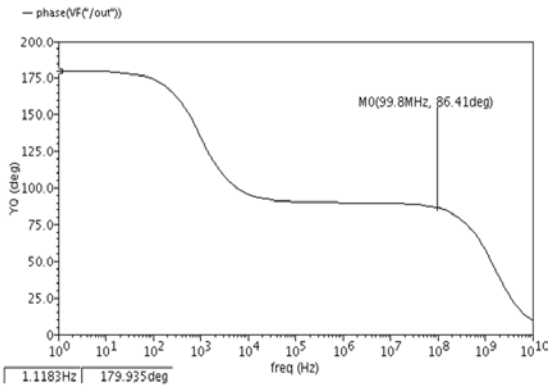
The initial parameters of the op-amp will be set as that the gain=100dB, GBW=100MHz and the SR=0.5V/us. Then the description by Verilog-AMS is as below:

```
electrical cout;
real Vin_real;
real C1,gm,R1;
parameter real Vos=0;
parameter real Rin=1M;
parameter real Rout=100;
parameter real gain=1.0e5;
parameter real GBW=1.0e8;
parameter real iin_max=100e-6;
parameter real slew_rate=0.5e6;
parameter real ibias=100e-6;
analog begin
 @(initial_step)
  begin
   C1=iin_max/slew_rate;
  gm=2*`M_PI*freq_unitygain*C1;
   R1=gain/gm;
  End
 I(inn)<+ibias;
 I(inp)<+ibias;
 Vin_real=V(inp,inn)+Vos;
 I(inp,inn)<+Vin_real/Rin;
 I(cout)<+-gm*Vin_real;
 I(cout)<+C1*ddt(V(cout));
 I(cout)<+V(cout)/R1;
 I(out)<+-V(cout)/Rout;
 I(out)<+V(out)/Rout;
end
```

Simulate this model described by Verilog-AMS and obtain the result is shown in Fig.7.



(a) Amplitude-frequency



(b) Phase-frequency

Fig.7. Simulation result of complex op-amp model

We know that the reasonable value of a CMOS op-amp input resistance is about 1M and the out resistance is 100. The result of the simulation of this model shows that the GBW of the op-amp is nearly 100MHz. And the -3dB bandwidth is about 1MHz. The phase margin of the op-amp is 86.4°. This shows that the out put pole is the secondary primary pole and the dominant pole is generated in internal circuit.

4. THE APPLICATION OF OP-AMP MODEL DESCRIBED BY VERILOG-AMS

In this section, the macro model will be used in more complex system. The integral operation circuit is a circuit that often applied to analog circuit, its principle diagram is in Fig.8.

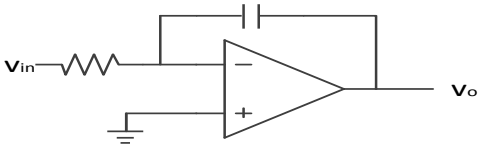


Fig.8. Integral operation circuit

The relationship between input voltage and output voltage is: $V_o(t) = -\frac{1}{RC}\int V_{in}(t)dt$

Then the description by Verilog-AMS is as below:

```
//Verilog-AMS HDL for "thc_UIRFPA_AMS_10DEC20", "integrator" "verilogams"

`include "constants.vams"
`include "disciplines.vams"

module integrator (out,level,in);
 output out;
```

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```
 input in,level;
 electrical out,in; disciplines
 logic level;
 integer assert;
 parameter real ic=0;
 parameter real gain=-1e9;
 parameter real reference=2.4;
 analog begin
  if(level)
   begin
    assert=1;
   end
  else
   begin
    assert=0;
   end
  V(out)<+gain*idt((V(in)-
reference),ic,assert)+reference;
 end
endmodule
```

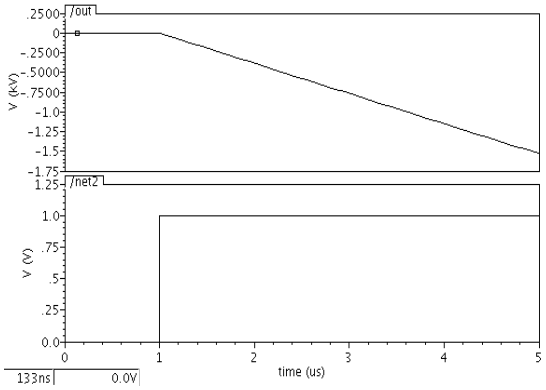

Fig9. The result of integrating circuit

We applied the macro model of op-amp that described in III by Verilog-AMS to integral operation circuit. The result is shown in the Fig.9. In the figure, it can be seen that when the input step signal is applied, the output signal is the backward integration of input signal. The function of the integrating is correctly achieved. And also we find the simulation time is reduced in about 30% compared to the simulation in a transistor level.

In the meantime, the simulation result in Fig.9 also maintains an appropriate accuracy. And the simulation process is simplified by just editing several lines of Verilog-AMS language sentence instead of drawing complicated circuit schematics. The usage of this method is also very important for the Top-down design. For the system designer can define the spec of the op-amp before the design of the total integrating circuit. And the trade-off between the system level and the circuit level will introduces benefits to the work of the circuit designers.

5. CONCLUSION

This paper puts forward a method of building a macro model of op-amp, and describes these models by using Verilog-AMS, then using Cadence Virtuoso AMS simulator to do the simulation and validation. Finally, it uses a macro model of op-amp that described by Verilog-AMS to a integration operator to further verified the correctness of the models. The simulation results show that Verilog-AMS as a kind of hardware description language, can describe circuit in the high-level, simplify the simulation process and reduce the simulation time while can maintain the appropriate accuracy. It also has very important significance in the Top-down system design.

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