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RESEARCH AND DESIGN OF CPU FOR TEACHING BASED ON SPARC V8

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ABSTRACT

Research and design of CPU for teaching has been a hotspot of computer professional teaching. The verification experiment is given priority tothe computer system structure and principle experiment course offered by the University at present and this is not conducive to students making the theory and the modern computer industry combination. Based on leon2 kernel, CPU for teaching based on SPARC V8 is designed. Leon2 kernel is broken down to independent functional modules from top to down, then a teaching experimental platform is built using EDA software provided by the company Mentor and SPE¬_C integrated development environment. Finally, students who use the teaching experiment platform can do self-determined design based on Leon2 kernel modules. Teaching experiment indicates that the research is beneficial for students to do more in-depth study and search on the structure of the computer, thereby improving the quality of practice teaching for computer system structure and principle.

Keywords: *CPU for teaching, System Structure, SPARC V8, Leon2, Self-determined design*

1. INTRODUCTION

The experiment is essential in Principles of computer organization and system structure in courses[1]. Through experiments, students will be able to grasp theory learned in the lesson, combine theory and practice and improve their practical capacity[2]。

Designed and verified by students in the teaching have become important elements of the experiment, and CPU design [3] occupies a very important place in the teaching of computer majors. CPU is the control center for the entire computer system, but also the most complex parts of the system [4]. In your computer knowledge structure, CPU plays a critical role of connecting between the preceding and the following. Via the theoretical basis and design experience of CPU, students whether are engaged in hardware design or software development in the future will be of great help. Confirmatory experimental model in the teaching process for the CPU design is based on [5], such as the processor instruction set design, the design and realization of the pipeline, the pipeline conflict and cache performance analysis. These experiments are based on a simulated environment. Simulation refers to: students experiment in set environment, performing simulating experiment used software given by teachers. Students quickly finish the experiment in the simulation environment, grasping a certain amount of knowledge. However, they can't get the opportunity to build real computer prototypes and free play space. Independently design could not be made well without the structure to conduct more in-depth research and exploring to your computer, which greatly limits the improvement of students' practical ability.

In order to solve the problems existing in the teaching experiment, this paper presents the research and design of CPU for teaching based on the SPARC V8 architecture. This design is not emulated CPU design instead of using the Leon2 processor based on SPARCV8 architecture as a design instance, and use EDA software for teaching provided by the Mentor Company and SPE_C integrated development environment to build the teaching experiment platform. Leon2 kernel is broken down to independent functional modules from top to down, these independent modules are precisely the functional modules required to constitute a complete CPU, and then in the building on the experimental platform of the various functional modules are independent simulation, finally student experiment independently using the platform designed and Leon2 kernel modules are provided. Through this research and design, it establishes a teaching-oriented design of open CPU platform. Providing

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students a platform for designing independently and space for free play. Students can achieve more complete and in-depth understanding of computer composition and purpose of the knowledge system structure in the CPU design process, thereby enhancing the quality of experimental teaching of computer composition principle and system structure. The system uses the fpga development board of independent design, and figure 1 shows:

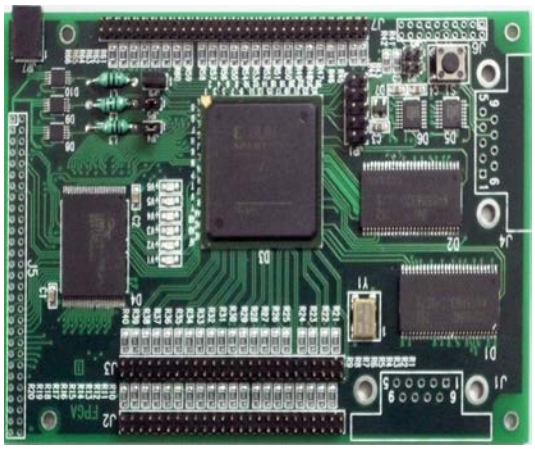

Figure 1: Fpga development board

2. SPARC V8 ARCHITECTURE AND Leon2 PROCESSOR

A. *Introduction of SPARC V8*

SPARC, all called "Scalable Processor Architecture ", is a kind of processor architecture that performance can be improved proportional to the technology, is developed by the Sun Company in 1985 on the basis of RISC II architecture, which is researched by the University of California, Berkeley. It is a CPU instruction set architecture [6]. Extensible command set of SPARC can improve the efficiency of enforcement procedures and optimization of a compiler generated code, thus making the code execution is more efficient and fast. Architecture [7] uses a "register Windows" system, and this system structure for users, especially in large applications, enables the compiler to generate more directly, efficiently and optimize your code. Relative to the other RISC architecture[8], this window structure minimizes memory load/store instructions and accelerates the speed of code execution. For languages such as C++, where object-oriented programming is dominant, register windows[9] result in an even greater reduction in instructions executed. When you run under the operating system, context switching between the processes in this structure can be carried out faster. Overall, the SPARC architecture has the following outstanding features:

1) Unified format for instruction decoding;
2) Instruction plates, symmetric, simple basic ways of addressing 2~3 kinds;
3) Most of the instructions are single cycle instruction with five stage pipeline;
4) Using mass-register ("register Windows" system);
5) Only the LOAD/STORE instruction can access memory.

B. *Introduction of LEON2*

Leon2 was developed by Gaisler Research Company in 2003, which implements a 32-bit processor confirming to the IEEE-1754 (SPARC V8). It is a processor IP core designed for embedded applications. Its predecessor, ERC32 and Leon are developed by the ESA. Leon2 mainly balances performance and price, reliability, portability, scalability, software compatibility, and so on. Its Internal hardware resources can be configured, it is primarily intended for embedded systems, you can use the FPGA/CPLD and ASIC technologies[10] to perform. Leon2 processor on-chip resources are as follows: separate instruction and data caches, hardware multiplier and divider, interrupt controller, debug support unit with trace buffer, two 24-bit timers, two UARTs, power-down function, watchdog, 16-bit I/O port, flexible memory controller, Ethernet MAC and PCI interface. Leon2 VHDL module is available on the most comprehensive tools for simulation, and can be in any VHDL87 compliant emulator emulation; new modules designed with AMBA AHB/APB bus architecture can easily join the Leon2, completing user customization of the application. A block diagram of LEON2 can be seen in figure2. Structure of the entire system supported by the AMBA AHB and APB, connects SPARC processor, the Cache system and on-chip peripherals and other equipment.

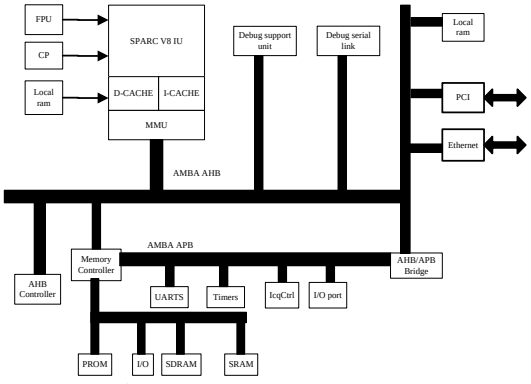

Figure 2: Leon2 structure

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Currently Leon2 has a wide range of applications at home and abroad. ThumbPod fingerprint security system at the University of California, Los Angeles, and the NJ1030 GPS baseband products of Nemerix Company uses the Leon2 processor. Domestic aerospace develops Satellite data processing system based on Leon2, Leon2-based satellite image processing system also has been developed by National Astronomical Observatory of the Chinese Academy of Sciences. This study for Leon2 downloads Leon2 kernel on the FPGA, and then uses the instructions prepared making the Leon2 processor running. Students are in a truly independent on processor design after that Leon2 is decomposed into individual functional module. And Leon2 kernel source code is open source, students according to their own ideas to make repeated modifications, thereby making more in-depth exploration and study on the structure of the computer.

3. DESIGN OF CPU FOR TEACHING BASED ON LEON2

In order to realize the design for teaching experiment platform based on SPARC V8 architecture design, this paper makes Leon2 processor as a design example. Leon2 kernel is broken down to independent functional modules from top to down, and then making an analysis and emulation for each module. On the basis of more in-depth study and search on each module, completing module teaching experimental design combined with teaching experiments requirement. In the use of these modules to experimental design requires EDA and FPGA technology. With Mentor companies providing hardware and software collaborative simulation environment to implement hardware and software collaborative simulation for each module. Combining hardware and software collaborative simulation lead students to better understand the structure and function of the various modules, here on the design of the key modules of the experiment are described in simple.

A. *Pipeline Experiment*

Pipeline experiment is aimed at the Leon2 integer unit IU. Integer unit using five stage pipeline structure, respectively fetching (FE), decoding (DE), executive (EX), memory (ME), writing back (WR), performs all other instructions in addition to floating point processor and coprocessor. Five-level pipelined implementation process as shown in Figure3.

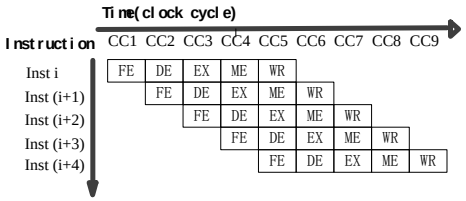

Figure 3: five-stage pipeline

The instruction fetch cycle (IF), according to the PC instruction address fetches instructions from memory into the instruction register IR, while PC value plus 4, pointing to the next instruction in sequence; the instruction decode (ID), instruction is decoded, reading the desired operand accessing the common group of registers via the register number of IR; In the implementation cycle (EX), ALU, logic, and shift operations are performed; the memory access cycle (MEM)established specifically for the LOAD/STORE directive, if it is a load instruction, using a cycle of effective address read out the corresponding data from the memory, if it is a store instruction, it writes data to the specified effective address points out storage unit; the write-back cycle (WB), the result of any ALU, logical, shift, or cache read operations are written back to the register file.

In the design process of making VHDL language describe five-stage pipeline function modular, get the structure block diagram. Through the structure block diagram, students can better understand the working principle of five pipeline stages. On the basis of this designing, a series of experiments are done. Combining with the study of computer system structure content, students modify function code of the five-stage pipeline, and use different ways to achieve the function of each stage. Experiment design of assembly line process, in addition to outside of the e-class line of the module also need to set the data path and control module. Through the data path and a control part, a clear understanding of the data in the process of operation is how to send number, store, access, operation, the output results, but also clearly seethe control signal in data operation process is how to control.

B. *Pipeline Conflict Experiment*

In the integer unit learning, it must pay attention to five-stage pipelined implementation and module function, but also solve the pipeline conflict problems in the implementation process, such as conflict of data and structure, mastering the solutions to these conflicts. Accordingly in the IU teaching around these areas experimental design is made.

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Combination with other modules, Students verify the implementation process of a command in the IU, through their own written instructions to achieve five stage pipelined execution. After work in the familiar five-line paragraphs, it also uses non-line approach to instruction features, instructions are executed in the manner and with the lines of the results are compared.

In the pipeline to execute instructions, students observe whether there exists correlation and conflict, and find solutions to conflicts and problems related to the method. In the next experiment, lines smooth implement, and there is no conflict and the related issues. Through the computer architecture course and various experiments designed in IU module, to understand a command execution process, at the same time, in the course of experiment improving students' the ability to solve and analyze problems. Taking cycle subtraction as an example, experimental result diagram is shown in figure 4:

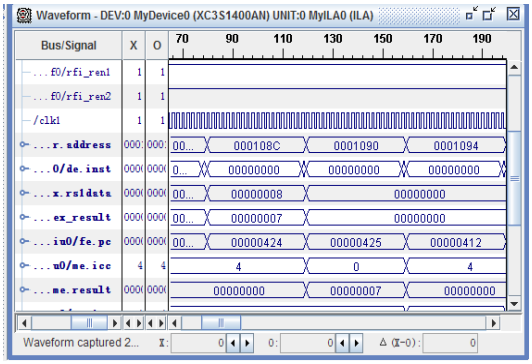

Figure 4: Waveform simulation diagram

C. *Cache Performance Experiment*

The LEON2 processor implements the Harvard architecture with separate instruction and data buses, connected to two independent cache controllers. Cache controller is the core module of the whole cache system. The controller is primarily performed two tasks: CPU read and write data request and processing of cache instructions read/write main memory. Cache subsystem's configurable model has direct mapping mode and 2~4 group linked to multiple associated mode; optional three replacement algorithm is LRU, LRR and pseudo random. Harvard structure divides cache, eliminating the conflict between data references and instructions reference, the data and instruction fetch can proceed at the same time, thus greatly improve the processing speed [11]. Harvard architecture allows you to independently select and optimize the cache size, line size and associate degrees, making teaching design for great freedom. This article discusses how to improve cache performance, the solution of cache system and IU data inconsistency problems to realize teaching experiment design.

In order to master cache capacity, associative degree, block size effect on the performance of cache [12], students can redesign based on the existing VHDL code based on, choosing the basic parameters, including capacity, associative degree, block size, a write strategy and replacement strategy. While the selection of these parameters, needs comprehensive consideration of cache hit ratios, average power consumption of the average access time, and cache performance. Students will own the modified code emulation to get diagrams of the various parameters and cache failure rate, so as to get the best selection of performance parameters. Through ownership of the cache design student thoroughly understand the factors that affect the performance of cache.

D. *Data Inconsistency of cache Experiment*

Because of the cache, the data may be in memory or in the cache, as long as the CPU is the only device that changes and reads data, and cache exits between the CPU and memory, there is no access to a copy of the old or inconsistent risks. However, I/O devices to access memory may result in inconsistent memory and cache data, or make other devices to read invalid copies. Designing experiment for this issue, at the time of data inconsistencies, students find the cause and solve the problem. In Leon2, dataflow of IF can be seen in figure 5. When IU is taking instruction cycle, addresses on the one hand are sent to the controller, address and read signal issued by the controller to the I-Cache address, and then the instructions are removed from I-Data into the instruction registers of IF/DE. On the other hand, addresses are sent to address registers of IF/DE.

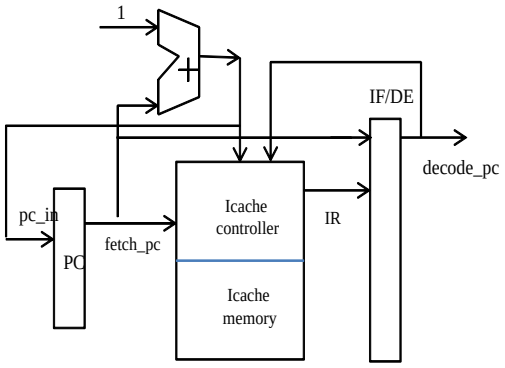

Figure 5: Dataflow of IF

Sending address from the controller to the I-Cache to the directive fetched needs a clock cycle,

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if the Cache misses, needs more than one clock cycle. That there is a problem: IR instruction address is whether consistent with the NPC, that is deposited in the NPC's address is whether the address of the instruction in the IR. Students come up with their own design ideas to solve this problem, and in the problem solved process, students can be more familiar with Cache controller working principle, and be able to apply what they are learning knowledge into practice.

E. *Interrupt Experiment*

The LEON interrupt controller is used to prioritize and propagate interrupt requests from internal or external devices to the integer unit. In total 15 interrupts are handled, divided on two priority levels. When designing interrupt experiment, on-chip peripherals are needed. Through the separating module, the student know the CPU is how to respond when an interrupt occurs, and they can also know the CPU is how to set the corresponding position to handle the interrupt and scene protection and recovery process in CPU treatment interruption. On that basis, students prepare the interrupt service routine for an interrupt source. In the preparation of the interrupt service routine, that he interrupt controller should be how to modify is the problem that students should solve by themselves, but also consider the issue of priority interrupt source. Through the interrupt service program and the concrete realization process, Students themselves master interrupt processing system principle, and can be able to handle a specific interrupt, thereby achieving the objective of a thorough study of interrupt processing.

In the principles of computer organization and system structure of experiment, interrupt learning is a difficulty. In previous experiments, the interruption experiment just other stationary model, students only mechanically do experiments in accordance with the requirements of teachers, and cannot have in-depth understanding of specific work process for interruption. Through the Interruption experiment designed above and the interrupt service routine, students are well mastered the interrupt, the interrupt response and interrupt processing technology. Taking UART as an example, experimental result diagram is shown in figure 6:

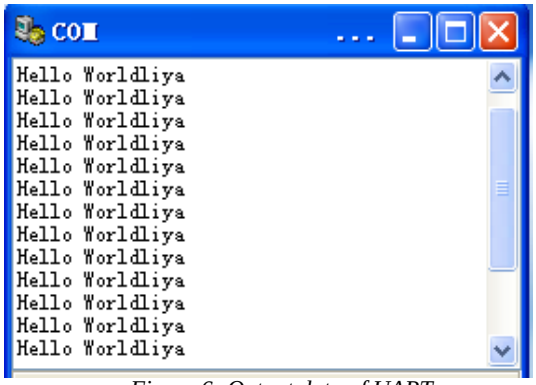

Figure 6: Output data of UART

4. CONCLUTION

With the Leon2 processor, this article designs experiments on some modules, such as five-stage pipeline, Cache and interrupt controller. In the process of experimental design, some modules are presented only block diagram, the specific contents require students to use VHDL hardware description language, and students should be able to solve compiled debugging difficulties as far as possible according to the theoretical study. After the completion of functional simulation, downloading it to self-design FPGA Development Board for hardware debugging and simulation. Through the completion of above experiments, students will be independent design and hardware emulation, deepening the understanding to theory, and increasing the practice experience, so as to enhance students' ability to analyze questions and solve questions. At the same time, this paper's study and design of CPU for teaching has accumulated valuable experience for our country CPU design.

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