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DESIGNING OF A PULSE WIDTH MODULATION SYSTEM USING EMBEDDED SYSTEM DESIGN TECHNIQUES

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ABSTRACT

Pulse Width Modulation (PWM) signals have wide applications in different field as communication and control systems. This paper introduces a design of a Micro Blaze soft core processor system that can be accommodated to act as PWM system. The designed processor system is programmed in C language to act as PWM system. The obtained results are traced on chip scope integrated logic analyzer and on oscilloscope for the purpose of comparison .The percentage error is less than 1%.

Keywords: *Soft-Core Processor ,Embedded System, FPGA, Pulse Width Modulation(PWM) , Spartan 3E*

1. INTRODUCTION

PWM signals are widely applied to power electronic circuits and electrical drives [1]. The PWM signal can be generated based on the use of either analog circuits or digital circuits. Using embedded system techniques to generate PWM signal is easier and more suitable for complex structures.

Many digital and transistor logic circuit (such as processors, microcontrollers, etc) can develop PWM, but what is interesting is to design the PWM using the latest programmable device so as to use the features of FPGA. FPGAs based PWM controller is the choice of every controller designer, because of the design fidelity ,flexibility, and simplicity[2].

EDTs helps the designer to construct a processor system with peripherals on FPGAs .The processor system can then be programmed to act as what the designer aims, The soft-core processor used in this work is MicroBlaze type.

A design of Pulse-Width Modulated (PWM) embedded module is based on an 8-bit MCU compatible with 8051 family ,the PWM module can support PWM pulse signals by initializing the control register and duty-cycle register is proposed by [3] .in a digital technique to generate Pulse Width Modulation (PWM) signal using counters, comparators, and latching circuits implemented by Verilog HDL program based on FPGA is presented by [4] . New Type of PWM Peripherals In Nios II processor by alter was designed and accommodated by [5] to count of the frequency and the duty cycle.[6] described how to generate pulse width modulated controller use trapezoidal rule.

The target of the paper is to generate PWM signal to be implemented on FPGA, using EDTs and to be configured on Spartan 3E slice.

2. EMBEDDED DESIGN TECHNIQUES

Figure (1) displays the philosophy of embedded design techniques that is used to construct the soft core processor system[7].it is composed of the hardware part and software part .The hardware part is described in Microprocessor Hardware Specification(MHS) file and transferred to a bit file using ISE design flow(design entry , synthesis, implementation ,verification, device programming).The software part is described in microprocessor software specification (MSS) file and transferred into ELF file through software generation steps .Both bit file and ELF file are transferred into a system bit file through Data2MEM stage, there the bit file can be configured on FPGA through JTAG.

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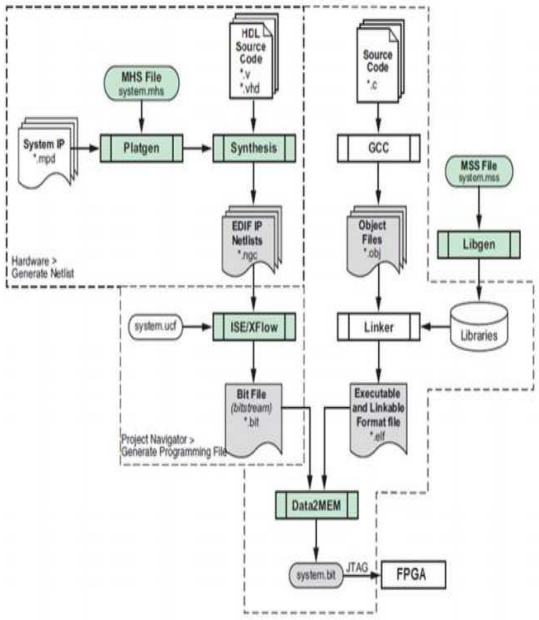

Figure 1. Embedded Design Philosophy

The hardware part of the system is as shown in figure 2,it is composed of:

1. The MicroBlaze embedded soft core processor which is a reduced instruction set computer (RISC) optimized for implementation in Xilinx Field Programmable Gate Arrays (FPGAs) [8].

2. Processor Local Bus (PLB) v4.6 that provides bus infrastructure for connecting an optional number of PLB masters and slaves into an overall PLB system [9].

3. Multi-Port Memory Controller MPMC which is a fully parameterizable memory controller that supports SDRAM/DDR/DDR2 memory [10].

4. DDR-SDRAM with 64 Mbytes that is used for program execution , it is accessed by MicroBlaze using Multi-Port Memory Controller (MPMC)[10].

5. BRAM Block which is a configurable memory module that attaches to a variety of BRAM Interface Controllers[11].

6. LMB BRAM Interface Controller which is the interface between the Local Memory Bus(LMB) and the bram_block peripheral. A BRAM memory subsystem consists of the controller along with the bram_block peripheral[12].

7. Universal Asynchronous Receiver Transmitter (UART) Lite Interface that connects to the PLB (Processor Local Bus) and provides the controller interface for asynchronous serial data transfer. This soft IP core is designed to interface with the PLBV46[13].

8. Timer/Counter Module that connects to the PLB (Processor Local Bus) and it is a 32-bit timer module[14].

The software part is composed of two main portions, software part configuring the Board Support Package (BSP) and writing the software applications. The configuration of the BSP includes the selection of device drivers and libraries. The Board Support Package (BSP) is a collection of files that defines the hardware elements of system for each processor. The BSP contains the various embedded software elements, such as software driver files, selected libraries, standard I/O devices, interrupt handler routines, and other related features[7]. Software applications is the code that is runs on the software platforms . it is written in C language .

3. GENERATION OF PULSE WIDTH MODULATION USING EDTS

The Plus Width Module (PWM) outputs a square wave with modulated period and modulated duty cycle as shown figure(3). The frequency of the PWM is the inverse of the period (1/period).

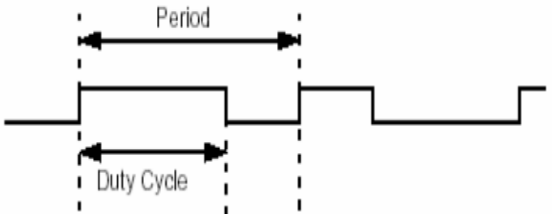

Figure 3. Pulse Width Modulation Waveform

The timers that were constructed in the hardware part as shown in figure (2) were used to generate the PWM signal, they are organized as two identical timer modules as shown in Figure 4. Each timer module has an associated load register that is

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used to hold either the initial value of the counter for event generation, or a capture value, depending on the mode of the timer[14].

There are three modes that can be used with the two Timer/Counter modules[14]:
• Generate mode
•Capture mode
• Pulse Width Modulation (PWM) mode.

In PWM mode, two timer/counters are used as a pair to produce an output signal (PWM) with a specified frequency and duty factor. Timer0 sets the period and Timer1 sets the high time(duty cycle) for the PWM output[14].

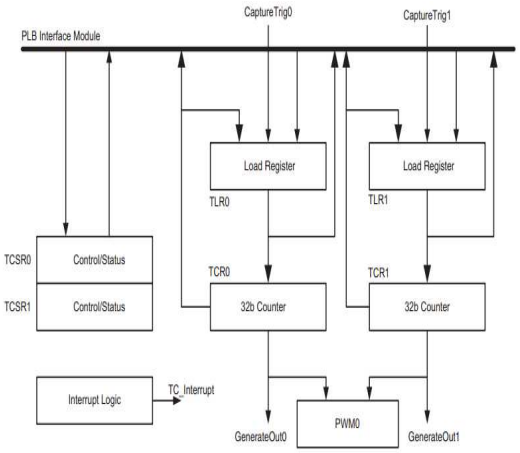

Figure 4. Xps Timer/Counter Detailed Block Diagram

The PWM period is determined by the generate value in Timer0's load register (TLR0) and the PWM high time is determined by the generate value in Timer1's load register (TLR1). The period and duty cycle(high time) are calculated as follows:

When counters are configured to count down and used :
PWM_PERIOD = (TLR0 + 2) x PLB_CLOCK_PERIOD
PWM_HIGH_TIME = (TLR1 + 2) x PLB_CLOCK_PERIOD

When counters are configured to count up:
PWM_PERIOD = (MAX_COUNT - TL R0 + 2) x PLB_CLOCK_PERIOD
PWM_HIGH_TIME = (MAX_COUNT - TLR1 + 2) x PLB_CLOCK_PERIOD
Where
PLB_CLOCK_PERIOD is the Processor Local Bus _CLOCK_PERIOD

MAX_COUNT is the maximum count value for the counter, such as0xFFFFFFFF for a 32-bit counter.
(TLR0 and TLR1) timer/counter load register is the timer/counter either timer 0 or timer 1 and this register is 32 bit. the required value loaded through this register.

Figure(5) shows the flow chart of the PWM is used.

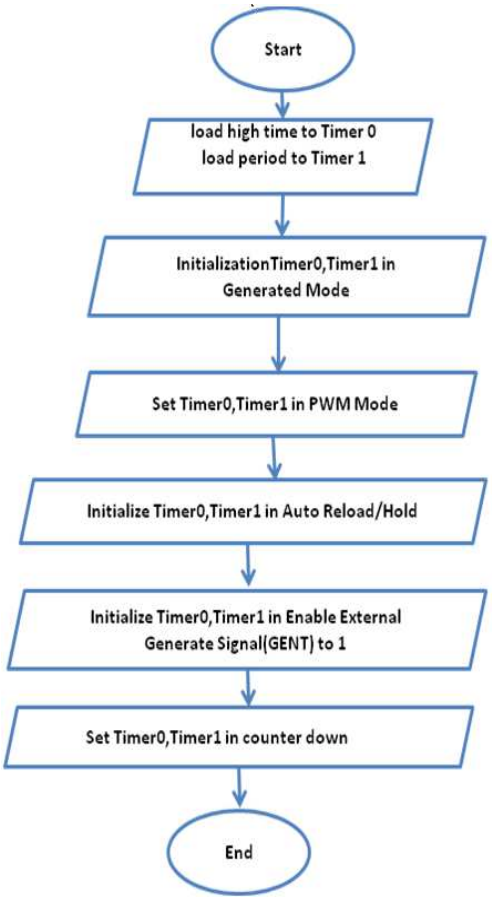

Figure 5. Flow Chart Of PWM

3. RESULTS

The platform studio in which the hardware part is developed issues a block diagram of the designed processor system as shown in Figure 6, as well as the address map of the system as shown in Figure 7.

Figure 8 shows the resultant PWM wave for different values of duty cycles (a=10%),(b=20%), (c=50%), (d=75%) displayed on the chip scope analyzer window . The samples were gathered through write phase of the PLB. It is noticed that the part of the wave whose value(1) (on case) increased with increasing the value of Timer 0 load

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register ; therefore the system behaves as a PWM system. Figure (9) shows the resultant PWM waves for different duty cycles (a=10%),(b=20%), (c=50%), (d=75%) displayed on oscilloscope .

The comparison between the two results obtained by chip scope analyzer and the oscilloscope shows that the percentage error is less than. 1% .

5. CONCLUSION

A pulse width modulation system with different duty cycle is designed and configured on FPGAs slice of type Spartan 3E using Embedded Design Techniques which present a flexible ,easy and trustable methodology to design different kind of systems as it facilitates a processor system configuration on FPGAs. The configured system can be programmed to act according to the target of the system. The maximum frequency that can be operated on is 100 mHZ , due to the limitation of the clock generator the used board. The duty cycle range is between (5%_95%) .

FPGA slice with 64 bit timers may be used in the future work to extend the range of the duty cycles.

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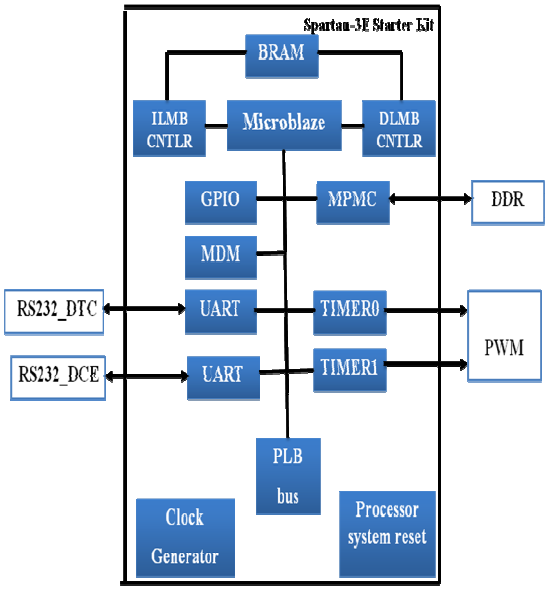


Figure 2. The block diagram of the hardware part of the designed system

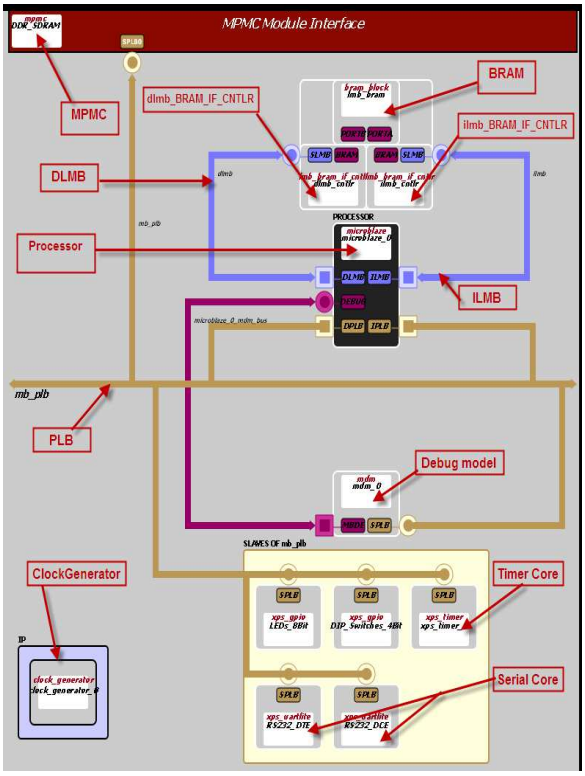
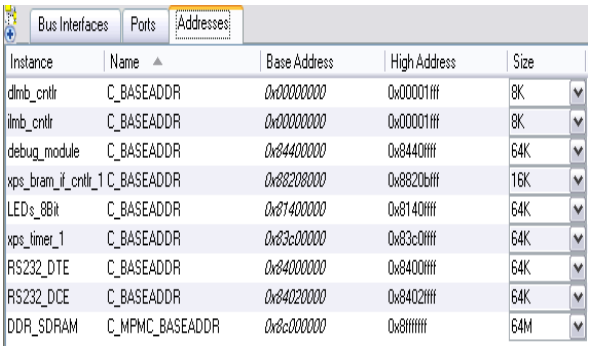
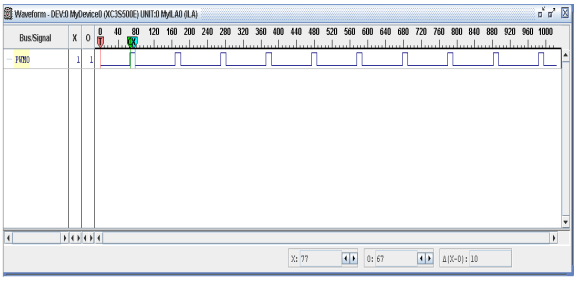


Figure 6. The resultant block diagram of hardware issued by the platform studio

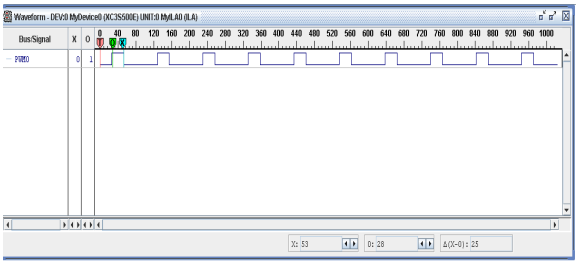


Instance	Name	Base Address	High Address	Size
dlmb_cntlr	C_BASEADDR	0x00000000	0x00001fff	8K
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001fff	8K
debug_module	C_BASEADDR	0x84400000	0x8440ffff	64K
xps_bram_if_cntlr_1	C_BASEADDR	0x88208000	0x8820bfff	16K
LEDs_8Bit	C_BASEADDR	0x81400000	0x8140ffff	64K
xps_timer_1	C_BASEADDR	0x83c00000	0x83c0ffff	64K
RS232_DTE	C_BASEADDR	0x84000000	0x8400ffff	64K
RS232_DCE	C_BASEADDR	0x84020000	0x8402ffff	64K
DDR_SDRAM	C_MPMC_BASEADDR	0x8c000000	0x8fffffff	64M

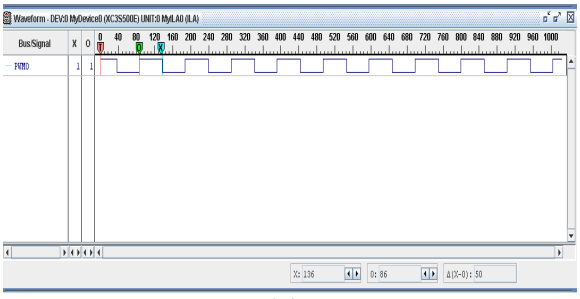
Figure 7. The address map of the designed system components



(a)



(b)



(c)

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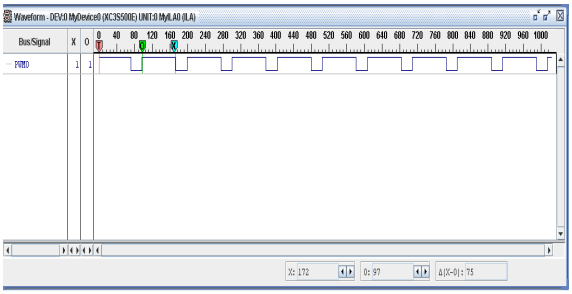
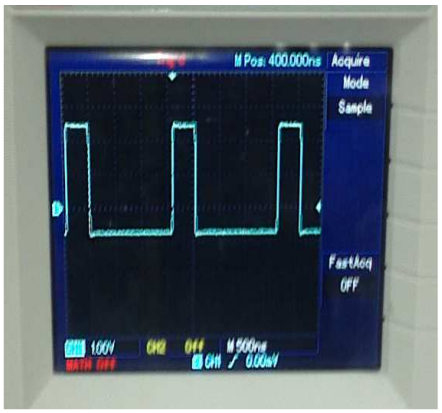
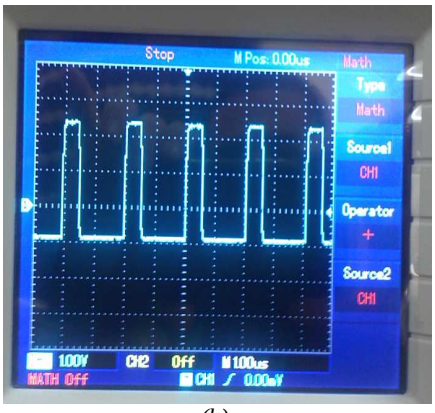


(d)

Figure 8. output of the designed PWM for different values of duty cycle on the chip scope analyzer window



(a)



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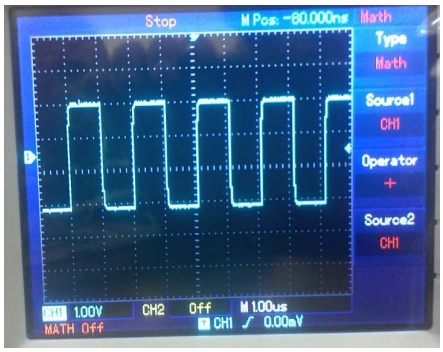

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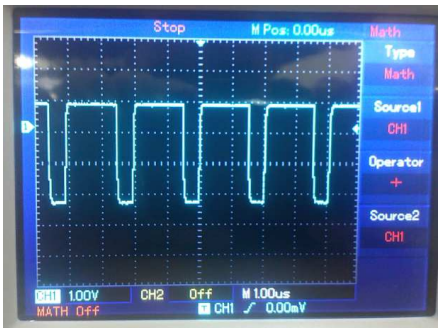

(d)

Figure 9. output of the designed PWM for different values of duty cycle on the oscilloscope.

Appendix A
Symbols

Symbol	Description
Capture Trig	Capture Trigger
TLR	Timer Load Register
TCR	Timer Counter Register
TCSR	Timer Control Status Register
PWM0	Pulse Width Modulation output
Generate Out	Generate Output