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THE DESIGN OF DIGITAL FREQUENCY SYNTHESIZER BASED ON VHDL

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ABSTRACT

Direct digital frequency synthesizer (DSS) was proposed by Tiemey at 1971 and this frequency synthesis technique soon came to the attention of people because of its good frequency resolution and fast frequency performance. Now, it is extensively used in telecommunication and electronic machine region and it is a key technology to realize full digitalization. This text introduces the principle and characteristics of DSS and gives the method of implementing DDS using VHDL. The design proposal touches on MAX+PLUS II platform. By this way, we can make the Chip products instead of multiple chip board products, so as to reduce power consumption, improve reliability, and also can be easily to design on line modification.

Key words: *Digital Frequency Synthesizer, (DSS), VHDL, MAX+PLUS II platform*

With the progress of science and technology, the traditional signal source frequency which has bad stability, slow frequency conversion speed and lower accuracy can not meet the actual needs. So, it is necessary to develop a new signal source. In recent years, due to the progress of microelectronics technology, direct digital frequency synthesis technology got rapid development. And it is widely used in radar, digital communications and electronic warfare and other fields because of its high frequency resolution, frequency conversion speed, output signal with continuous phase and full digitization architecture.

1. DSS PRINCIPLE

DSS is a frequency synthesis technology which gets the desired waveform directly from the concept of the phase. A DSS is composed by frequency control register, high speed phase accumulator and sine look-up table. In the figure 1, frequency control word controls the frequency of DDS output sine wave and phase control word controls the phase of DDS output sine wave. Phase accumulator is the core of the DDS system; it is composed with an accumulator and an N- phase register. When a clock pulse comes, the phase register increases by step K. Counting up the output of the phase register and the phase control word, the result will be the address of sine look-up table. Sine look-up table is composed by ROM which has digital amplitude information of full cycle sine wave. The address of each look-up table corresponds to a phase point from degree 0 to degree 360. The lookup table could map into digital amplitude signal of sine and cosine wave from input address information. At the same time, the result will be inputted into the digital-to-analog converter, through a low pass filter, and then we can get a pure spectrum sine wave.

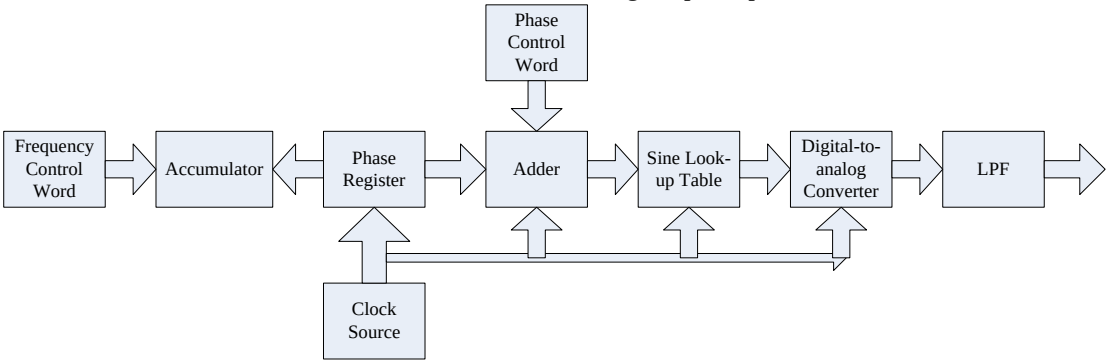

Figure 1. The Graph Of Dss Working Principle

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2. THE DESIGN AND IMPLEMENTATION OF DSS BASED ON FPGA

According to figure 2, supposing the phase control word is 0, then the FPGA design of the phase accumulator which is the core part of DDS can be divided into the following several modules: Phase accumulator SUM99, phase register REG1, Sine look-up table ROM and Output register REG2.The internal block diagram is shown in the figure 2.In the figure, input signal contains clock signal CLK, enable signal EN, reset signal RESET, frequency control word K and output signal Q.

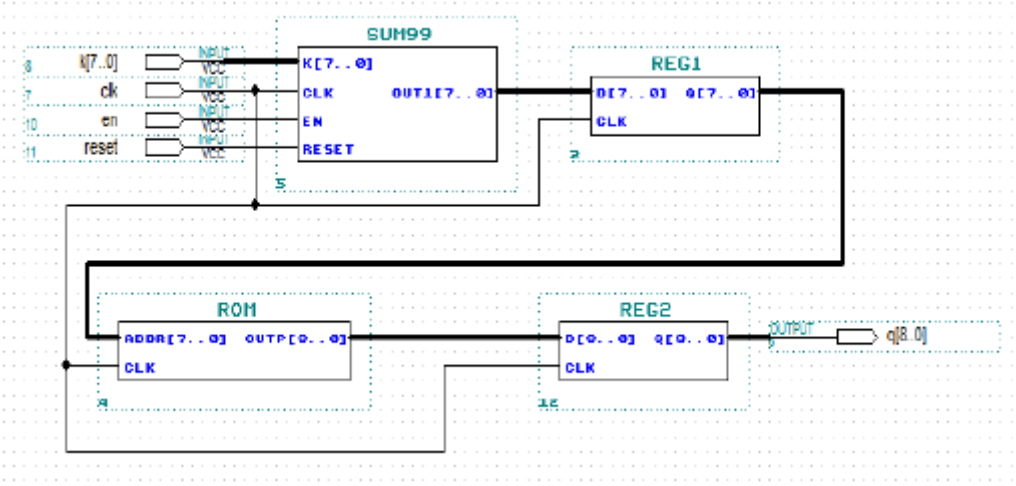

Figure 2. The Figure Of Dss Integral Assembly

The whole DDS module uses a clock signal. So the operation speed of each module keeps synchronization. The phase accumulator SUM99 is a 10 bit adder with accumulation function. It does additive operation with 10 bit frequency control word K as compensation. When it is full, the counter will be clear, and the rerun. The phase register REG1 is a general 10 bit register, The input data will be registered here, when the next clock comes, the register data output. The sine look-up table is the most critical part of the DDS. We sampling sine function firstly, then the sampling results will be put into the corresponding storage unit in the ROM module. Every address corresponds to a numerical value, the output is 9 bits. In order to ensure the stability of output data, the ROM output data is sent into REG2, when the next clock comes, the value will be output. The whole system is a module which works under control of the synchronized clock signal CLK.

3. PROGRAM IMPLEMENTATION OF DSS

K is frequency control word, CLK is clock signal, EN is enable signal, and RESET is reset signal. When RESET is high level, the accumulator will be clear. When the RESET is 0 and EN is high level, the system operates in CLK frequency. As matter of fact, the clock speed directly reflects the working speed of the system; it shows the superiority of FPGA speed. Accumulator will increase K when a clock pulse comes. Because the attribute of the pin OUT1 is OUT, so it cannot be used as assignment source. It can only be assigned, so we define the signal TEMP to realize this function.

In order to guarantee the stability of the output data, the output data of SUM99 is put into the address port of the ROM after the function of latch. From the following procedure, we can know that the essence of the latch is a multi digit D trigger. In VHDL, we get the trigger through introduced through the incomplete conditional statement. The input address and the output data are binary number; this function is realized through the function “dec2bin” in the MATLAB. The input address and the output data can be converted into binary number by the following program:

The ten - binary conversion of address:

```
x=1:1024;
y=dec2bin(x)
```

The ten - binary conversion of output data:

```
T=2*pi/1024;
t= [0: T: 2*pi];
y=255*sin (t);
z=round(y);
dec2bin (z);
```

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this instruction dec2bin(x) requires that input data is a non-negative integer, when we samples the second half of the sine week, we can first sample its absolute value, and then add the sign bit.

4. THE SIMULATION RESULTS OF EACH MODULE

4.1 The Simulation Of Phase Accumulator SUM99

(1)The waveform simulation results

The software simulation of phase accumulator is as follows: When the reset port is effective, the accumulator will be clear. When the reset port is invalid, and enable port is high level, the phase accumulator will increase in pace K. We Simulate with K value of 36, so that the output value will be grow with step 36. The operational results will be stored temporarily in signal TEMP. The above simulation results show the integrity of the phase accumulator function. The output of the phase accumulator connects to the input of the register REG1.

Figure 3.The Simulation Waveform Of Sum99.Vdh

From the figure 3, we can see that when the internal pin of TEMP increases with K as the step size, the output port OUT1 also increases with K as the step size, so the accumulation function is realized.

If we amplify the simulation wave, we can see that a little time delay between the rising edge of CLK and the signal out when it rises from 0 to 1.We can look through the time delay through timing analyzer in MAX+PLUS II. It likes figure 4:

(2) The simulation of the delay analysis

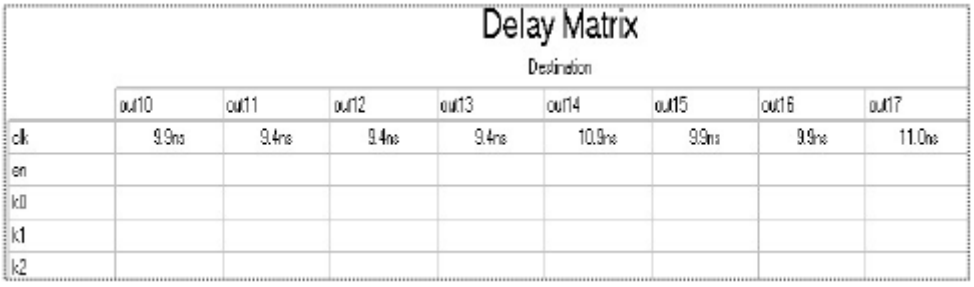

Figure 4: The Delay Analysis Of Sum99.Vdh

4.2 The Simulation Of Sine Look-Up Table ROM

(1)The waveform simulation results

A sine look-up table is stored in the ROM, when a pulse comes, the port ADDR will increase 10 when simulation. The simulation results show in figure 5. Along with the address input increase, the output grows according to sine wave numerical. The simulation results show that the value which is stored in ROM is a sine wave.

(2) The simulation of the delay analysis

As shown in Figure 6, the output of sine look-up table delays around 9ns compared with the input. And it is substantially similar to the figure 4, which meets the system coordination of every part.

4.3 The Simulation Results Analysis Of The Whole System

(1) The simulation waveform of the entire DDS system

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Figure 5: The Simulation Waveform Of Rom.Vdh

Figure 6: The Delay Analysis Of Rom.Vdh

Firstly, we generate symbols from every partial component, and then assemble into DDS.VHD. Its simulation results are shown in Figure 7, in this DDS simulation waveform, it contains the entire assembly pin signal. The frequency control words are set to 7F, the internal signal TEMP also grows with 7F step, the result is registered to latch REG1, and the output of the latch is regarded as address input signal of the sine look-up table ROM. Then a sine wave series will be output. In order to ensure the stability of the output data, the result is output through REG2. The entire system has minimal delay compared input with output.

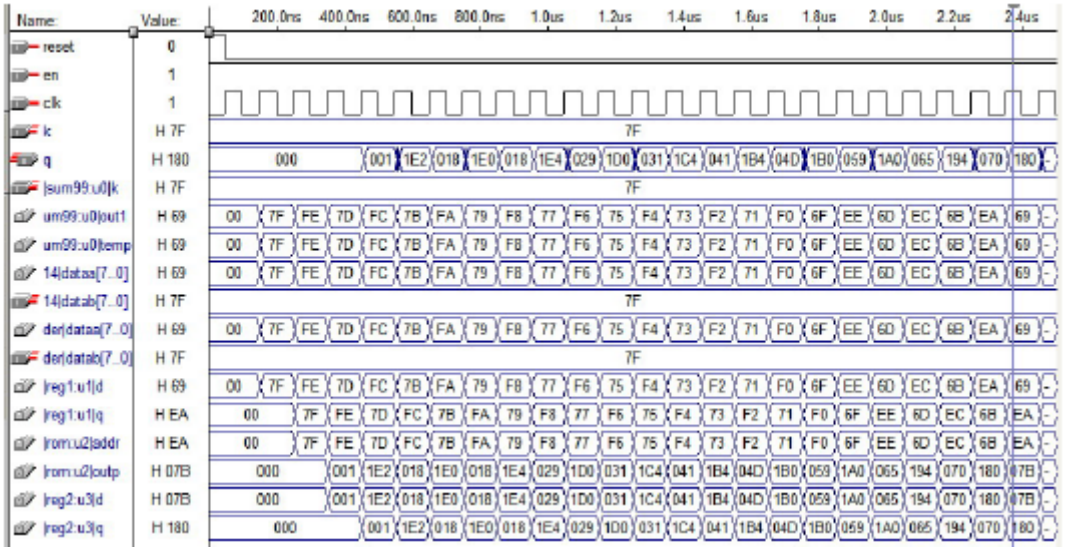

Figure 7: The Simulation Waveform Of Dss.Vdh

(2)The time delay characteristics analysis of the entire DDS system

As shown in Figure 8, the whole system works with the same clock CLK under the action of coordination. The delay matrix reflects the output Q input clock delay is about 7ns.And the delay time of each component is approached each other. This also reflects high performance of the FPGA devices.

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Figure 8: The Delay Analysis Of Dss.Vdh

5. CONCLUSIONS

Along with the circuit scale enlarges constantly in the electronic systems, the circuit complexity is also growing, therefore, the traditional electronic system design method has been far from the development of modern electronic technology and requirements, the more advanced, more fast and powerful EDA tools is urgent needed. The simulation in this text proposed a method to make digital Frequency Synthesizer Based on VHDL, and the results show that its performance has reached the expected requirements.

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