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DESIGN AND HARDWARE PLATFORM REALIZATION OF UM-BUS TEST SYSTEM

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ABSTRACT

This article is based on the UM-BUS which is a high-speed dynamic reconfigurable serial Bus, design the test system and completion hardware platform. The test system uses un-filter monitor function to complete the data collection in the case does not affect the transmission characteristics of the bus, according to bus protocol specially designed fault injection mechanism improved the testing of the failure mode; at last through the PCI-E and USB3.0 realize the high-speed transmission with computer.UM-BUS bus terminal transceiver function can be done on the basis of the test tasks according to the needs of the design of the test board. In addition, the design also comes with a storage function, the overall data acquisition and storage process in the case of without relying on computer.

Keywords: *UM-BUS, Test system, FPGA, PCI-E, USB3.0, DDR2*

1. INTRODUCTION

With embedded systems developed and widely used in the national economy, aerospace, military, industrial control, transportation and other fields, increasing the requirements high reliability and fail-safe in embedded systems. Typically dealing with it by redundant, UM-BUS is a high-speed computer internal bus with the highly reliable capabilities of failure self-healing. The concurrent of redundant channel increase the transfer rate of the bus, while the concurrent channel taking advantage of dynamic reconfiguration to improve the fault tolerance of the bus when the system fails, it is able to quickly detect the fault lines and location them.

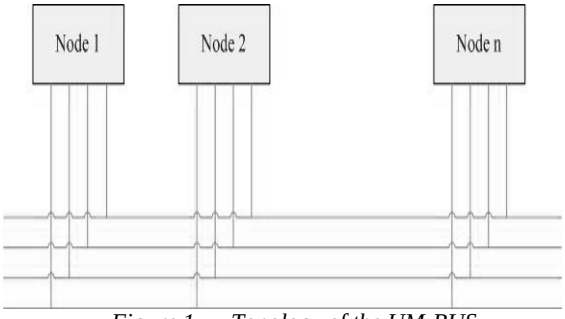

Figure 1. Topology of the UM-BUS

To guarantee the high reliability of the bus system, bus testing is essential. UM-BUS test system information processing board is critical hardware on the test, which is used to complete bus information integrated, resource sharing, data processing, task coordination, and fault-tolerant reconfigurable. There are two ways in the traditional bus test: First, test and diagnostic the subsystems through the various of test interface and partly acquisition data from the installation of the sensor directly in the underlying; second is directly through an integrated electronic system get the data, the test system intervention through the coupler to the integrated electronic system, then it can read the bus data directly from the various subsystems. However, these methods on record of the data transfer process between the bus and the capacity for failure reproduction and analytical processing capacity is weak; what's more, these methods are not perfect for fault injection, the fault injection testing on devices cannot be done. Although the above-mentioned test methods widely around test platform application, but they are not flexible fault injection capabilities makes the most of the bus test is still get rid of the pattern, that is the input the drives then test output responses, cannot be a positive test. Be bus test results verify actual bus run a variety of state, as well as changes in the environment, when the actual abnormal excitation or abnormal response, in particular, many of which are not easy to reproduce the failure appears cause a lot of troubles. In this paper, design a new test program based on UM-BUS which can improve the test coverage and implementation the hardware platform.

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2. THE DESIGN OF BUS TEST SYSTEM

Based on SOC test technology, satisfaction test demand for UM-Bus, the system design a FPGA platform. The main functions the platform contains affairs library, Bus task library and test stimulus generation functional modeling part. Its core is lead the concept of transaction into the verification process, abstract the pin level to a specified high level, which can effectively support the development and reuse of the test platform. The establishment of the bus task library treat measured bus object to complete the description of the basic functions of abstraction and sequential logic. Completion of the test on the SOC bus timing stage data acquisition, by the output detection module will transfer data to the computer or the CF card to prepare the further analysis of the data by a bus function model.

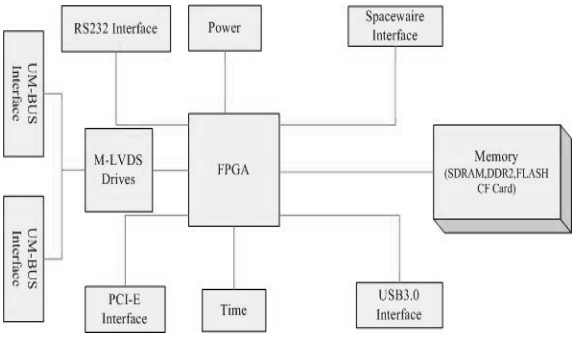

Figure 2. Schematic of the Test Board

The system can real-time acquisition, processing, monitoring and recording bus signals on UM-BUS, assist in the completion of post-hoc analysis and laboratory UM-BUS bus data signal simulation, speed up bus error positioning, shorten the data processing cycle, reduce the number of experiments and experimental costs. Overall system functions can be divided into three parts:

A. Un-filter Monitor Function Design

First, the system can be used as un-filter monitor of the UM-BUS system, collect information between the transmitting and receiving end. Un-filter monitor including the meaning of two levels: first, to read all the data passing the UM-BUS which is not directed against one or several terminal devices, nor for one or several bus command, but including all types of commands and responses to the commands; Secondly, the transmission data on the bus, due to various factors, not only have the correct line UM-BUS transfer predetermined data, including some does not comply with the provisions transfer data, which is considered erroneous data, un-filter the other hand, refers to, regardless of the data is correct or not, the system will have the data processing and storage.

The FPGA function module into the signal converter when the system operates in this mode, the data on the UM-BUS driven by M_LVDS for data processing in the FPGA, and finally transfer the processed data to the PC for storage or stored directly order to meet the needs of the UM-BUS communication of high-speed test the system to select the two high-speed communication bus that is, PCI-E and USB3.0 interface design can be connected with the computer to be able to complete a large number of high-speed data when transmission. To be able to make the test system can meet the need of some special test without computer, acquisition and storage data to the CF card.

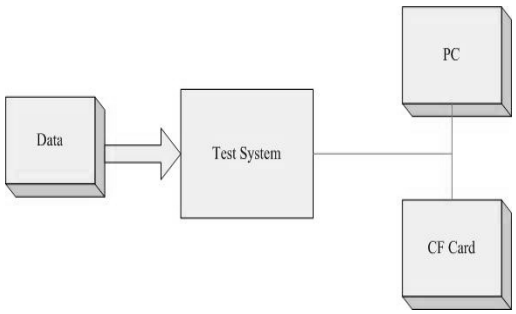

Figure 3. Schematic of the Un-filter Function

B. Multifunctional Design

The board can be completed the receive and send terminal function at the same time, that is, at the same time to achieve a combination of bus terminal and test the data acquisition system, the completion of the bus filter data acquisition system front-end functionality.

When the system work in this module, the hardware settings each terminal has its own unique terminal ID and Synchronous transmission of real-time access to the UM-BUS network, transmission real-time data of on the bus controller and the receiving end to no filter receiver module synchronization.

C. Fault Injection Mechanism

The platform can be used as the UM-BUS test system fault generation module. According to dynamically reconfigurable high reliability for UM-BUS, how we can better achieve fault injection will be a huge challenge. The system is directly connected in series to the bus system between the receiving and transmitting terminal does not interfere with the actual communication, which can

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be realized in accordance with the predetermined program fault injection function, verify the compliance of the UM-BUS for completion of the specific fault responses with intended design.

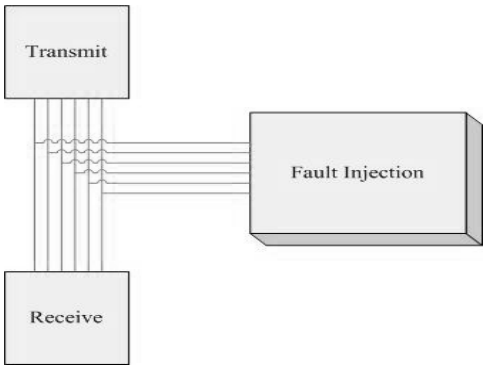

Figure 4. Schematic of theFault Injection Function

3. HARDWARE PLATFORM DESIGN

The hardware platform design includes mainly includes three parts, the first is the selection and design of the master power supply, which can supply for the entire test system and be able to meet the requirements of each system module voltage conversion; secondly, the design of the storage section, take into account the real-time processing of large amounts of data but also storage these data directly, cache design is required to complete the intermediate data buffer; Finally the board interfaces which are able to complete a variety of different needs and supporting with kinds of interface circuits, so you can make the test board to multifunction.

A. Master Power Supply Design

The system adopts FPGA as the core of the master, so that will be able to easily meet the conversion of a variety of different functions of the plate can be achieved through different programs download. Selected Xilinx Inc. Virtex-5family, this series chip design using the 65 nm lithography node. The reasons for the choose the series chips are that they can provide high-speed real-time computing and a large number of IO connections, while the chips are also able to provide the hard core of the PCI-E support behind the interface design interface circuit, so the afterwards design will gain a great help. More due to the system design to chip interface circuit, two power supply design program. First, by the PCI-E 12V power by the multi-level transformation converts power a variety of needs; second, direct external 12V DC power supply to the desired voltage conversion circuit transformation. This will not only meet the plate and connected to the PC, the power supply can be out of work when the PC at the same time be able to select the external power supply.

B. Storage Design

To be taken into account the work of the system may have to deal with a large number of real-time data streams, selected three memory chips are two Flash chips, two SDRAM chips, two DDR2 chips. By the progressively large capacity cache and Ping-Pong switching operation to achieve real-time communication of the data stream. These memory chips are connected directly to the FPGA, FPGA to control the workflow of each chip. Two 1Gbits DDR2 chip using a separate address, control and data busses, and support the use of the Ping-Pong down the data transfer mode. Why two DDR2 chips? Be considered compatible with the Ping-Pong down the data transfer mode, data input and output can support large cache at the same time, so you can play the USB3.0 transfer speed to the extreme, to meet a variety of data transmission needs. In order to respond to the needs of the special circumstances, the system can also achieve the realization of self-storage function, so I chose the faster CF card with the above cache to achieve real-time acquisition of data storage capabilities.

C. Interface design

1） UM-BUS Interface:In order to fulfillment UM-BUS bus tandem relationship and be able to run the UM-BUS terminal function. The plate on the set of two 32 the UM-BUS interfaces, so that you can meet the multi-channel data to send, receive, and simultaneous transmission and reception functions. The operating mode is as follows:

First the board as receiving or transmitting terminal operating mode, drive through the M-LVDS connection, FPGA and UM-BUS interface circuits connected to the bus network terminal. Second, because of the two UM-BUS interfaces board can be simultaneously performed transmission and reception of the communication task, the main purpose can be completed as follows fault injection and un-filtering of the communication function of the data acquisition, the formation of UM-BUS test system bus the network structure of the communication part.

2） PCI-E and USB3.0 Interface:PCI Express uses serial connection characteristics can easily improve the speed of data transmission to a very high frequency, reaching far beyond the transfer rate of the PCI bus. PCI-Express connections can be configured as x4 data bandwidth with each

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channel transfer rate of 2.5Gb/S. The hard-core embedded PCI-Express Endpoint Block the Xilinx the company's Virtex5 Series FPGA chip, which offers the possibility to configure the PCI-Express bus solutions for the realization of monolithic. This article uses Virtex5-LX85T FPGA chip design PCI-Express interface hardware circuit, PCI-Express data transfer.USB3.0 also known as super speed data bus, its transmission speed can reach 5Gbps bandwidth up to 600MB / S. USB3.0 chip chose Cypress Company the FX3 series CYUSB3014-BZXI chip, and the interface complies with USB3.0 specification. The lines between the FPGA and USB3.0 chip and FPGA with external IO with equilong design to ensure reliable transmission of high-speed signals.

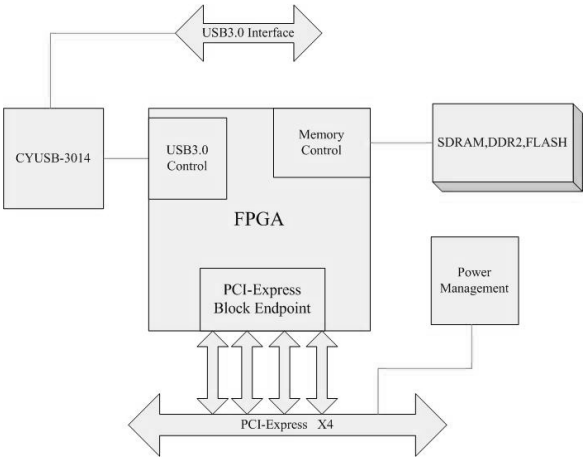

Figure 5. Schematic of thePCI-E and USB3.0 Interface

D. PCB design

The Printed Circuit Board (PCB) as the carrier and the signal of the electronic device and data transmission medium, the station has an important position in the vast majority of electronic products. The logical structure is correct, compact and ideal for high-speed signal transmission function of the PCB prototype electronic products and validation testing completed quality and speed have played a very important role. Mentor EE tools, which is Mentor Graphics introduced advanced PCB design tools based on the Windows interface, identified cable smooth software by engineers, it contains a very powerful automatic routing tool Expedition, which is a very professional wiring rules, known as the best route tools. DxDesigner (ViewDraw the upgrade version) introduced by Mentor Graphics schematic entry tool, its powerful, user-friendly, can support a variety of PCB Layout tools. The design uses the Mentor software DxDesginer and Expedition complete schematic and PCB layout.

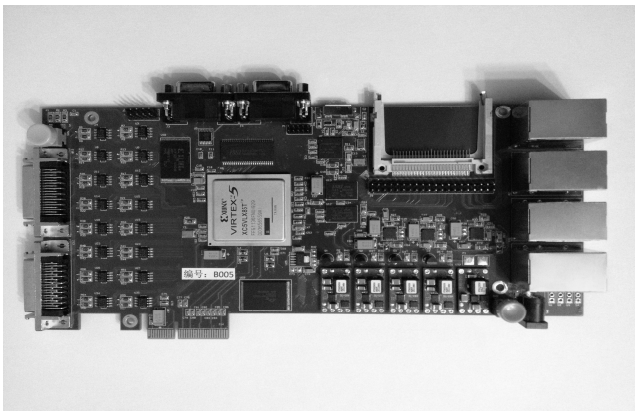

Figure 6. Layout of the PCB Design

Using signal integrity tool analysis the board after the layout is necessary to ensure the integrity of the signal, and shorten the design cycle. Adopt the Mentor company Hyperlynx7.1 simulation software wiring simulation tools of this article, the following figure shows the signal waveform of the board UM-BUS differential signal lines, proven to meet the communication requirements of the signal.

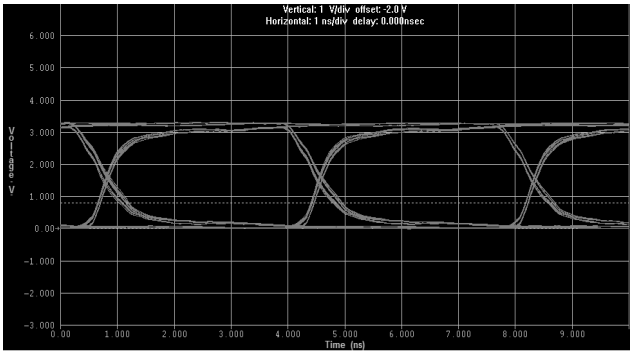

Figure 7. Waveform of Differential Signal

4. CONCLUTION

In this paper, design abus test system to the high speed dynamically reconfigurable serial bus, which are able to complete the high-speed data transmissionand real-time storage, fault injection, and to be able to as the bus data transmission, receiving and data collection terminalsat the same time. Completed by Mentor Graphics' high-end PCB design software EE development. Simulation by Hyperlynx for high-speed signal lines, designed to achieve the scheduled communication design requirements. This paper analyzes the structure of the entire UM-BUS test system design and complete hardware platform. These works will have a guiding significance for the completion of the entire test system and high-speed bus test systems engineering practice.

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