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IMPLEMENTATION OF A BRUSHLESS DC MOTOR AS A VIRTUAL MOTOR

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ABSTRACT

Due to their simple structure, high efficiency, fast dynamic response, Permanent Magnet Brushless DC (PMBLDC) machines are extensively used in automation, consumer electronics, electric vehicles and medical and industrial applications. Availability of these high energy density permanent magnet materials enhances the performance of PMBLDC motor drive and also reduces the size and losses in these machines. Depending on the application the controllers need to be tested, for which motors of various ratings are required. Utilizing real motors of different sizes and capacities for development and testing is difficult and mundane. If the functionality of the motor can be rendered by a system on a chip, it will reduce the development time. Hence, the development of a virtual BLDC motor is considered in this paper. A model of the BLDC motor is simulated, and its characteristics are implemented on a FPGA. It allows the realization of motors of various ratings to be tested by changing the parameters. This system functions as time and energy efficient solution for the testing and validation with out any risk of damage to motor or controller under test.

Keywords: *System on Chip (SoC), BLDC, FPGA, Virtual Motor, Controller Validation*

1. INTRODUCTION

Electric drives are employed in applications in which a wide range in speed and torque control for the electric motor is desired. BLDC motors are safe, superior to the synchronous motors and induction motors in their speed torque characteristics and dynamic response. A field-programmable gate array (FPGA) uses an array of logic blocks, which can be programmed by user. It provides a platform for interfacing custom hardware and complex software in systems-on-chip (SoC). Though the BLDC control system can be implemented with devices such as programmable logic devices and Digital Signal Controllers these do not offer total flexibility for custom hardware development. Hence, an FPGA is preferred. Affirming the hardware capabilities of FPGA, it is relatively easy to implement myriad control systems and validate the control algorithms with the help of simulation tools and models.

BLDC motors are a type of synchronous motors: the magnetic field generated by the stator and the magnetic field generated by the rotor rotate at the same frequency. Three phase BLDC motors are the most widely used. Depending on the interconnection of the coils in the stator windings the BLDC motor is constructed in two ways: the one which gives back electromotive force (EMF) as trapezoidal and the other sinusoidal. For a three-phase BLDC motor with trapezoidal flux distribution the back emf waveform is as shown in Figure 1.

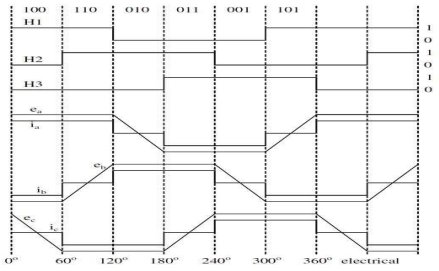

Figure 1. Three Phase Trapezoidal Back EMF With Current

The back EMF induced per phase of the motor winding is constant for 120° and changes linearly with rotor angle before and after the constant part.

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An introduction to BLDC motor is presented in this section. The previous research work carried out is reviewed in section 2 and the dynamic model of the BLDC motor is outlined in section 3. Section 4 deals with the concepts of virtual motor being modelled and section 5 explains the simulation of virtual BLDC motor using Verilog and its implementation using the Spartan 3E with results. Hardware implementation is presented in section 6 with the results obtained experimentally along with the conclusions.

2. PREVIOUS RESEARCH

The present day research is mainly based on motor drives and controllers for PMBLDC. State-of-the-art of FPGA technologies and their contribution to industrial control applications are reviewed [1]. The use of FPGAs to implement artificial intelligence based industrial controllers is reviewed. The controller is based on the extended Kalman filter. Dufour, C., et al. presented the results of closed-loop control experiments using a virtual PMSM drive implemented on a FPGA card connected to an external controller [2].

The FPGA-based permanent magnet synchronous motor (PMSM) motor drive is implemented on an eDRIVEsim simulator, based on the RT-LAB platform. The FPGA-based motor model is designed with Xilinx System Generator blockset with no HDL hand coding. The pulse width modulation (PWM) controller is designed using rapid control prototyping methodology, based on Simulink. It is implemented on a separate RT-LAB system using standard Opal-RT FPGA-based I/O cards for analog input capture and PWM generation. The design by Bogdan Alecsa and Alexandru Onea describes a method to implement a digital BLDC motor speed controller inside an FPGA device [3]. The controller design is a classical proportional and Integral (PI) type implemented using System Generator and Simulink.

Jiang, S.; Liang, J.; Liu, Y.; Yamazaki, K.; Fujishima, M. presented the modelling and co simulation method of a FPGA based PMSM control system; the current control is based on Space Vector PWM. The function model is built in Matlab environment, and the behavioural model (VHDL model) is programmed in the synthesis software platform. The co-simulation between function model and VHDL model is implemented by integrating two models into one co-simulation model, the hardware timing and the function simulation can be tested and verified at the same time [4]. Design by Jiancheng Fang, Xinxiu Zhou, and Gang Liu propose a novel way to control the torque ripple in small inductance motors [5]. Research on modeling IGBT based voltage source converter to represent the non-linear device switching characteristics has been presented by Aung Myaing and Venkata Dinavahi [6].

The design by Christian Dufour, Jean Bélanger, Simon Abourida, Vincent Lapointe presents real-time simulator of a PMSM drive based on a finite-element analysis (FEA) method and implemented on an FPGA card for HIL testing of motor drive controllers [7]. A recent work by Oleg Vodyakho, Mischa, Chris S. Edrington and Fletcher Fleming implements induction machine emulator platform that utilizes the power hardware-in-the-loop concept in conjunction with a high fidelity machine model and load dynamics [8]. The electrical machine and its load dynamics are simulated with a real-time digital simulator, which generates appropriate control commands to a power electronics-based voltage amplifier that interfaces to a variable speed drive. But this design includes a transformer for isolation purposes which makes the entire system bulky and is targeted for power convert circuits.

Yu Xiaobo and Li Xiao Gao Yong, based their method for motor control using the back emf as a sensor-less BLDC motor [9]. Pragasen Pillay and Ramu Krishnan discussed about the modelling, simulation, and analysis of PMBLDC motor [10]. Anand Sathyan et al discussed about a digital control scheme for BLDC motor drives in domestic applications [11]. A simple novel digital PWM control has been implemented using FPGA for a trapezoidal BLDC motor drive system. P. Kumar and P. Bauer developed an analytical model for determining instantaneous air-gap field density of a PMBLDC motor [12]. This instantaneous field distribution can be further used to determine the cogging torque, induced back electromotive force, and iron losses in the motor.

Ming-Fa Tsai, Tran Phu Quy, Bo-Feng Wu, and Chung-Shi Tseng, discussed modelling using Matlab / Simulink and control of a BLDC motor using FPGA, to evaluate the performance of the motor with various control schemes [13]. The control and PWM-generation logic block were developed and transferred to digital hardware circuit in VHDL hardware description language for co-simulation verification with ModelSim environment. Dagbagi, M. and Idkhajine, L. presented a framework for the use of FPGA based motor modeling when the state-space approach is used [14]. Computations are performed in floating-

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point using commercially available arithmetic cores.

Hao Chen, Song Sun, Aliprantis, D.C. and Zambreno, J. presented the implementation of an induction machine dynamic simulation on a FPGA board [15]. Using FPGAs as computational engines can lead to significant simulation speed gains when compared to a typical personal computer, especially when operations can be efficiently parallelized on the board. Monmasson, E.; et al. presented the benefits of using FPGAs in the case of complex control applications with a sensorless motor controller [16]. This controller is based on the extended Kalman filter. Duman, E. Can and H. Akin, E., carried out an implementation of an induction machine model in real time using the FPGA [17]. Honghao Guo, Bo Zhou, Jichen Li, Fangshun Cheng and Le Zhang, used RT-LAB for modelling BLDC-based wind turbine emulator [18]. Real-time simulation is made possible with such a sophisticated hardware and software.

Metin Demirtas and Aslan Deniz Karaoglan, discussed a tuning and optimization of PI parameters for DSP-based BLDC motor drive [19]. This paper proposes response surface methodology (RSM) for tuning Proportional Integral (PI) coefficients for a PMBLDC motor drive. Motion Control Kit (MCK243) is used to carry out digital motion control applications. Milivojevic, N. et al, discussed digital pulse width modulation control for a BLDC drive in both motoring and generating modes of operation [20]. This control strategy requires no current sensors and can be implemented on a FPGA. This paper investigates potential stability issues due to the simplicity of this control under various conditions of load disturbances and also owing to the reduction in processor capability.

Most of the above works are carried out using sophisticated hardware and proprietary software like RT-Lab etc. In this paper, virtual motor implementation on an FPGA module is dealt with by modeling the PMBLDC motor characteristics in a simple manner. The motor characteristics, hall sensors, inverter module are all modeled on a single chip, thus saving space and aid in easy interfacing and validation of external motor controllers. This virtual motor could be used during the design stage of digital controllers for BLDC motor as a codesign and co-verification tool.

3. MODEL OF THE BLDC MOTOR

For coming out with a virtual BLDC motor the dynamics of the motor are to be well understood. Mathematical model is required for its simulation and realization. S.P. Natarajan, C. Chellamuthu and K. Giridharan had developed a model for the BLDC motor using the equivalent circuit of the motor consisting of a resistance, inductance and the back emf of each phase [21]. Various models of BLDC motors are presented in [22]. Basic circuit analysis was used to find the per-phase voltage thereby attaining the electrical equations for a BLDC machine as given in (1) to (6). The model developed in Matlab / Simulink is controlled by PI and intelligent controllers and the comparison was presented.

$$\frac{di_x}{dt} = \frac{\left(v_x - e_x - i_x * R\right)}{L} \quad (1)$$

$$\frac{di_y}{dt} = \frac{\left(v_y - e_y - i_y * R\right)}{L} \quad (2)$$

$$\frac{di_z}{dt} = \frac{\left(v_z - e_z - i_z * R\right)}{L} \quad (3)$$

$$\frac{d\omega}{dt} = \frac{\left(T_m - T_l - B * \omega\right)}{L} \quad (4)$$

$$\frac{d\theta}{dt} = \omega \quad (5)$$

where ω is the rotor speed and θ is the rotor position, v_x, v_y, v_z are the phase voltages, i_x, i_y, i_z are the phase currents, e_x, e_y, e_z are the phase back-EMF voltages, R is the phase resistance, L is the synchronous inductance per phase and includes both leakage and armature reaction inductances. The electromagnetic torque T_e, is given by

$$T_e = \frac{\left(e_x i_x + e_y i_y + e_z i_z\right)}{\omega} \quad (6)$$

4. VIRTUAL BLDC MOTOR

A virtual BLDC motor model was developed using a microcontroller and basic characteristics of the motor was presented [23]. The virtual motor mimics behavior of the real motor in its characteristics. The hall sensor output from the virtual motor is fed back to the motor controller's commutation block, which gives appropriate gating signals to the inverter switches. The motor model

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was further developed using a FPGA based model in which Euler method is used to solve the differential equations to give the motor characteristics [24].

In the present work the virtual motor is improved by using the modified Euler's method to solve the differential equations. The virtual motor takes the three terminal voltages from the inverter as the input. The load torque is also given as another input to the virtual motor. The various modules of the virtual motor generate, the phase currents, speed and position theta as the output.

The sub-modules of the virtual motor generate the back emf and hall sensor signals from the rotor position. The controllers under test are digital, and it is appropriate that the signals from the virtual motor are digital, avoiding the power circuit. The simplified representation of the virtual motor is as given in Figure 2.

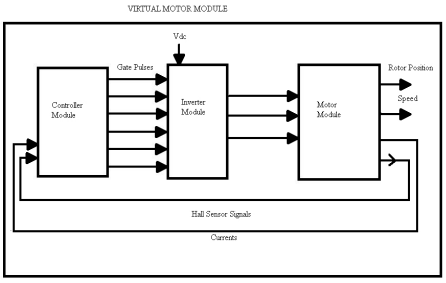

Figure 2. Virtual Motor With An Inverter And Controller Module

The simplest numerical method for the solution of initial value problems is Euler's method. It uses a fixed step size h and generates the approximate solution by using (7) and (8)

$$y_{n+1} = y_n + h * f(t_n, y_n) \quad (7)$$

$$t_{n+1} = t_n + h \quad (8)$$

The modified Euler numerical method uses Euler to step halfway across the interval evaluates the function at this intermediate point and then uses that slope to take the actual step as given in (9) to (12)

$$s_1 = f(t_n, y_n) \quad (9)$$

$$s_2 = f\left(t_n + \frac{h}{2}, y_n + \frac{h}{2} * s_1\right) \quad (10)$$

$$y_{n+1} = y_n + h * s_2 \quad (11)$$

$$t_{n+1} = t_n + h \quad (12)$$

The coding for the controller, inverter and the virtual motor is developed, using the Verilog HDL in the Xilinx software. The program module consists of the motor module which is a numerical solver of the differential equations. The method used is the modified Euler method. The solution gives the three phase currents, rotor speed and position θ. The position θ is used for the emf module to generate the trapezoidal back emf functions. It is also used to generate the three Hall sensor outputs. The controller takes the speed and current samples, and compares them with the reference speed and current. The inverter is triggered depending upon the hall sensor output. The inverter module is activated by these gate pulses generated by the controller. The output of the inverter module is the three phase voltages, which are supplied to the motor. The virtual motor accepts these voltages along with the load torque, and the solver gives three phase currents i_x, i_y, i_z, speed ω and position θ as the output.

5. SIMULATION AND RESULT

A. Verilog Implementation

The functionality of the various circuits of the BLDC motor was implemented using Verilog HDL programming. These programs were simulated before FPGA implementation to verify the performance of the program. The results of the decoder module that generates gate pulses using hall sensor signals are shown in Figure 3. The inverter module was designed such that voltages are represented using only two bits. The MSB shows sign and the LSB shows magnitude. The output of this module is shown in Figure 4. The entire motor module was simulated and the results showing the back-emfs and currents of phase A along with motor speed and hall sensor signals are shown in Figure 5. Note that the variables are in 24 bit fixed point representation with 13 least significant bits are used to represent decimal places.

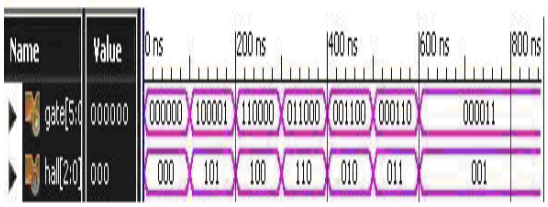

Figure 3. Decoder Output.

Journal of Theoretical and Applied Information Technology
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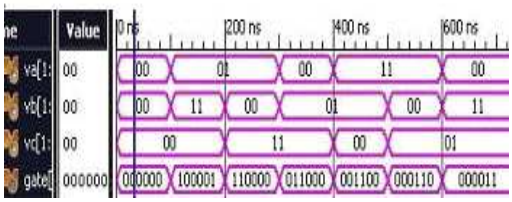

Figure 4. Inverter Output

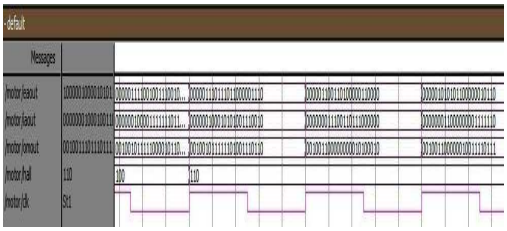
Figure 5. Motor Output

B. FPGA Implementation

The Verilog code that imitates the functionality of the motor was downloaded into a Xilinx Spartan 3E FPGA. The Spartan3E starter kit was used. The digital variables were converted to analog form using the built-in Digital to Analog converter and the waveforms were observed in an oscilloscope. The setup is shown in Figure 6. The waveform showing the inverter phase voltage of phase X,Y,Z is shown in Figure 7. The waveform showing the back-emf of phase X,Y,Z which is trapezoidal in nature are shown in Figure 8. The figures 9 to 11 show the variation of torque with speed. The waveform in Figure 9 represents the torque at steady state speed. Figure 10 (a) represents increase in load torque from 25% of the rated value to 100%, with proportional decrease in speed. Corresponding current waveform is shown in Figure 10 (b). Figure 11 (a) indicates decrease in load torque from 100% to 25% of rated torque with proportional increase in speed and the corresponding current waveform is displayed in Figure 11 (b). This is in accordance with the equation (5), since torque is inversely proportional to the speed and directly proportional to the current.

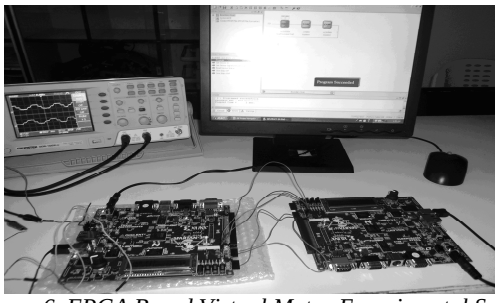
Figure 6. FPGA Based Virtual Motor Experimental Setup

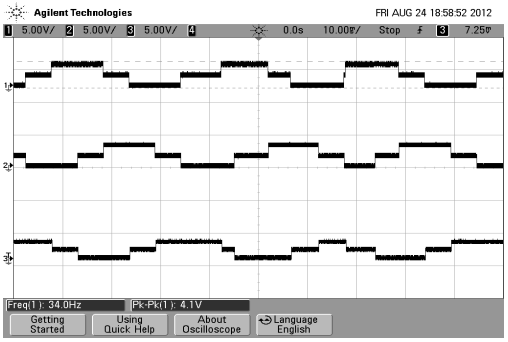

Figure 7. Phase Voltage Waveform.

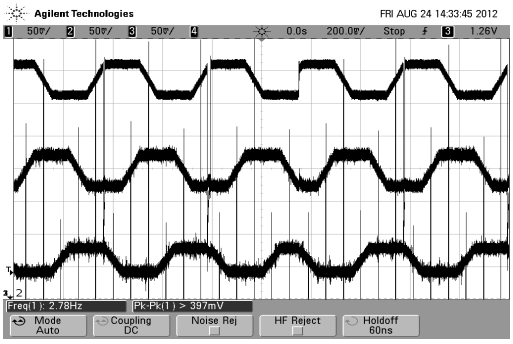

Figure 8. Back Emf Waveform

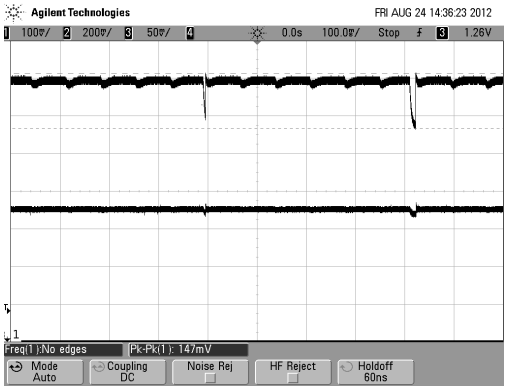

Figure 9. Torque And Speed At Steady State

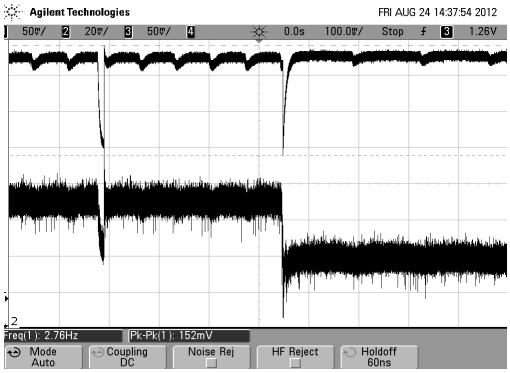

Figure 10 A. Decrease In Speed When Load Torque Increased From 25% Of Rated Torque To 100%

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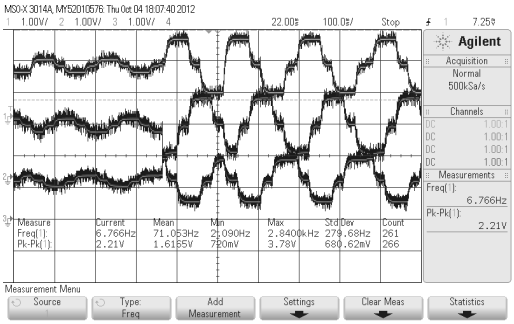

Figure 10 B. Current Corresponding To Increase In Load Torque From 25% Of Rated Torque To 100%

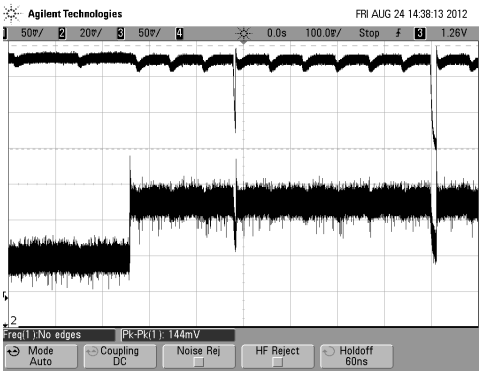

Figure 11 A. Increase In Speed With Decrease In Torque From 100% Of The Rated Torque To 25%

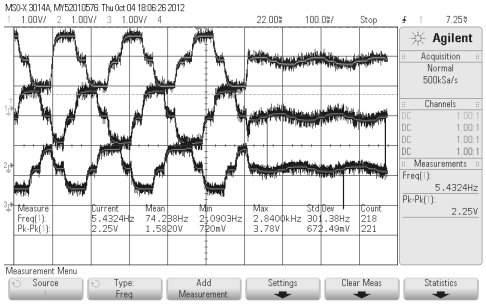

Figure 11 B. Current Waveform Corresponding To Decrease In Load Torque From 100% Of The Rated Torque To 25%

6. HARDWARE IMPLEMENTATION

The hall sensor output from PMBLDC motor is given as the input to the FPGA Spartan 3E. The FPGA generates the gate pulses required to drive the IGBT switches. The hardware implementation is tested with the setup shown in Figure 12. Once the supply is given to the inverter, controller is applied with a ramp at a voltage corresponding to the reference speed for about 2 seconds which will start the motor. As it rotates, it produces the hall sensor signals. Once the decoded signals are obtained, these are given to the gates of the IGBT switches which produce the three phase Vx,Vy,Vz voltages. These voltages are fed as input to the motor and it rotates. The stator currents and terminal voltage are shown in Figure 13 and 14 respectively.

7. CONCLUSION

Working with a virtual motor than a real motor provides an efficient way to test new control algorithm and versatility to use various load torque combinations thereby speeding up the process and providing an efficient test method. The simulation of the BLDC motor model is carried out using Xilinx ISE and the results are presented. The dynamic characteristics of the BLDC are written into a FPGA, using the Verilog HDL to behave as a virtual motor. The coding implements the mathematical solution based on modified Euler method, to solve the differential equations. For simplicity, the virtual motor, the inverter and controller are implemented within a single FPGA. The results compared with real BLDC motor agrees well with the virtual motor thus validating the virtual motor model. This model can be used for educational purposes and for validating the controllers being designed. The work can be extended in future by implementing the improved Euler method or Runge Kutta methods based solvers. The implementations of the virtual motor could be done in a single chip as System on Chip and used for validation of various motor controllers.

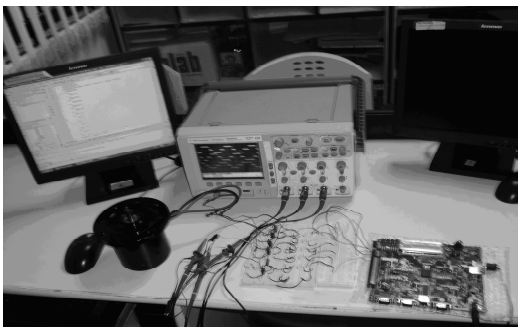

Figure 12. BLDC Hardware Experimental Setup

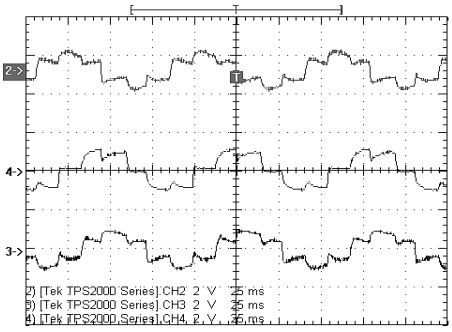

Figure 13. Stator Currents

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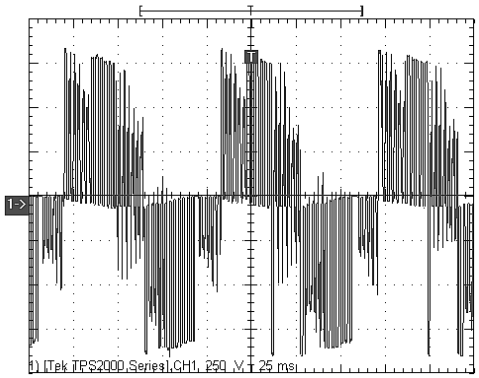

Figure 14. Terminal Voltage.

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