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STUDY OF A NEW PHASE DETECTOR BASED ON CMOS

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ABSTRACT

An analog phase discriminator, based on the two complementary CMOS switches, was proposed to measure the initial phase of the sinusoidal wave. The circuit structure of the phase discriminator and its principle were presented, and the phase computational formula was derived through a series of circuit theories. So the initial phase was acquired directly from the circuit, which covered a wide frequency range with high accuracy, controllable, stability and reliability. The effectiveness and feasibility were verified through simulation experiments at the frequency of 1.25MHz. The results show that the maximum phase error is less than 0.05 °, and the corresponding root-mean-square(RMS) value is lower than 0.2 under 256 times measurement.

Keywords: *Phase Detector, Complimentary, CMOS Switches, Initial Phase Detection*

1. INTRODUCTION

Phase is one of the three elements of the alternating signal. And the phase difference of sinusoidal signals at the same frequency is widely used in many areas, such as industrial automation, intelligent control and electronic communications [1, 2]. The study of the phase detector, whether analog or digital phase detector, is mainly focused on the measurement of the phase difference of the two sinusoidal signals of the same frequency. However, under certain conditions, such as the measurement of material permittivity, impedance measurement, the initial phase of the sinusoidal signal becomes the key element due to containing important information [3]. The initial phase detection of the sinusoidal signal is mainly obtained through the traditional analog phase or digital phase detection techniques with a reference signal to get the phase difference and then convert it into the initial phase. But the direct detection of the initial phase of the sinusoidal signal has seldom been studied.

In the analog phase detection, simplified calculation of the linear interpolation method to improve the accuracy of the measurement for SCM system was proposed by Zupu Deng in Sichuan computer Research Institute. After analyzing the shortcomings of the widely used zero-crossing time difference test mode, and the specific approach was also given, but no improvement in the phase detection circuit was made and the operating frequency was not high enough [4]. In digital phase detection, containing the repeat count, while the retardation of the measured signal a plurality of cycles in the cycle of the original measured signal of the same number of counts was proposed by Lianlian Wang in Suzhou University, where the counting result of the plurality of phase pulse width was obtained through the two counting result of subtraction [5]. Zhang Yunmei and Yang Yuzhen, describes a method to implement the phase locked loop with the single—chip 8031 used and presents the design scheme of the frequency—comparator and phase — comparator and the hardware realization method. But the result is not as desired and it only could operate at the low frequency [6]. A high resolution phase detector based on PLL is proposed by JI Rong etc. Based on all analysis of the effects of static phase errors delay-locked loop, it incorporates the feature of the PD with the feature of the Alexander I'D. Compared with conventional linear and binary phase detectors, it not only has advantages of a perfect linear PD, but also solves the problem of dead zone in course of charge pump switch transition, which exists in linear phase detesters [7].The phase difference was calculated from the ratio of the counting result in the pulse width of the phase and the counting result

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of the original signal within cycle, and the CPLD was used as a counter, the counting error of this method itself was reduced to some extent, and the accuracy of the phase was also improved. But the error would be larger when relatively high measurement accuracy is required or the pulse width of the phase is less than the count clock cycle. Space-based real-time signal difference phase detection system based on FPGA was proposed [8], this digital circuit was able to detect the tiny phase difference of the analog signal, and could be used to correct the operation of the space-based system or identify the problem of the space-based system. And an adaptive method was used to be able to meet the requirements of complex environments and to achieve a better phase accuracy.

Above all, the present status, a CMOS-based switch phase is designed in this paper; its reasonableness is proved through circuit theory derivation. Section 2 presents the structure of the whole system. In section 3, we propose the circuit structure and design for each module of the system, including Transformer Modulation, Control Circuit Design, CMOS Switches Design, Integration Design and Voltage Regulation and A/D Conversion. Section 4 shows the simulation results at the 1.25MHz of the sinusoidal signal based on PSPICE and the analysis to the experiment data. We give the conclusion to the whole paper in section 5 that the phase discriminator simplifies the detection process of the initial phase; the initial phase of the sinusoidal signal could be detected directly without conversion.

2. INITIAL PHASE DETECTION SYSTEM

The system block diagram is shown in Fig.1. Firstly, the signal to be detected is shaped by the transformer, sent to the phase discriminator switches. And the signal generator produces the series of control waves. Then, the shaped signal is sent to the integrator circuit, and the CPU is responsible for generating the control timing series. The integrator output signal is to be appropriately adjusted by the voltage adjustment circuit so that the voltage amplitude could be limited in the sampling voltage range of the A / D conversion in order to get a proper magnification. Finally, based on the delivered voltages from the A / D, the initial phase of the signal to be detected can be obtained

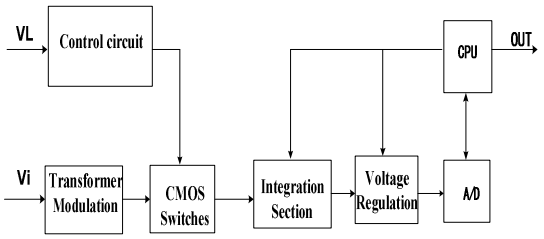

Figure1 System Block Diagram

3. CIRCUIT STRUCTURE AND DESIGN

3.1 Transformer Modulation

To obtain inverted and non-inverted forms of the input, the design of the shaping circuit of the transformer is taken, as shown in Fig. 2. The sinusoidal signal Vi is applied to the transformer T, which works in single-ended mode of double side transformations, with the deputy coil turns ratio 2:1 and the center tap to ground of the transformer secondary coil, wherein R1 = R2.

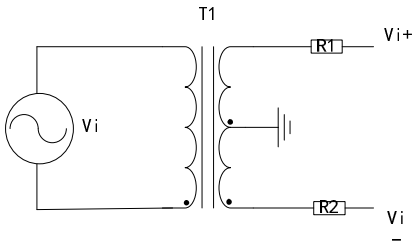

Figure2 Transformer Modulation

3.2 Control Circuit Design

For the extraction, Sine and Cosine clocks VL are as select lines for the CMOS switch group. The control signal generator circuit is shown in Fig. 3, including two integrated operational amplifiers A1and A2, which are AD797 with a very low noise, low distortion. VL is applied to the positive input terminal of A1 and a negative input terminal of A2, the other two terminals of them are grounded, so A1 and A2 form up a comparator. And the output LO+, LO- that the groups opposite phase square wave are generated from it, which are then used as the control signal to the switches.

3.2 CMOS Switches Design

The CMOS switches are the key component as to obtain the information of the initial phase of the input. The CMOS circuit frame as shown in Fig. 4, in which Q1, Q2, Q3, Q4, are four identical N-channel enhancement type MOSFET tubes which are integrated on the same chip, and therefore they are of a good symmetry. The transistors are divided into two groups, Q1 and Q2 is a group, Q3, and Q4

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is another group.Q1, Q2, Q3, Q4 made an interlock switch group, which constitutes the double-balanced phase detector. The control signals are applied respectively to the gate electrode to change the switches wok state. LO + is connected to the gates of Q1and Q2, and LO- linked to the gates of Q3 and Q4. The four FET transistors play a role of switches to Vi + and Vi - without the effects of mixing and amplification. When LO + is at the positive half cycle, LO- must be in the negative half cycle, Q1 and Q2 are on conduction, but Q3 and Q4 are cutoff. And while LO + is at the negative half cycle, LO- must be in the positive half cycle, Q1 and Q2 are on turn, meantime Q3 and Q4 turn off. The output of the CMOS switches can be expressed as Equ. (1).

$$V = \begin{cases} A\sin(\omega t + \phi), 0 < t \le T/2 \\ -A\sin(\omega t + \phi), T/2 \le t < T \end{cases} \quad (1)$$

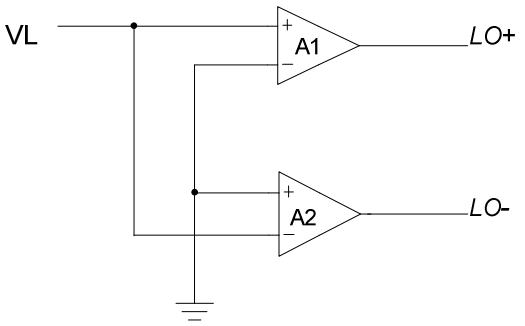

Figure 3 Control circuit

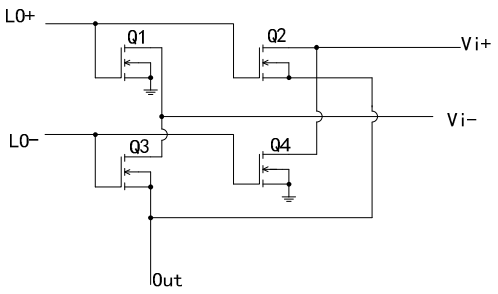

Figure4 CMOS Switches circuit

3.4 Integration Section

The integrator section is shown in Fig. 6. It is a crucial part as it is responsible for getting a pure DC from the output of CMOS groups. And from the DC data, the result of the initial phase can be calculated. S1 is set to control the working status of the integrating capacitor C, and S2 is to control the input of the integrator circuit. The timing diagram was plotted in the Fig.7.

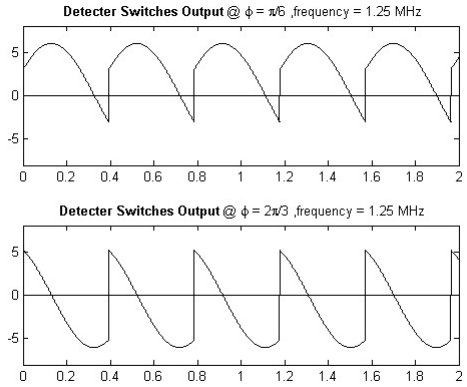

Figure5 Ideal Wave Forms V in Matlab

A plot expected output signals at the phase shifts of π/6 and π/3 are shown in Fig.5 using Matlab analysis.

The circuit does integration from t_1 to t_2 and it holds the result of integration, then starting from t_0 to t_1, the integration capacitor will be in discharge. Assuming the beginning of each integration, the amount of charge on the integrating capacitor is at zero. So at the period of each integration $0 \sim T$, the average voltage of the integrator can be expressed as the following

$$\overline{V} = \frac{1}{T}\int_0^T V dt = \frac{2A}{\pi}\cos\phi \quad (2)$$

Therefore, the initial phase of the input sinusoidal signal is obtained as Equ. (3).

$$\phi = acr\cos(\frac{\pi\overline{V}}{2A}), 0 \le \phi \le \pi \quad (3)$$

3.5 Voltage Regulation and A/D Conversion

The voltage adjustment is designed to regulate the voltage to the scope of the A/D sampling voltage. As shown in Fig. 8, it includes a no inverting scaling circuit which is composed of Rf, R4, R5, R6 and A5, and an inverting scaling circuit which contains A6, Rf2 and R7. Wherein B1, B2, B3 are the same transistors 2SC3326 as the choosing switches which are mastered by CPU, which are on at the high level but off at the low voltage.

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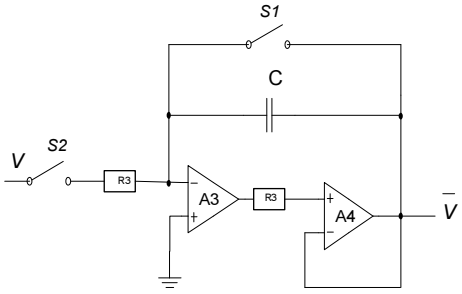

Figure6 Integration Circuit

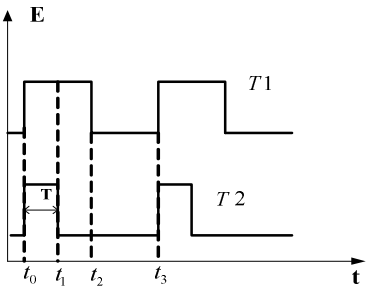

Figure7 Integration Timing Diagram

The AD7988 is adapted to the scheme as an A/D converter which is a 6-bit analog-to-digital converter ranging from 2.5 to 5V voltages.

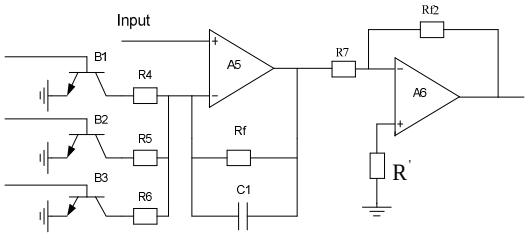

Figure8 Voltage Adjustment Diagram

4. EXPERIMENTAL RESULTS

Based on the above circuits and theoretical deduction Equ. (3), the simulation results are obtained as shown in Fig.9 and Fig10 by means of PSPICE simulation, where the amplitude of the input sinusoidal is 5V with the frequency of 1.25MHz. Fig.9 stands for the errors of the measurement versus the expected, and Fig.10 describes the root mean square (RMS) distribution of 256 times measurement. So the results show that the initial phase's absolute errors are less than 0.05 °, and the RMS values under measurements of 256 times are below 0.2.

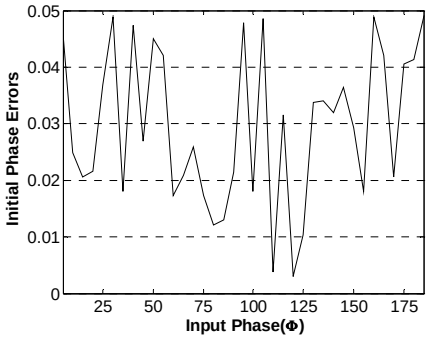

Figure9 Phase Error Chart

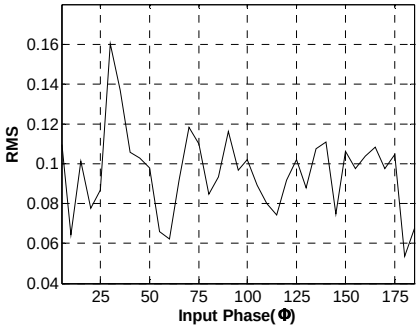

Figure10 RMS Chart

5. CONCLUSION

In this study, the phase detector's oscillation signal is a square wave acting as the role of switch, which is not directly to be multiplied with the input signal. As a result of complementary symmetrical structure of the two groups of switches, the four FET tubes can be integrated in a single chip, so the circuit is of a consistent performance with a nice symmetry. At the same time, the integration period is increased, and the output voltage is enlarged with double amount while compared to a single CMOS transistor increasing. This phase detector has a large dynamic range, wide frequency coverage, stable performance, and the experiments show that the system can reach better measurement accuracy. At the same time, we acknowledge our task is not perfect and much further work need to be done in the future.

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