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FPGA-BASED DESIGN ON REAL-TIME TOW STAIN DETECTION

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ABSTRACT

This paper introduces a tow stain detection method based on FPGA. To capture moving images through the line scanning CCD in real time and to design algorithms according to the different characteristics on the tow and stains.Then download it to FPGA development board running and debugging. Finally, displayimages on PC through the video conversion module.The experiments show that this design can effectively detect the stains on the running tow with high speed. It also has good stability and high error detection rate.

Keywords： *FPGA; CCD; Stain Detection*

1. INTRODUCTION

FPGA (Field Programmable Gates Array) is the further development of programmable devices, such as PAL, GAL, CPLD and so on. FPGA device is a kind of high density digital integrated circuit configurating and defining on site according to the requirements of the system by the user. Miniaturization, convenient, low power consumption, programmable, fast, practical and some other advantages make it has been widely used in recent years[1]. It appears as a semi-custom circuit in Application-specific Integrated Circuit (ASIC) field, not only solving the shortcomings of the original custom circuit but also overcoming the limit of gate numbers of the existing programmable devices[2].

FPGA development board is able to meet the need of long-running production line testing with low-powerchips. Besides it would not be affected even under uninterrupted operation,which ensures the accuracy of the judgments and the speed of the operation.

2. STAIN DETECTION FRAMEWORK DESIGN

The overall framework of tow stain detection is shown in Figure1.

The procedures of testing are as follows.The line scanning CCD(D5M)captures real-time images first. And then FPGA controller processes the collected data with the inside algorithm. Once detecting stains, FPGA alarms a signal and controls the VGA to pause for 6 seconds, at the same time records the second seconds' image information and transfers the image to real-time display on PC through the video conversion module. Staffs can do some follow-up processings according to the detection screen or the saved data information.

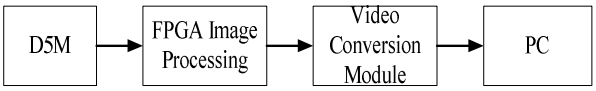

Figure1. The Overall Framework Of Tow Stain Detection

3. SOFTWARE DESIGN

3.1 Algorithm Design

We get the image with a black stain on it and save as a BMP format file. Camparing and analysing the stain's and the tow's RGB components.

Figure2 is the gray level histogram of a image without any stains, while Figure3 is the gray level histogram with a black stain on it.

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By comparison of the two images, we can find that for the black stain the B component values in a range between 25 to 90 while the background(tow) values more than 150.

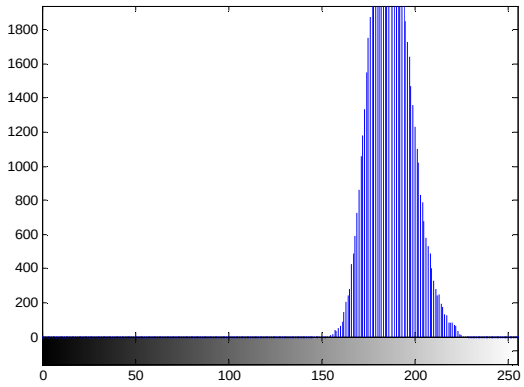

Figure2. Gray Level Histogram Of A Image Without Stains Under B Component

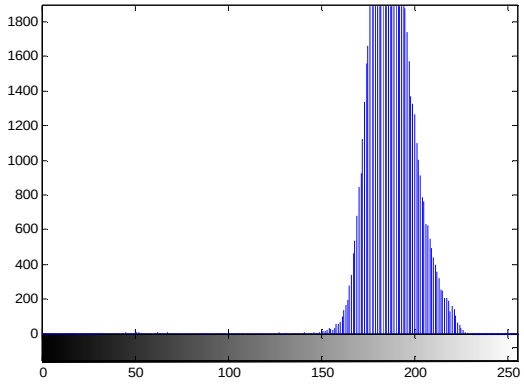

Figure3. The Image's Gray Level Histogram With A Black Stain Under B Component

Therefore, using a simple threshold segmentation algorithm[3] can isolate the black stain from tow. Threshold function can be expressed as follows:

$$f(x)=\begin{cases}255 & x \geq T\\ 0 & x < T\end{cases}$$

Where T is the selected threshold.

For example,when dealing with black stain in the program, we set the parameter TH= 12'h90 under the B component.

Dealing with other stains, we take a similar approach, implement these algorithms in the program and download it to the FPGA development board.

3.2 FPGA Design

Most FPGA designs use modular ideas[4], by which a complex system can be divided into a number of small and easily manageable units. The main modules of stain detection are shown in Figure 4.

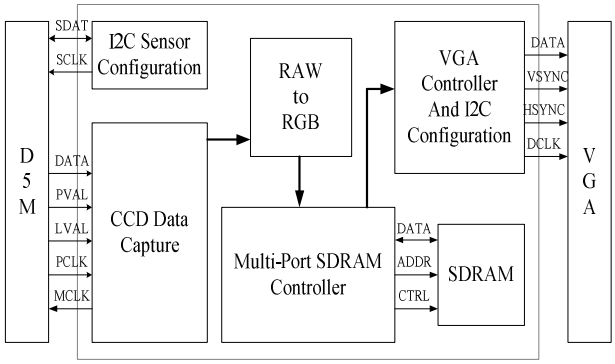

Figure 4. FPGA Modular Design

Image Acquisition Module: D5M scans images from left to right and returns to the left to scan the next line when a line's pixels are all scanned. Each pixel's RGB values is expressed as 2*2 grid square which is shown in Figure5: where R is the value of the current pixel's R component and B is the value of the current pixel's B component while G is the average of Gr and Gb[5][6].

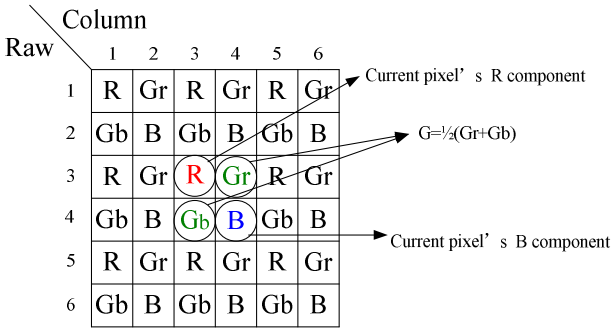

Figure5. RGB Component Diagram Of D5M

2)I2C Control Module:CCD part is under the control of I2C mode. I2C (Inter-Integrated Circuit)bus is a two-wire serial bus(data and clock)[7]. It's used to connect the microcontroller and its peripherals. The required clock of CCD module is generated by I2C, while CCD Data Capture module generates the first clock that D5M requires. The acquired images can be displayed on VGA when converted to RGB formats.

3)RAW to RGB module: the Raw format is converted to RGB format in this part.And designing a detection algorithm according to the relative characteristics of the tow and stains.At the same time Generating an alarm signal to video

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conversion module to save the image information timely.

We use Linebuffer in this module which, in fact, is shift register altshift_taps. Shiftin is the input and the output is shiftout.

altshift_taps_component.lpm_type="altshift_taps ",

altshift_taps_component.number_of_taps = 3,

altshift_taps_component.tap_distance = 1280,

altshift_taps_component.width = 12;

The mentioned program above illustrates that parallel output lines (number_of_taps) is 3 and the width(tap_distance) is 1280. Each pixel is represented with 12 bits wide. That is, outputting 3 lines and 1 row together and after 1280 clock outputting an image with 3 integral lines.

Realizing the designed algorithms in this module and down program to the FPGA development board.To get the best threshold and accuracy on the basis of multiple experimental debugging.

4)SDRAM Control Module:In this experiment we choose DE2_70 as FPGA development board.There are two 32MB-SDRAM on DE2_70[8].Gr and B components are stored in the first SDRAM and the Gr and R components are stored in the second one.

5)VGA Control Mode: VGA displays images in real time with line by line scanning mode,including line scanning and field scanning[9].

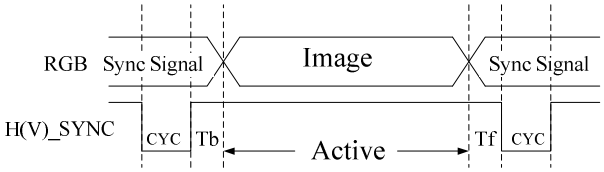

Figure 6. FPGA Modular Design

As is shown in Figure6, the synchronizing signal includes the back and the front part and the logic low part between them[10][11]. Some parameters in the program are as follows:

```
//      Horizontal Parameter      ( Pixel )
parameter     H_SYNC_CYC  =     112;
parameter     H_SYNC_BACK=      248;
parameter     H_SYNC_ACT  =     1280;
parameter     H_SYNC_FRONT=     48;
parameter     H_SYNC_TOTAL=     1688;
//      Virtical Parameter      ( Line )
parameter     V_SYNC_CYC  =     3;
parameter     V_SYNC_BACK=      38;
parameter     V_SYNC_ACT  =     1024;
parameter     V_SYNC_FRONT=     1;
parameter     V_SYNC_TOTAL=     1066;
//      Start Offset
Parameter X_START
      =H_SYNC_CYC+H_SYNC_BACK;
Parameter Y_START
      =V_SYNC_CYC+V_SYNC_BACK;
```

We set the line counter and field counter separately.Line scan is starting when line counter equals X_START.And once the entire line is scanned over continues scanning the next line.Field scan is the same as line scan.

Figure7 gives the software flowchart:

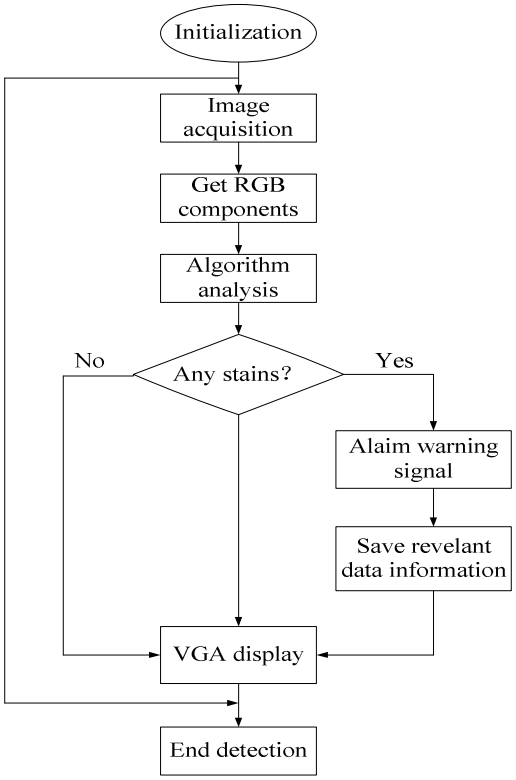

Figure7. Software Flowchart

4. THE SIMULATION AND TESTING

We choose Altera's software QuartusII10.0 to synthesize the design and Modelsim-Altera to

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simulate. The design is tested by using DE2_70 as the FPGA development board.

The specific steps that QuartusII10.0 calls modelsim6.5 to simulate are as follows[12][13]:

(1)Selecting Modelsim-Altera as the simulation tool before the new project is finished.

(2)Set the path of modelsim.exe:ools->options->EDA tools options(usually in modelsim installation directory under win32 folder).

(3)After the project is compiled, creating a test file:processing->start->start test bench template writer.This file lies in the simulate/modelsim folder of the project with suffix vt.Open and complete the test file.

(4)Follow the steps that assignment->setting->EDA tools setting->simulation->complie test bench to select complie test bench and click test bench.

(5)Finally clicking tools->run EDA simulate tool->EDA RTL simulation that can successfully call modelsim simulation.

For the entire system, we give each module a separate simulation fist and then take the joint testing[14]. The main algorithm module RAW2RGB's simulation is shown in Figure8.

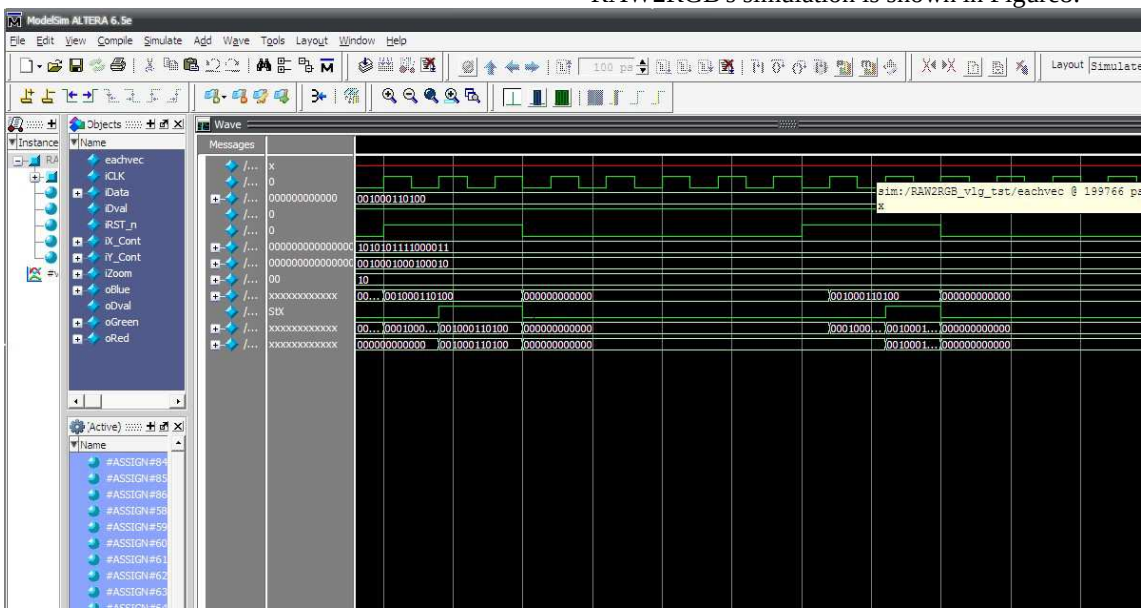

Figure8. The Simulation Of RAW2RGB Module

We can see the output waveform agrees with the design requirements and achieves the original goals.

Debugging the entire system in production line. The production line's speed is up to 10m/s and the stain's size is only 5mm2.The test results show that the design can detecte stains quickly and efficiently. The system functions stable and at the same time cannot be affected by the external environment.

5. SUMMARIZE

Because of its short design cycle, high reliability, fast function speed and the superiority of the cost, FPGA has become the fastest-growing category in the electronic components industry[15].

This paper takes full account of the tow and the stains characteristics, the production line's fast speed, the request high accuracy and the changing environment, designs a tow stain detection system based on FPGA technology. It not only simplifies hardware design, improves production efficiency and automation level, but also reduces the waste of social labor, which has a good application prospect.

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