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NOVEL HIGH RELIABILITY BANDGAP-BASED UNDER-VOLTAGE-LOCKOUT METHODS

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ABSTRACT

In this paper, a novel method to build under-voltage-lockout (UVLO) circuit has been developed. The method based on bandgap reference voltage comparator, which take advantage of a reference voltage produced by itself realizes voltage compare, stability of parameters such as threshold point voltage, hysteretic range, without utilizing an extra bandgap reference voltage. An abstractive feature of the proposed circuit is that it achieves UVLO function by a simple structure, without complicated logic components. Therefore, its power consumption is low. With the presented method, the novel under voltage lock out circuit achieves hysteretic range of 2.39V; its turn-on voltage is 12.0V, and turn-off voltage is 9.61V at 25℃.Simulation results are based on 0.5 μm BCD process technologies.

Keywords: *Power Management, Under Voltage Lock Out, Bandgap Voltage Reference, Hysteretic Range.*

1. INTRODUCTION

With the development of semiconductor technology, the requirement of power management chips, such as switch frequency, transmission delay, power consumption become more and more important to make sure the chips work in the steadily situation. Generally, when the chip starts up, the power outside charges its internal capacitors, so the chip's voltage rises gradually to its start-up level. However, the system is likely turned off over again just after opening if the load currents of the system are too large.

Under voltage lock out (UVLO) circuits are essential in the power management chips to avoid the above situation. A great variety of UVLO circuits has been developed for make sure the system starts up normally and works steadily, most of them based on the conventional structure which consists of sample resistance, bandgap reference block, and voltage comparator (as shown in Fig. 1) [2].

When the system starts up, supply voltage VDD generate a stable reference voltage to the voltage comparator by the on-chip bandgap reference module. Meanwhile, sample resistance net provide the supply voltage's information to the another pin of comparator. When the sample voltage is lower than the reference voltage, comparator output controls the other modules within the chip, prohibit system work; On the other hand, the system start to work [4]. Actually, the UVLO circuit just likes a hysteresis comparator; it must have the features of rapid reaction speed, steady threshold voltage, reasonable hysteretic range and low temperature drift.

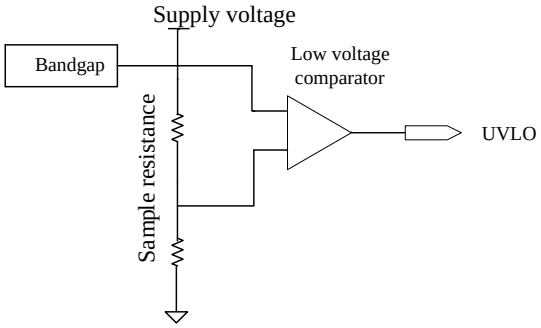

Figure 1 Traditional UVLO Structure

These circuits expand a lot of energy because of their complex structure. In addition, the bandgap reference voltage only produces an exact voltage within limits. If the reference voltage is not stable, the UVLO circuit can't work in the right situation. It could hurt the system no matter the reference voltage is higher or lower than the normal value.

In this paper, a bandgap reference voltage comparator is employed to implement the proposed UVLO circuit. It could reach the

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performances of UVLO circuit without complicated digital logic, bandgap reference block, and conventional voltage comparator. The chief features of proposed circuit are simple circuit topology, low temperature drift, accurate threshold voltage, and low power consumptions. A proposed block diagram is shown in Fig.2.

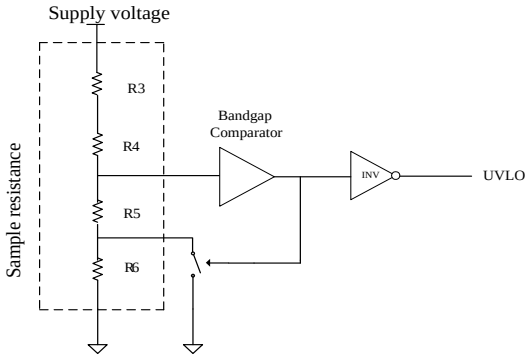

Figure 2 A Novel UVLO circuit

2. UVLO METHODS DESCRIPTION

Fig. 2 shows the composition of the proposed UVLO, which is composed of a bandgap-comparator, and sample resistance.

When the system is in under-voltage state, the bandgap-comparator compares the inner VREF signal with the division of the system voltage which is sampled by the resistances and output an under-voltage signal. Then, the under-voltage signal is strengthen and inverted by INV block.

3. UVLO CIRCUIT REALIZATION

Fig.3 shows the circuit architecture of the proposed under voltage locks out. It consists of bandgap reference voltage comparator, current mirror, inverter, and sample resistance. The resistive divider consists of R3, R4, R5, and R6. They can reflect changes in supply voltage. By controlling M1 access or not make the circuit have a function of hysteresis. Q1, Q2, R1, and R2 composed the comparator utilizing bandgap reference principle. M2 and M3 are the active loads of the comparator. Since the emitter area of Q1 is as 10 times as that of Q2, the transconductance relationship of the two bipolar is as follows:

$$g_{m1} = 10 g_{m2} \tag{1}$$

By small signal analysis shows:

$$g_m = \frac{\beta + 1}{r_{be}} \tag{2}$$

Where β is the DC current amplification factor, r_{be} is the resistance between base and emitter. Because of the feedback of their emitter resistors R1 and R2, the equivalent transconductances of the two bipolar are:

$$G_{m1} = \frac{g_{m1}}{1 + g_{m1}(R1 + R2)} \tag{3}$$

$$G_{m2} = \frac{g_{m2}}{1 + g_{m2} R2} \tag{4}$$

Consider of equation (1), we can obtain

$$G_{m1} = \frac{g_{m2}}{1 + g_{m2} R_2 + g_{m2} R_1 + 1/10 - 1} \tag{5}$$

Generally, $g_{m2}R1 >> 1$, so $G_{m1} << G_{m2}$, it means that the varying rate of I_{C1} is much rapider than that of I_{C2} as VCC fluctuates. I_{C1} is the current through collector of Q1, while I_{C2} is the current through collector of Q2. This current's asymmetric transformation is the key to work of bandgap comparator. So we simulate the currents of the two bipolars varying with VDD as shown in Fig.4.

From the figure above, we can see that, before 2.3ms, $I_{C1} > I_{C2}$, UVLO is low, the chip does not work. At 2.3ms, both of the currents of the two bipoars increase sharply. But the transconductance of Q1 is smaller than that of Q2, I_{C2} have been influenced greater. Quickly, $I_{C1} < I_{C2}$. The output of UVLO is high.

M2, M3, M4 form a current mirror structure, M2 will copy the current flow through Q1 to M3, while the current flow through M3 is equal to Q2's collecting electrode current. When I_{C1} and I_{C2} are inconsistent, M3 will change its work region, the potential of point B which is used to control M5 also changes. When M5 is turn-on, Q6 would work, M6's gate potential is high. Therefore, the potential of point C is low, M1 is turn-off, so the output signal of UVLO block is high. On the contrary, when M5 is turn-off, the output signal of UVLO block is low.

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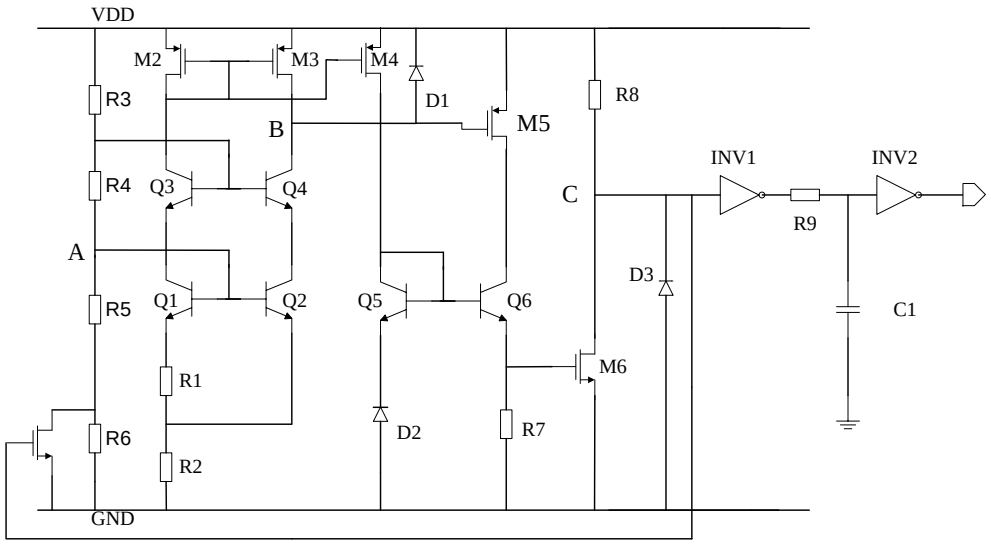

Figure 3 Structure of the Proposed UVLO Circuit

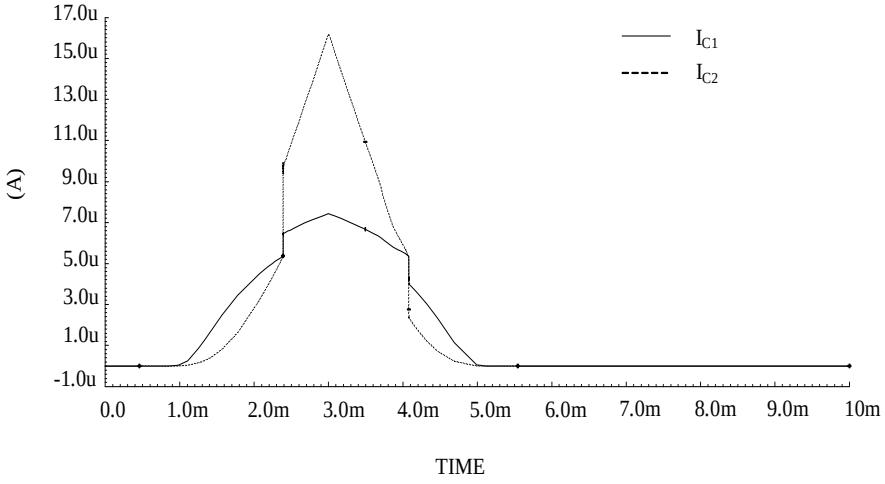

Figure 4 Curves of IC1, IC2 versus VDD

Through the above analysis we can see, the UVLO block will change its output when I_{C1} is not equal to I_{C2}, so circuit is in equilibrium when I_{C1} and I_{C2} are consistent. At this point, the potential of point A is the reference voltage.

From the Fig.3 we can see,

$$I_{C1} = I_{C2} = \frac{V_{BE2} - V_{BE1}}{R_1} \quad (6)$$

The voltage between base and emitter of bipolar is

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \quad (7)$$

$$I_{C1} = I_{C2} = \frac{V_T}{R_1} \ln 10 \quad (8)$$

Where Is represents the reverse saturation current of the base-emitter junction, and V_T is the thermal voltage. The base voltage of Q2 is the threshold voltage.

$$V_{REF} = V_{BE2} + 2I_{C2}R_2 \quad (9)$$

Substituting [6] in [7] gives

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$$V_{REF} = V_{BE2} + 2\frac{R_2}{R_1}V_T \ln 10 \quad (10)$$

When T=300K, V_T =0.026V. V_T is proportional to the absolute temperature, V_T increases as the temperature increases while V_{BE} decreases. The temperature coefficient of V_{BE} is

$$\partial V_{BE} / \partial T \approx -2mv/°C \quad (11)$$

In Eq. (8) the first term increases with temperature and the second term decreases with temperature. The threshold independent of the temperature and the supply voltage can be obtained by properly adjusting the ratio of R2 to R1.

There are three situations when the power supply VDD rises from the low value to the high gradually.

1. When the circuit start-up, the supply power VDD is low, so the potential of point A is lower than threshold voltage. Because the equivalent transconductance of Q1 is lower than that of Q2 as noted above, I_{C2} is smaller than I_{C1} when VDD does not reach to normal supply voltage. If M3 work in the saturation region, Q4 work in the linear region, I_{M3} which equals to I_{M2}, is larger than I_{C2}, It is impossible in the same direct current gateway, so M3 work in the linear region. Potential of point B is approximately equal to VDD, $|V_{GS5}|$is lower than V_{TH5}, and M5 is turn-off, UVLO's output is high potential. At this point, the power management chip does not work, and M1 is turn-on. The potential of point A is:

$$V_A = \frac{R_5}{R_3 + R_4 + R_5} VDD \quad (12)$$

2. When VDD continuously rises to be close to Von, the collector currents of Q1 and Q2 are appropriately equal, so $I_{C1} \approx I_{C2}$, Thus, all of the MOSFET is wok in saturation region, and have equal drain currents.

3. When VDD is higher than V_{ON}, the potential of point A exceeds V_{ON}, I_{C2} become larger than I_{C1}. It is impossible that I_{M3} is smaller than I_{C2} in the same one direct current gateway. So Q4 is impelled to work in saturation region to make sure $I_{M3}=I_{C2}$. Thus, it is low level at node B, M5 is turn-on, there is a current flow through R7 to make sure M6's gate potential is high than threshold voltage. UVLO's output is low level, M1 is turn-off, R3, R4, R5 and R6 is series connection. The potential of point A is:

$$V_A = \frac{R_5 + R_6}{R_3 + R_4 + R_5 + R_6} VDD \quad (13)$$

The chip works normally in this case. It is obviously that the UVLO circuit has a very rapid reaction speedy, because the mirrored pairs are quite sensitive to the difference of their currents. There are also three situations when VDD becomes lower from the high value.

From discussing above, we can obtain the UVLO circuit's hysteretic range. When VDD rises but does not reach to Von, UVLO is high, M1 is on, when V_A reach to V_{REF}, the output situation of UVLO will change, the potential of VDD at this point is the high level of threshold voltage, so

$$V_{ON} = \frac{R_3 + R_4 + R_5}{R_5} V_{REF} \quad (14)$$

Similarly, we can get the turn-off voltage V_{OFF} as follows:

$$V_{OFF} = \frac{R_3 + R_4 + R_5 + R_6}{R_5 + R_6} V_{REF} \quad (15)$$

Thus the hysteretic range of the UVLO circuit is

$$V_{ON} - V_{OFF} = \left(\frac{R_3 + R_4 + R_5}{R_5} - \frac{R_3 + R_4 + R_5 + R_6}{R_5 + R_6} \right) V_{REF} \quad (16)$$

From the formula above, we know the hysteretic range can be determined by the value of R6.

4. SIMULATION RESULTS

The circuit has been simulated by using the EDA soft, Hspice, based on 0.5μm BCD process technologies. Because the power management chips are often applied in a wide range of temperature and many of the transistor parameters influenced by temperature so much. It is necessary to reduce the errors of the hysteretic range and the threshold voltage to satisfy the requirement used in a wide range of temperature. The simulation results of designed UVLO circuit varying with

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temperatures, in -25℃, 25℃, 75℃, 125℃ respectively, are shown in Figure 5.

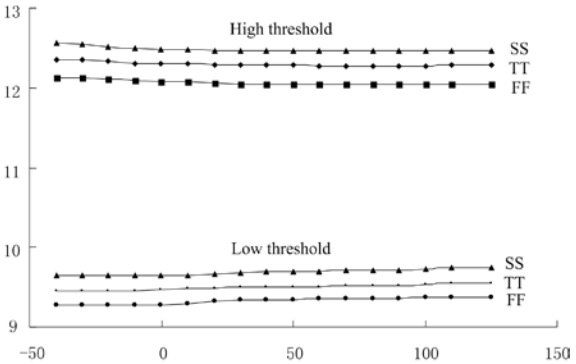

Figure 5: Temperature characteristic of threshold voltage under different model corners

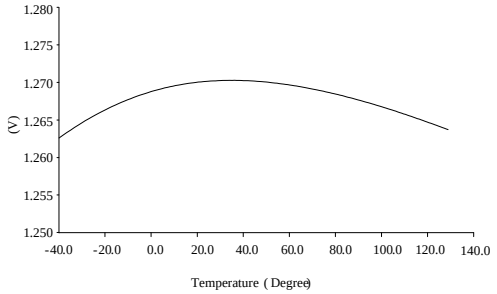

Figure 6 Temperature coefficient of bandgap-Comparator

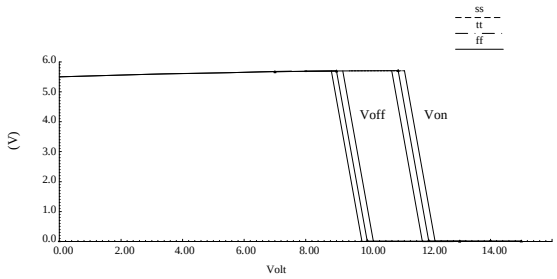

Figure 7 Hysteretic Range in Different corners

The temperature characteristic of the bandgap-comparator with the TT model corner is shown in Figure 6. The temperature coefficiency will get to about 20ppm/℃ and greatly increase the stability of UVLO threshold voltage. Thus the major advantage of the designed circuit is that it can work in a wide range of temperature with low range. Figure 7 shows the result of different corners. As it shown in Figure 5 and Figure 7, error voltage is no larger than 0.05V, only account for 5 per thousand of threshold voltage.

5. CONCLUSION

Under voltage lock out is one of the necessary functions in power management chips. This paper describes a improved UVLO circuit which is based on bandgap comparator structure. The major advantages are having a small area without an extra bandgap and the complex digital logic. The threshold voltage of the hysteretic range varies little with the variation of the temperature from -25 ℃ to 125℃. The UVLO can be applied in low power dissipation power management chips. It can be used in many double voltage applications [13, 14].

6. ACKNOWLEDGEMENTS

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