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AN EXPERT SYSTEM BASED SOFTWARE FOR REDUCTION OF SEQUENCE NETWORKS

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ABSTRACT

This paper describes a new Expert System Based Software for Reduction of Sequence Networks. The main aim is to develop a new tool that helps students to reduce the corresponding sequence networks to its simplest form. Reduction of sequence networks is important for power system fault analysis. The equivalent positive-, negative- and zero- sequences are represented as a series and series-parallel combination of per-unit impedance. Reduction process will replaces them by the single equivalent impedance for each sequence network. Using this tool, students will deeply understand the flow of reduction process. Rather than that, the system is capable to examine the sequence network to observe whether it can be reduced depends on the selected fault location. This system applies the expert system concepts during the process. Hopefully this tool will provide new medium in learning and teaching fault analysis besides make it easy and interesting to learn.

Keywords: *Sequence Networks, Network Reduction, Fault Analysis, Expert System*

1. INTRODUCTION

A Graphical User Interface (GUI) permits students to visualize the effect of parameter changes on the system being studied. GUI provides interactive and comprehensive interfacing in learning process. The fact is that graphical solutions give insight information about the studied system very quickly without the need of a rigorous analysis. This will allow students to spend more time in analyzing the results obtained.

In the new era of educational technology, many researches had been done to develop an interactive and interesting GUI based software for learning and teaching power system analysis. Few of the researches are being carried-out on software development for the purpose of fault analysis studies with difference focus area [1-6]. Some focus on teaching the symmetrical components [1, 3], sequence networks [4], but most concentrates on simulation on fault analysis [2, 5, 6]. However, none of them have the ability to simplify sequence networks step by step from different point of fault location.

The main objective of this project is to develop an educational tool to reduce the corresponding sequence networks to its simplest form. This tool will aid students in visualizing the step-by-step

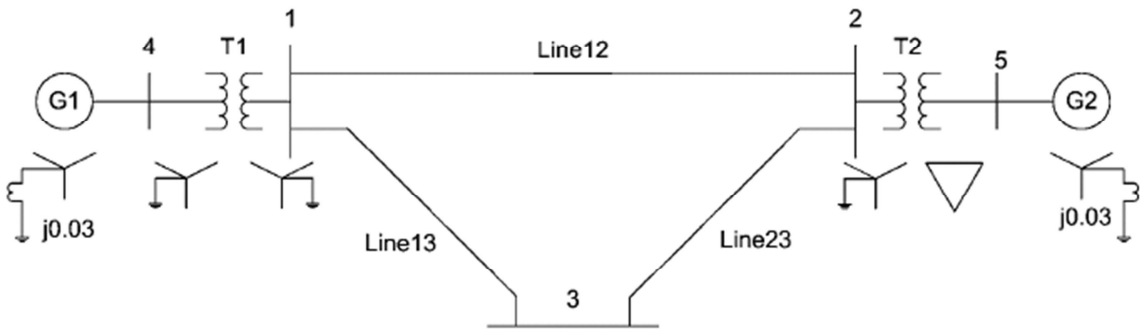

Figure 1:*An Example Of Simple 3 Buses Single-Line Diagram*

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reduction process at different locations without involving lots of mathematical calculations. Therefore, the developed tool must provide an interactive and user-friendly environment and hence applying the advantages of GUI.

2. NETWORKS REDUCTION

Network reduction is a process to obtain an equivalent Thevenin's impedance projection at certain point. Different location will result different impedance value. For shunt fault calculations (three phase, line-to-line, single-line-to-ground and double-line-to-ground faults), each of independent sequence networks can be reduced to a single equivalent impedance. These are commonly designated as Z_1, Z_2, and Z_0 for the respective sequence networks [8].

Reduction method is very useful when dealing with a simple diagram such as examples shown in Figure 1, but it is not suitable for complex diagram. When the degree of diagram complexity varied, it will affect the process of finding the equivalent Thevenin's impedance and required a higher level degree of reduction method such as the matrix reduction. A simple sequence networks normally consist of a series, parallel, delta and/or wye combinations. Therefore, reducing them required the basic theories of series and parallel combination and also delta to wye and wye to delta transformations.

Reducing negative- and zero- sequence networks are straight forward because they did not contain generated voltages and loads as in positive-sequence network. Therefore, the can be reduced using basic reduction method. However, reducing positive- sequence network is a little bit tricky whereby the Thevenin theorem needs to be applied.

3. WYE AND DELTA TRANSFORMATION

Wye (Y) and delta (Δ) transformation is useful in reducing loop-type sequence networks. This transformation normally been used with series and parallel transformations in order to get the Thevenin's equivalent impedance at certain point.

Figure 2 shows the wye and delta diagram. If impedance ZAB, ZBC, and ZCA are connected in delta, the equivalent wye impedances, ZA, ZB, and ZC are given as,

$$Z_A = \frac{Z_{AB}Z_{CA}}{Z_{AB}+Z_{BC}+Z_{CA}} \quad (1)$$

$$Z_B = \frac{Z_{AB}Z_{BC}}{Z_{AB}+Z_{BC}+Z_{CA}} \quad (2)$$

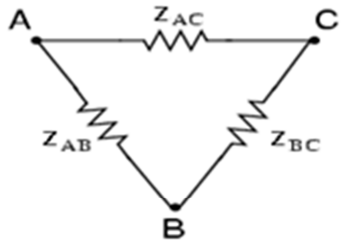
$$Z_C = \frac{Z_{BC}Z_{CA}}{Z_{AB}+Z_{BC}+Z_{CA}} \quad (3)$$

If we want to convert the known wye connected impedances, ZA, ZB, and ZC to it equivalent delta impedances, the convenient equations to be used are

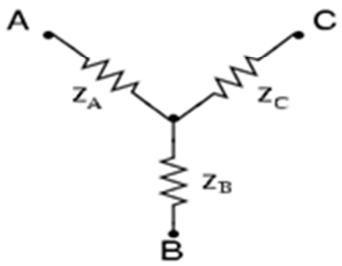
$$Z_{AB} = Z_A + Z_B + \frac{Z_A Z_B}{Z_C} \quad (4)$$

$$Z_{BC} = Z_B + Z_C + \frac{Z_B Z_C}{Z_A} \quad (5)$$

$$Z_{CA} = Z_C + Z_A + \frac{Z_C Z_A}{Z_B} \quad (6)$$



Delta (Δ) Network



Wye (Y) Network

Figure 2: Delta And Wye Network Diagram

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4. DESCRIPTION OF THE SOFTWARE

This software is written in Microsoft Visual Basic 6.0 (VB6) language and standard Windows functions and features are included. Figure 3 shows some of the GUI features in this software package. In this software, user can visualize the step-by-step reduction process of sequence networks. However, user must select the faulty bus or starting point before continues to reduction window or otherwise system will indicate an error. For example diagram as in Figure 1, bus 3 is selected as a faulty bus. The step-by-step reduction can be done in two ways, either manually or automatically. Both processes can be selected using an appropriate buttons located on the right-bottom side of the window as shown in Figure 3.

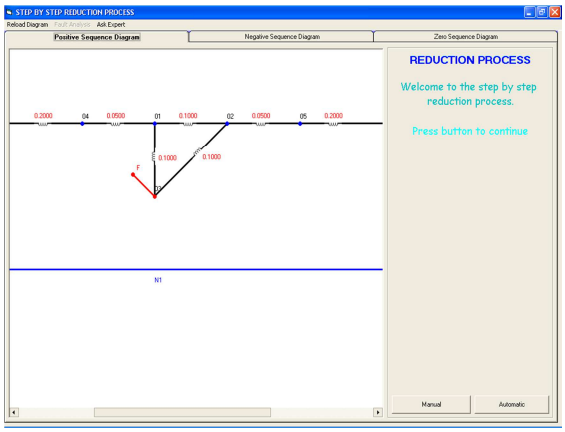


Figure 3: A Window For Step-By-Step Reduction process

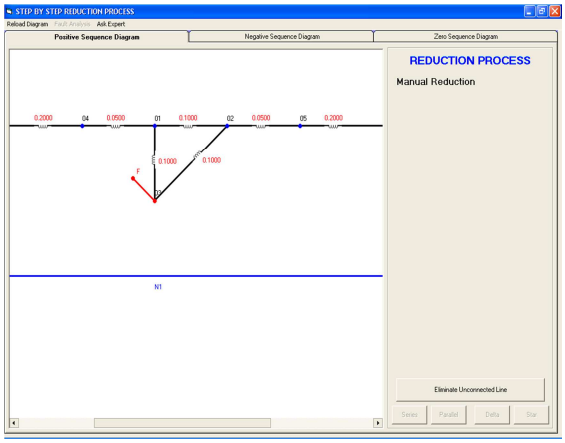


Figure 4: GUI For Manual Reduction Process

The developed software has a capability to reduce a simple diagram as shown in Figure 1 by applying four basic reduction rules; series, parallel, *wye* to delta and delta to *wye* conversion to obtain reduction

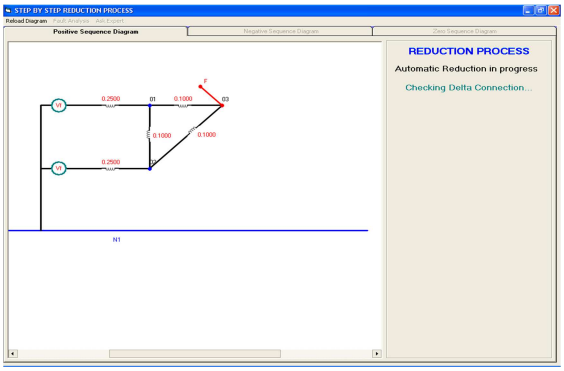
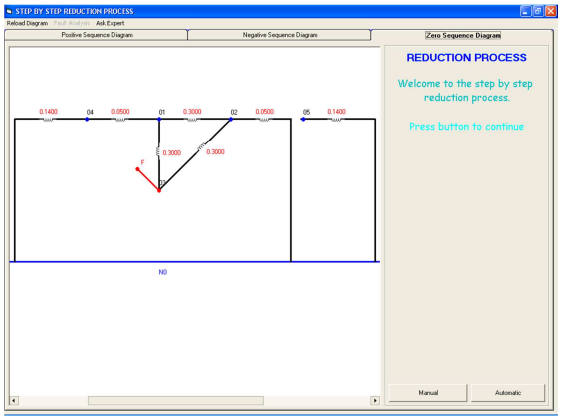
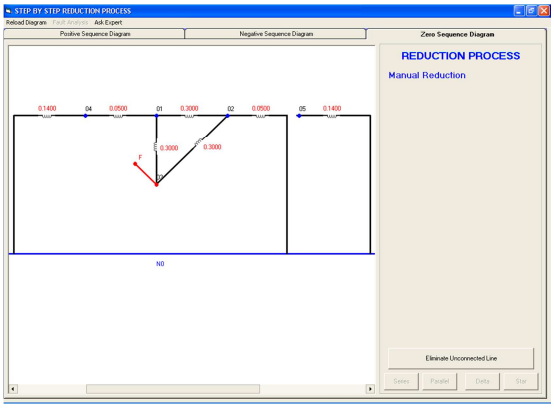


Figure 5: GUI For Automatic Reduction Process

impedance value for every sequence. It utilizes build-in intelligent system engine to recognize the availability of four types of connection, series, parallel, *wye*, and delta. After that it will wait until user select types of connection need to be converted. This routine will be continued until all the final result been produced. This procedure is call as manual reduction process. Figure 4 shows the startup window for manual reduction process.



Step 1



Step 2

Figure 6: Step-By-Step Reduction Process For Zero-Sequence Network

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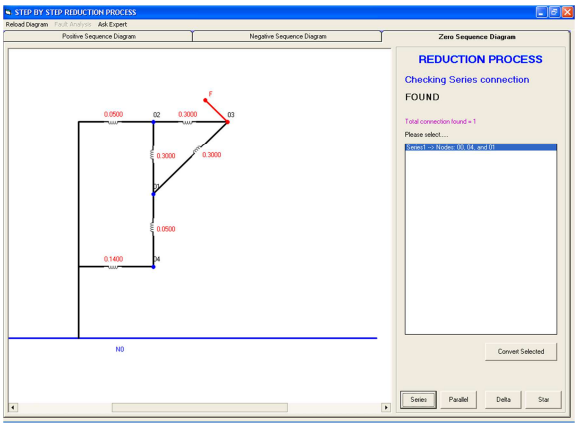
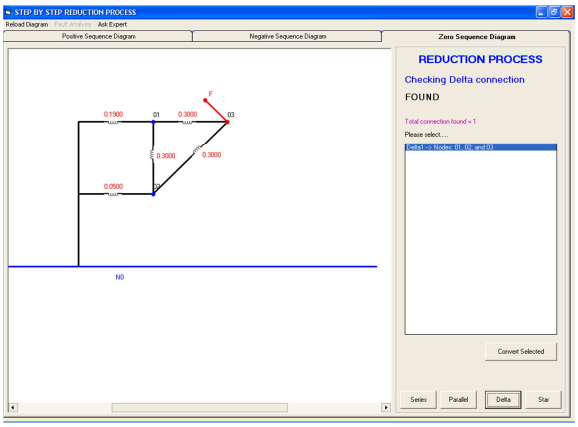
Besides of doing everything manually, user can let the software to perform the reduction process by itself. This procedure is known as automatic reduction process. This option will allow diagram to be reduced step by step animatedly using it standard flow. This process is useful when user only need to obtain the final result without concerning on how the diagram being reduce or the way it been reduced. Figure 5 shows the startup window for automatic reduction process.

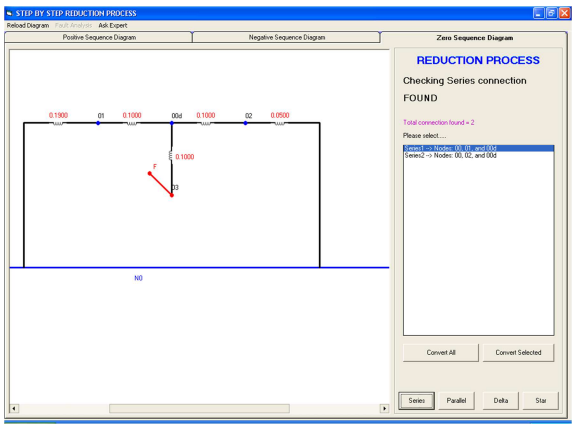
This software also has built-in intelligent system engine that will help users to evaluate the current reduction process. This engine is similar to expert system engine will give suggestion whether the diagram can be reduced or not at a selected point. Rather than that, users can request the system to



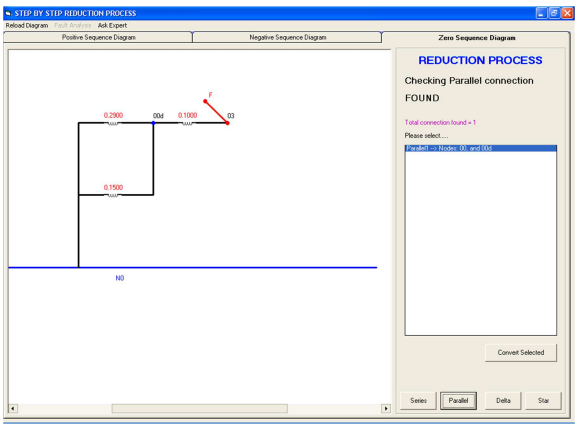
Step 3



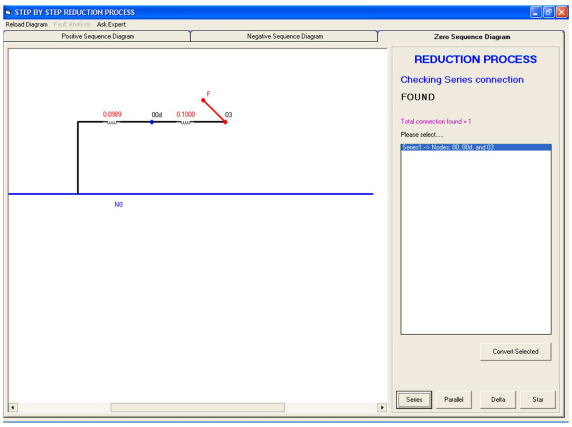
Step 4



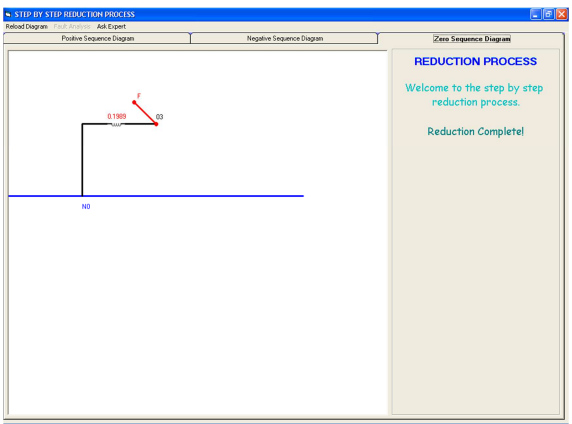
Step 5



Step 6



Step 7



Step 8

Figure 6: Step-By-Step Reduction Process For Zero- Sequence Network (Continue)

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evaluate the whole diagram and provide suggestion which point or location where the reduction process can be continued.

When selecting manual, the process will let users to exploit different combination of reduction rules as to acquire final result. Figure 6 shows step-by-step reduction process for zero- sequence network using manual reduction process. User can recall an original diagram using menu "Reload Diagram". The equivalent Thevenin's impedance values for all sequence networks using this software is shown in Figure 7.

5. CONCLUSION

A GUI based software package to facilitate the learning and teaching fault analysis was developed. This software is written in Visual Basic 6.0. This software reduces the corresponding sequence networks to its simplest form. In this software, students are able to view the flow of reduction processes. It enhances the understanding the network reduction process. Hopefully, this software will provide a comprehensive and interactive environment to aid students in understanding and learning the network reduction and fault analysis.

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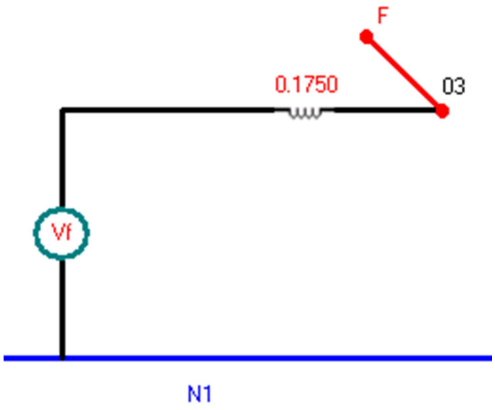
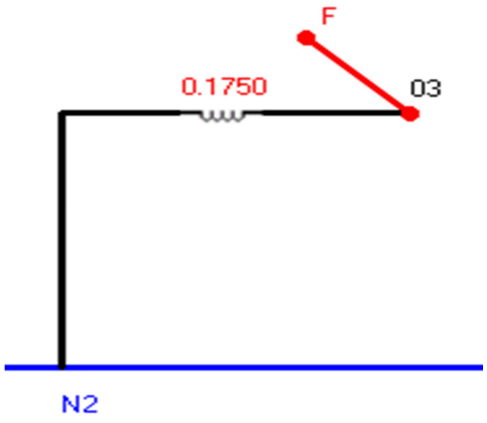
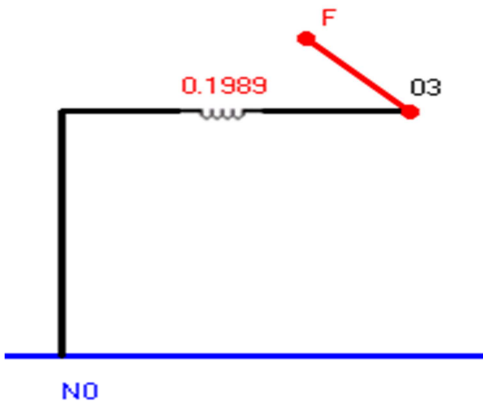


(a) positive- sequence impedance



(b) negative- sequence impedance



(c) zero- sequence impedance

Figure 7: Equivalent Thevenin's Impedance For All Sequence Obtains From Step-By-Step Reduction Process

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