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A MULTI-CHANNEL SIGNAL SOURCES BASED ON FPGA AND DDS

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ABSTRACT

In the field of Test & Control Instrument , multi-channel signal sources are needed as the excitation in the electrical parameters measurement. This paper presents a realization method of multiplexed signal source which combined the advantages of DDS principle with high speed programmable logic device FPGA, fully reflect the characteristics of fast switching frequency, high precision with DDS technology, and abundant FPGA logic resources. This design realized the optimization of DDS resources primarily through FPGA, made use of timing multi-threaded design ROM shared access, innovated an adjustable amplitude method, namely, applied FPGA internal procedures to modulate the normalized waveform sampling digital.

Keywords: *Multi-Channel, DDS, FPGA, ROM Shared Access*

1. INTRODUCTION

Test & Control Instrument is a general test platform gathered with the digital quantity converter test stand, instructions converter test stand and telemetry remote control system test stand. Its main purpose was providing the basis to detect accuracy and reliability of telemetry converter. The test platform was one large application equipment gathered with signal generator, automatic detection, automatic measurement and data analysis [1, 2]. The core of the missile equipments is the digital quantity telemetry converter, the instructions converter and the comprehensive measuring controller. Its main function is controlling all kinds of received flight parameters and different kinds of operation instructions on the aircraft. This system had been successfully applied to a certain type of aircraft field test, which performance and function index were much better than the application requirements [3].

2. DESIGN OF THE SIGNAL SOURCES

The signal source combination of the DDS technology, the advantages of LVDS bus technology and the FPGA-programmable features, and give full play their own advantage. In this way, it can achieve a real-time control signal source and the precision as well as multi-channel parallel output of function at the same time.

The block diagram of the multi-channel signal source is shown in Figure 1, the users' control commands and the waveform parameter data is send to the master card through the USB bus by the host computer, then the commands and data are forwarded to the signal source module through the back plane LVDS bus by the master card. The transmission of the command and the data in the signal source module transferred to the FPGA decoder followed serial-parallel conversion by LVDS interface, the purpose of selection LVDS is to achieving the board-level control.

Hardware, 32-channel signal of the signal source output points four same functions and hardware units to achieve the output and per unit outputs 8-channel waveform. Each unit constructs the waveform reconstruction circuit by a 16-bit high-precision D/A converter AD768 as the core, following a 8-channel signal conditioning circuit to achieve the requirements of the amplitude amplification and the offset. A multi-channel analog switch ADG1208 is used to achieve the selection of 8-channel signal output, and the various quarters mixed with analog signals switch

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to the respective channel to realize one-to-many switching. The sample and hold circuit is to ensure that the voltage value of each channel will not reduce in the switching process. The DPST switch ADG333A is the main device to constitute the output edge time of the rectangular wave circuit. After the output high and low, controlling switch to switch can output the corresponding rectangular wave. And the latter ADG333A, which also has a very important function, is to realize the choice of waveform filtering or not. In order to prevent containing high frequency components of the triangular wave and saw-tooth wave distortion through the filter circuit, and also need to ensure other signal output waveform smoothing, a DPST switch ADG333A is selected to achieve the final signal output .

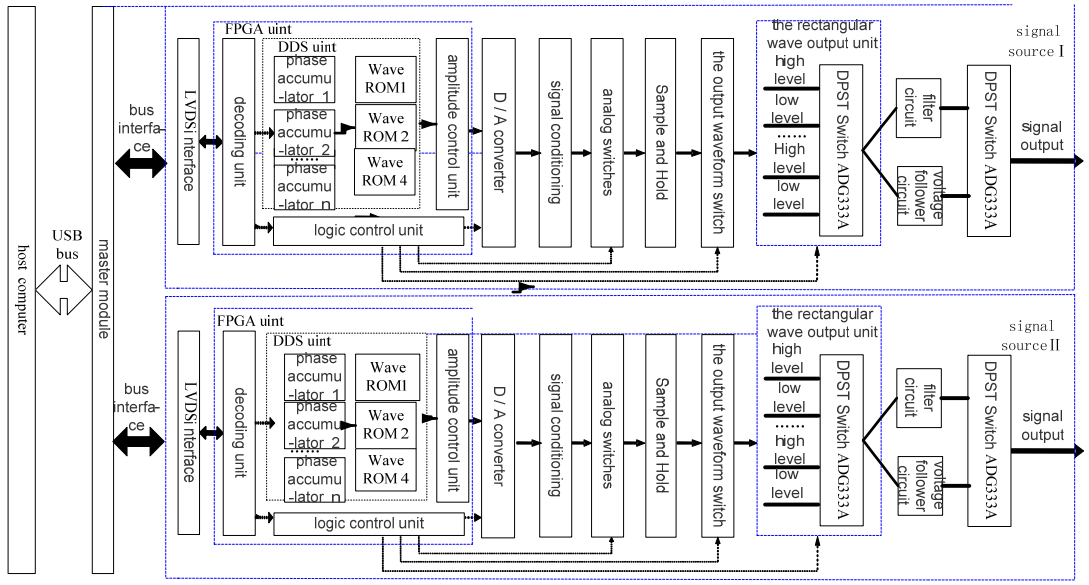

Figure1. The Schematic Block Diagram Of The Signal Source

From a procedural point of departure, Different control commands issued by the host computer when the source starts, the signal source module receives the LVDS serial data and transfers these data to FPGA to analyze after desterilizing. The part of DDS completed in the FPGA, and design ideas reference to the pipeline seamless access. ROM1 and ROM4 store normalized waveform sampling digital of sine wave, triangle wave, saw-tooth wave, square wave respectively. Addressing of 32-channel signal all share the same set of waveform ROM. Improved resource utilization to the maximum extent is possible, and achieve the data stream does not have time to pause to the data stream of the lower-level processing module, so we can achieve the maximize seamless buffering and processing of the data. In order to realize amplitude adjustable, the normalized waveform sampling digital is converted into the desired amplitude waveform digital in the FPGA and then is transferred to the D/A converters for digital analog conversion. This method is more flexible, high scalability, and the design of the hardware cost is also low.

A direct digital frequency synthesizer (DDS) consists of the frequency control word, the phase accumulator, the waveform storage ROM and the D/A converters and the low-pass filter [4, 6]. The basic principle of the DDS is based on Nyquist sampling theorem, the collected analog signal acquisition store into the waveform memory after quantization. The waveform data is outputted by the addressing look-up table, and then by the D/A converters and the low-pass filter can be restored the original waveform; the process of the realization is shown in Figure 2. In the design, the phase accumulator and the waveform memory are realized by the program instantiation inside FPGA. And the D/A converter, the low-pass filter are realized by an external high-precision DAC and the second-order RC filter circuit. The following will introduce and analyze the DDS implementation in the FPGA.

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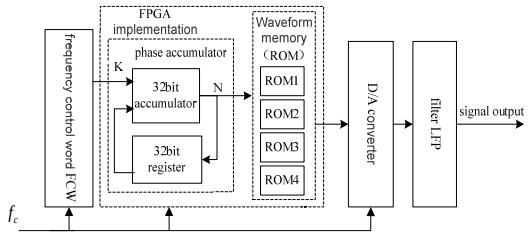

Figure2. A Block Diagram Of The Basic Principles Of DDS

According to the DDS equation:

$$f_0 = K \times \frac{f_c}{2^N} \qquad (1)$$

Where refers to the output frequency, refers to the clock frequency. Shows that when K = 1, the minimum frequency of the DDS system output signal is , that is, the DDS's frequency resolution. Based on the Nyquist sampling theorem, the maximum output of the DDS frequency is in theory.

We can see the maximum value of K can be taken to . Formula. 1 shows that DDS can be a very small frequency interval in the case of the unchanged systematic frequency as long as N is large enough. Considering the requirements and the parameters of the design comprehensively, the system clock of the entire internal FPGA is 120M in this article, but the clock of the DDS process is 46290Hz, and N is 32 by calculation and analysis. Suitable for the DDS equation of the design is as follows:

$$f_0 = 1.078 \times 10^{-5} K \qquad (2)$$

Formula 2 shows the size of the output frequency is determined by the frequency control word. In the design, according to the output frequency, the host computer issued accurate frequency control words, so as to achieve the functional requirements of real-time configuration of the frequency parameter. The maximum value of K can take, and a total maximum output frequency is 4.6289MHz, and then assigned to each channel maximum frequency of 32-channel outputs is 1446.5 Hz.It is bigger than1000Hz. It can meet the design requirements.

Figure 2 shows that, in order to achieve the corresponding relations of the phase and the frequency conversion, the phase accumulator consists of a 32-bit adders and 32-bit registers in FPGA. In the system clock, adder accumulate control word K of the input frequency after complete the calculation, and the results are temporarily stored in the register. For the next-accumulate operations, the store results are fed back to the other output of the adder, resulting in the addressing address of the waveform ROM. Again and again until the accumulator reaches its full scale, it will produce an overflow to complete a cycle of the action. Especially to be noted that, in order to ensure that the frequency resolution to meet the requirements, the number of bits of the accumulator take 32 bits, while the capacity of the wave ROM can not be achieved the same with the accumulator. So the address of the accumulator output need for phase truncation when addressing, and take high bit as the calling address, where the truncated data bit is decided by the waveform ROM capacity.

The wave ROM is essentially a saved waveform information memory, while addressing the address is the high truncated data of the phase accumulator output. For example, the wave ROM stores 28 sequence of sample values of one complete cycle of the signal, and these sample values are actually the signal amplitude for the 16-bit binary data. Therefore, the corresponding amplitude of the signal can be output in accordance with the addressable address. In this way, we can achieve the corresponding conversion of the phase and the amplitude of the waveform.

3 DESIGN OF SHARED ACCESS TO WAVE ROM

Generally, the DDS signal source is achieved by FPGA. The common method of the design is that each channel is configured with the independent accumulator and the waveform ROM, and it is shown in Figure 3.

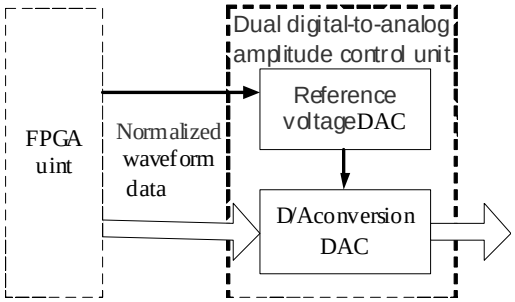

Figure3. The General Method Of Achieving DDS By FPGA

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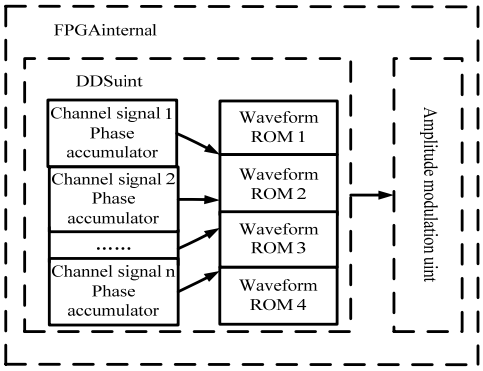

Figure4. The Optimized FPGA Internal Access Way

The waveform ROM usually stores the signal sample values of a complete cycle, of course, some of the design proposed to use 1/4 waveform storage method, that is to say, when the waveform is symmetrical, the wave ROM stores the waveform information of 1/4 cycle instead of the entire cycle, and then using the addressing changes to generate the complete waveform cycle [9, 10]. Whatever the storage method is , when a lot of ones of the signal source designed, a huge number of the phase accumulator and the waveform ROM will occupy a large part of the FPGA resources, and cause a large burden on FPGA. Therefore, how to allocate the limited resources has become a very critical design challenges.

In view of the above analysis, the way of ROM shared access is proposed to improve the rational utilization of resources in this paper. According to the requirements of the mission, AC signal of the signal source output should be five types, they are the triangle wave, the sine wave, the saw-tooth wave, the square wave and DC[9, 10].. DC does not need to individually configure waveform ROM. So the internal design of FPGA instantiate four waveform ROMs by IP Core to store four kinds of normalized sampling digital of the waveforms. Simultaneously, the phase accumulator of 32 generated share the four waveform ROMs in different time periods which is similar streamlined access. So we can reasonable use FPGA internal resources in the maximum degree, as is shown in Figure 4. Only one signal waveform addressing is effective at the same time, and the time of the waveform addressing in FPGA can be achieved by a system cycle generally. After a channel signal address completely and then the data is sent to the subsequent processing, the waveform ROM is idle state now and the next signal addressing can operate. Other channels are similar.

4 DESIGN OF PROGRAM-CONTROLLED AMPLITUDE MODULATION

At present, there are two amplitude adjustment methods of the DDS signal source. First, the normalized waveform samples values of different amplitudes are directly burned into each register, and then be converted to the waveform of the required output through DAC. Although this method is easy and intuitive, because of the limited number of registers it is impossible that the design of the source amplitude modulation is flexible as a small stepping and adjustable range [7, 10]. Secondly, the design of the amplitude modulation can be realized by multiple DAC nested in the hardware providing a reference voltage, as is shown in Figure 5, the amplitude of the output signal is controlled by adjusting its reference voltage in the DAC conversion process. The first DAC is used to convert the waveform sample value of the output of FPGA to the analog stepped signal. And the amplitude adjustment is achieved by the controlling output of the second DAC to change reference voltage of the first DAC real-time. It can be seen that this method is the high cost of the hardware, the complexity of the design process, and anti-jamming. In particular, the output of two DAC is affected by the peripheral circuit. Only when the resistors' and capacitors' precision need to meet the very high accuracy can the output signal is in the error range.

Therefore, the design presents the idea of the programmable amplitude adjustable based on FPGA. That is to say, the digital of the normalized waveform convert into the desired digital in FPGA, and then passed to DAC for the digital-analog transformation, as is shown in Figure 6. This amplitude modulation makes use of non-linear relationship of the periodic signal sampling digital, and does the data processing in FPGA. Although the speed of FPGA computing processing is not the best, we try to simplify the process of the data processing by accurate calculation with the hardware.

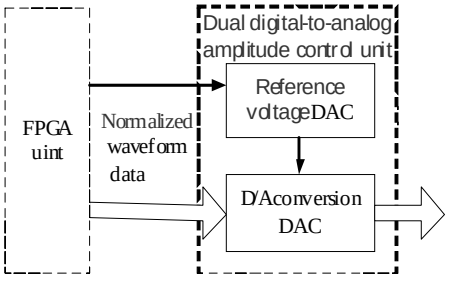

Figure5 The General Method Of Amplitude Modulation

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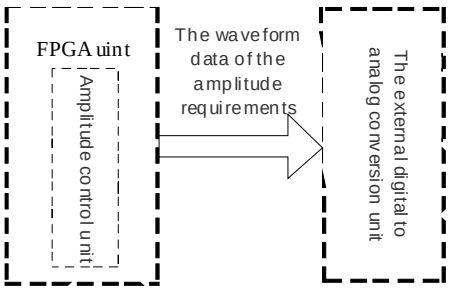

Figure6 The Amplitude Modulation Method Of The Signal Source In This Paper

Only need to call the IP Core of FPGA can be achieved flexibly to adjust the amplitude. And this don't cause logical burden. This method of the programmed amplitude modulation can achieve regulation with the small stepping and fast speed. It has better flexibility, extendibility and adaptability, and cost of the design is cheaper. So this method is more suitable for the design of the multi-channel signal source.

5 CONCLUSION

In the digital telemeter system (PCM), the channel transmission made use of the binary code sequences, insert the frame synchronization was easy to signal identification and extraction, and should be different to normal signal encoding remarkably and could reduce false synchronization and leakage synchronous probability. The frame synchronization adopted by the actual use telemetry system is EB 90 (11101011 10010000), and a child frame synchronization code is 14 6F (0001010001101111), which is the inverse code of the frame synchronization. ① and ③ in Fig.5 is the actual measurement pulse waveform measured by the oscilloscope, In Fig.5② is 422 data sources and in Fig.5④ is the measured switch quantity wave.

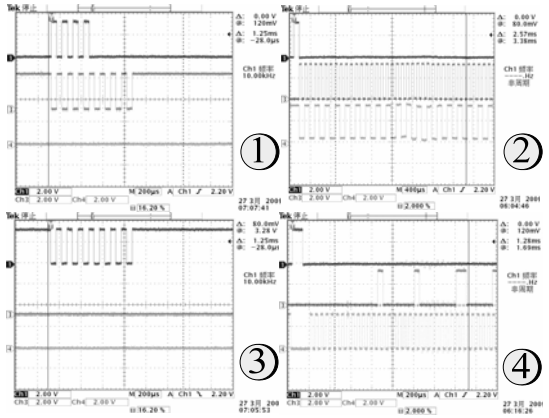

Fig.5. ①Pulse Signal ②422 Data Source ③Pulse Signal ④Switch Signal.

The PC writes the data acquisition application programs with VC++ and realizes the waveforms of the analog real-time display; one of the realization of Variable Frame PCM Telemetry System is shown in Fig.6.

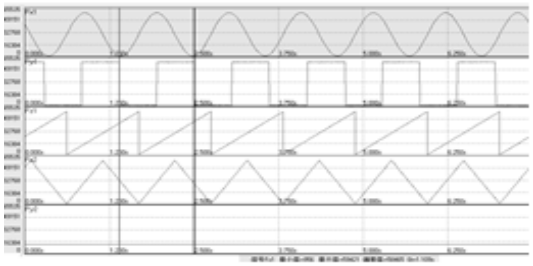

Fig.6. PCM Reconstruction Waveform And Actual Wave Contrast Figure

Through the online testing with the system, all kinds of the data sources fully meet the requirements of the system. At present, the system has been successfully applied to a certain type of the aircraft field test, its performance and function index are much better than the application requirements.

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