Journal of Theoretical and Applied Information Technology
15th November 2012. Vol. 45 No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

DESIGN AND IMPLEMENTATION OF A HIGH-SPEED DATA ACQUISITION TOMOGRAPHY SYSTEM

BIN CAI, BIN WANG
[1]Wuhan University of Science and Technology, Wuhan 430081, China

ABSTRACT

In order to implement online real-time non-destructive detection of turbine fluid distribution and the internal operation of the rotating machinery, we designed a high-speed data acquisition system based on PCI7300A and a high speed microcontroller—UBICOM. It is also for a further goal of carrying on graphical fault diagnosis and fault-tolerant control. This paper describes the system structure and introduces the methods used to implement the system, as well as the design concept and the principle of this program. The practical application showed that the system can realize online real-time collection of tomography projection data, and the acquisition speed can be up to 80M bit/s. Thus non-destructive testing of a rotary mechanism with a high rotation speed of 5000 r / min could be achieved.

Keywords: *Non-Destructive Testing, Fault Diagnosis, Fault-Tolerant Control, Data acquisition, Real Time*

1. INTRODUCTION

With the rapid development of industry, tomography imaging technology is known as the best non-destructive testing technique, since it clearly, accurately and intuitively showed the structure, composition, materials and defect status of the detected objects in the form of two-dimensional tomography image without any damage [1, 2]. In the past few years, Department of multiphase fluid dynamic testing in Rossendorf Research Center researches and develops a gamma-ray tomography detection system[3]. Similar to medical tomography scan, the detection system obtains the gamma - ray attenuation coefficient distribution of the detected object firstly, and then measures integrated attenuation from different angles, and finally uses the computer for image reconstruction[4]. This system has been identified to be applied in the detection of axial motors and turbines. To achieve a high resolution of the detection, a detector bow with 320 detection units has been established[5].

By using the existing data acquisition circuit, one detector unit can complete a data read in a time interval of 1ms. It will inevitably bring about the large amount of data while using a smaller volume of the sensor to achieve high resolution detection image[5]. For high-speed rotating machinery, to meet the demand of the real-time online testing, high-speed data acquisition has become a must to achieve the target. To be able to study detection of faster rotating machinery, such as turbines with a work rate of 1500 r / min, the existing data acquisition circuit can no longer meet the requirements[6]. Therefore, a tomography data acquisition system must be developed, and software programming should be made in accordance with the appropriate communication protocol[7].

2. STRUCTURE OF THE SYSTEM

In this set of CT scan NDT system, the Cesium 137 gamma-ray is used as radioactive sources, and its radiation ray angle is 44°[5]. As is shown in Fig 1, when the gamma-ray, which is sent out by ray source, passes through the measured turbine, it will be absorbed by a detector bow consisting of 320 units, and the pulse waveform is processed by subsequent conditioning circuit. After passing through the measured object, the gamma ray will produce different levels of attenuations depending on the material. And these gamma rays with different levels of attenuations will make different quantum numbers after passing through the detection circuit. With the received quantum numbers, we can get a ray projection of alternating lightness and darkness. When the turbine is rotating, there will be a lot of ray projection on a plane. The projection data is sent to the computer by data acquisition; the image reconstruction of the cross-section is completed based on the projection data. In order to ensure that the effective ray projection is received and the ray passing through the measured object is detected by detector unit, the measured turbine should be placed within the fan-shaped sector of gamma-ray source and detector bow[8].

Journal of Theoretical and Applied Information Technology
15th November 2012. Vol. 45 No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

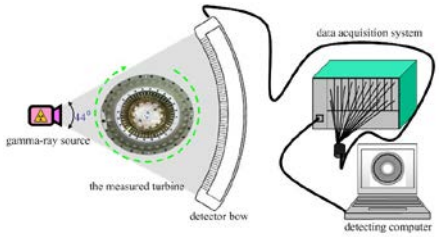

Figure 1: Composition Figure Of The CT Scan System

On a single detector unit, the detected gamma-ray is a quantum sequence whose energy is gradually weakening. Each detected gamma quantum will produce a voltage pulse. Through a pulse shaping and preamplifier circuit, Gaussian voltage pulse waveform with pulse width of 0.5ms is shaped to produce a voltage pulse during 1μs time's interval at most. The size of the amplitude of the voltage pulse reflects the size of the gamma-ray's energy hit in the detector unit[5,9]. When the voltage pulse passes through a window comparator, a counting circuit will count the voltage pulse which has exceeded a definite amplitude. If the voltage pulse exceeds the setting value, the count will add one; otherwise the number will remain unchanged.

The single counting circuit is composed of a 24-bit binary counter and a shift register which is parallel input and serial output. The role of the shift register is to store the number of pulse and output serial data. The entire counting system consists of ten count cards, and every count card includes two FPGAs, each of which is connected with 16 detector units. Each detector unit includes conditioning circuit such as pulse shaping, preamplifier and window comparator. Then the composite circuit and the digital signal circuit of 320 detector units are connected to computer through the 16-bit bus interface. All of the digital logic is implemented through FPGA. This means that the FPGA is to complete the function of voltage pulse counting of each detector unit[7,10].

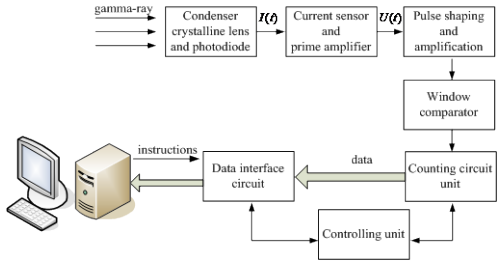

Figure 2: Block Diagram Of Data Acquisition System

3. HARDWARE DESIGN

3.1. Requirement Analysis

As the measured object, maximum speed of the turbine is 1500 r/ min; in other words, 25 per second. When tomography image detection is underway, the measured turbine and tomography system must rotate relatively. In order to achieve the synchronization of rotation and projection, an angular position sensor is installed in the detector bow. When the turbine rotates every 0.36^{o}, it will send a logic pulse to data acquisition system, requesting to complete a projection data acquisition. Therefore, the existing detection system, in order to complete the tomography measurement which synchronizes with the rotation angle, must complete 1000 projections in a time interval of one rotation; namely, 25,000 projections per second. It means that, the projection period can not exceed 40μs for a single projection. So in 40μs projection period, 40 gamma quanta at most can be got. Then a 6-bit binary number can fully express. The transmission speed of data acquisition system should meet as follows:

$$D_R \geq \frac{6Bit \times 320}{40\mu s} = 48MBit/s \qquad (1)$$

3.2. Interface Configuration

Data interface uses PCI300A，whose theoretical data transmission rate can reach 80 MByte/s. Board contains two16KWords FIFO for DI and DO channel. PCI7300A is connected with the computer through the PCI bus with the external circuit interface based on SCSI-100 interface[11]. PCI7300A has two 16-bit parallel data ports named PortA and PortB for data transmission with an external circuit. These two ports can be configured as a data input or data output. PCI7300A has four kinds of data input and output mode (internal clock, external clock, handshake, sudden shaking). A high-speed microcontroller UBICOM is selected as the logic controller of the counting card and as a data clock of the counting card; the handshake mode is selected as the PCI7300A data transmission mode. In this data acquisition system, the PCI7300A uses DI16DO16 mode; PORTA serves as 16-bit data input port and PORTB serves as a 16-bit instruction output port configuration, but in the system only the low 8 bits is used.

3.3. Design Of Logic Control Circuit

The high-speed microcontroller UBICOM SX52BD is used as the logic controller and RISC architecture is put into use. Its main characteristic is that the instruction cycle and machine clock cycle

Journal of Theoretical and Applied Information Technology
15th November 2012. Vol. 45 No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

is equal and it can operating at 75MHz machine clock frequency with five 8-bit I/O ports. When debugging, the maximum operating current of UBICOM SX52BD is 250mA, so the voltage module L7805CV (+5V) which can provide 1A working current and100nF tantalum capacitor are used as a regulated power supply. 10 kΩ is selected as a reset resistance. In order to ensure the long-term stable operation, a heat sink is additionally installed in UBICOM SX52BD.

3.4. Bus Design

The data acquisition bus block diagram is shown in Fig 3. The data acquisition unit has two interfaces. A 64-pin interface is used to connect counting cards bus while a SCSI-100 interface is used to connect PIC7300A. Each bus is described as follows:

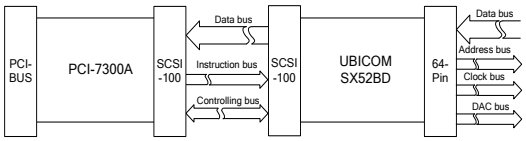

Figure 3: Block Diagram Of Data Acquisition Bus

Data bus: 16bits, used to transmit FPGA data in the counting card to the computer.

Instruction bus: 8bits, used to transmit detecting computer instructions to the logic controller UBICOM.

Controlling bus: 7bits, used for the communication and control between the host computer and logic controller.

Address bus: 5bits, used for the chip selection among 20 FPGAs by the logic controller.

Clock bus: 7bits, used to provide communication protocol control signals and clock signals when data is transmitted to FPGA.

DAC bus: 3bits, used to initialize the window comparator threshold in the detection unit through FPGA.

In addition, the interfaces on PCI7300A, DI_TRG, DI_REQ, DI_ACK,DO_TRG, DO_REQ and DO_ACK, are connected with UBICOM respectively for measuring data input trigger, data input request, data input response, data output instruction trigger, instruction output request and output response.

4. SOFTWARE DESIGN

4.1. Communication Protocol

When the data acquisition system is running, the logic controller (UBICOM) receives a specific instruction from detecting computer. Then, UBICOM sends Gamma quantum number in every detector unit to FPGA of corresponding counting card. At last, UBICOM sends data of FPGA to detecting computer according to the specified sequence. We write programs of UBICOM and Linker programs of PCI7300A. In this data acquisition system, when detecting computer transmits instructions, PCI7300A will use the handshake protocol. When detecting computer transmits data, PCI7300A will use external clock protocol.

4.2. Writing Of Pci7300a Linker Program

This linker program has two functions: 1. Sending instructions of detecting computer to UBICOM in logic control card. 2. When system receives data from counting card, UBICOM offers clock signal. Programming Software is Borland C++ Builder while dynamic link library file is PCIS-DASK. The program flow chart is shown in Fig 4 as follows:

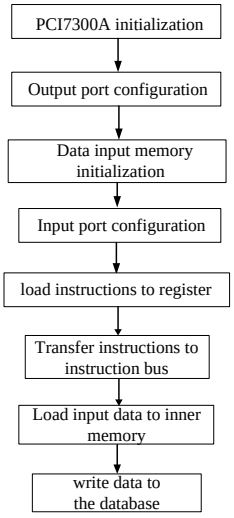

Figure 4: The Linker Program Flow Chart

4.3. Programming Of Buicom

Five 8-bit I/O ports of UBICOM SX52BD are respectively set up as follow:

PORTA	Address bus
PORTB	Data bus
PORTC	Clock bus
PORTD	DAC bus
PORTE	Controlling bus

Instructions sent by detecting computer are classified into two parts, the clearing counter and data transmission instructions. The logic controller program flow chart of UBICOM is shown in Fig 5. Projection cycle is no more than 40us. The number of voltage pulses of every detector unit is no more than 40, and it can be expressed in 6-bit binary

Journal of Theoretical and Applied Information Technology
15th November 2012. Vol. 45 No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

number. Every FPGA storage data is 6-bit binary number corresponding to 16 detector units. FPGA sends a frame of 16-bit data to detecting computer each time via 16-bit data bus and it takes 6 frames to transmit the data in one FPGA[12]. There are 20 FPGAs, so the 6-frame data needs to be transmitted for 20 times altogether.

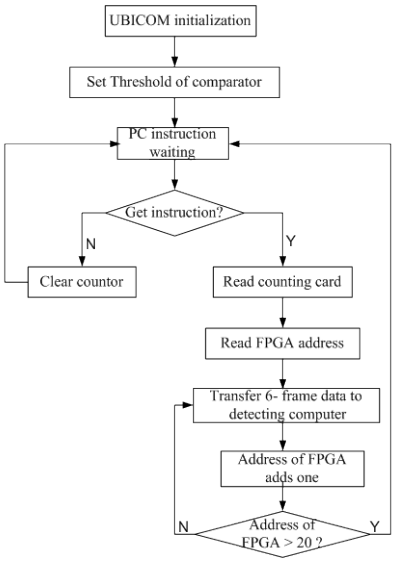

Figure 5: Logic Controller Program Flow Chart

5. DEBUGGING AND OPTIMIZATION

5.1. System Debugging

The layout plan of system debugging experiment with a counting card is shown in Fig 6. The detecting computer is connected to a counting card through the baseplate data acquisition system; the interface is a 66-pin bus. The system uses signal generator to simulate the signal sent to the counting card by the detector unit. Signal waveform of UBICOM is observed by the oscilloscope[13]. After receiving data in the counting card, measuring computer stores data in the hard disk. The signal generator is connected to 0 # wire of 0 # FPGA. The number of pulses issued by the signal generator will be stored on a counting card, and the data acquisition system is transmitted to the detecting computer via 0 # wire of the data bus. The data acquisition system will firstly transmit the MSB (most significant bit) and then LSB (least significant bit). The data will be transmitted to the detecting computer, as is showed in Fig 7, when 0 # wire receives 11 pulses from 0 # detector unit.

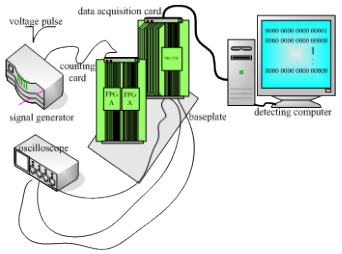

Figure 6: The Layout Plan Of System Debugging

Daten 5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	LSB
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Daten 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MSB

Figure 7: Transmission Charts Of Simulation Data

When the data is transmitted from a single FPGA to the PC, timing waveform of UBICOM control pin is diagrammed in Fig 8. Among them, the FPGA-Address: conducting chip selection of FPGA. Tri_State: triggering FPGA, and make the data read enable (active low). The interface of PCI_DI_REQ: input clock for PCI7300A data. Shift-Clock: FPGA outputs shift clock for the next frame of data.

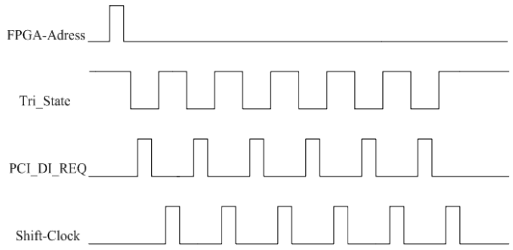

Figure 8: Timing Waveform Diagram Of UBICOM Data Transmission

5.2. Optimization Measure

The original UBICOM program uses two counters (FPGA address counter and frame counter), and two cycle programs (20 data read to FPGA and single frame data read to FPGA6). The optimization measures and the corresponding optimized projection cycles are shown in Table 1.

Table 1: My Contact Information

Optimization measures	Projection cycle
Remove the counters	41,2 μs
Place the main program and subroutines in the same program page	39,8 μs
Remove the cycle programs	31,69μs(<40μs)

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

No data read error appears after the on-line debugging. It proves that this optimization has been able to meet the needs of the data acquisition system. In the PCI7300A interface program, signal of PCI-DI-REQ is effective on rising edge by default before optimization. Optimized PCI-DI-REQ is set to be effective on signal falling edge, while Shift-Clock is on rising edge, and they share one UBICOM pin. After the optimization measures being taken, the projection time is reduced to 15μs. When the projection period is shortened to 15μs, the number of pulses on each detector unit is less than 15. The number of pulses can be expressed by a 4-bit binary number. Therefore, each FPGA only has four 16-bit data. Optimized picture of the single FPGA data transmission for timing waveform signal of UBICOM is shown in Fig 9. UBICOM uses a 16MHz crystal drive. After these optimization measures being taken, data collection systems and counting cards go through system joint debugging, and the projection cycle is 12μs. No data read error occurs, and the data acquisition system is well positioned to meet the design requirements.

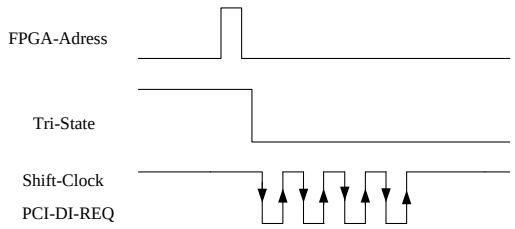

Figure 9: Timing Signal Diagram Of UBICOM With Bilateral Reading Technology

6. CONCLUSION

This paper designs a high-speed data acquisition tomography system based on logic control device UBICOM and data interface PCI-7300A, and provides software and hardware design program. By using optimized measures, especially the bilateral reading technology which reuses the rising and falling edges of a clock pulse, the speed of data acquisition is significantly improved, the cycle time of the entire tomography system could be reduced to 12μs so that it meets the requirements for the turbine detection of 1500 r/min. With the combination of tomography imaging detection system and the developed data acquisition system, we can achieve the imaging detection of turbine whose speed is up to 5000 r/ min, then make further online real-time fault diagnosis study.

REFRENCES:

[1] S. Li, Jianrong R. Luo, Yichun C. Wu, "Continuous and real-time data acquisition embedded system for east", IEEE Transactions on Nuclear Science, Vol.57, No.2, 2010, pp. 696-699.

[2] Martin Christian Hemmsen, Svetoslav Ivanov Nikolov, "Implementation of a versatile research data acquisition system using a commercially available medical ultrasound scanner", IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency control, Vol.59, No.7, 2011, pp. 1487-1499.

[3] Ivan K. H. Tsang, Billy Y. S. Yiu, Dave K. H. Cheung, "Design of a multi-channel pre-beamform data acquisition system for an ultrasound research scanner", IEEE International Ultrasonics Symposium Proceedings, Vol. 52, No. 4, 2009, pp. 1840-1843.

[4] Mykhaylo M. Dorozhovets, Pawel Potyranski, "Data acquisition system and reference model used for the investigation and verification of the resistance tomography system", IEEE Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications, September 5-7, 2005, pp. 36-40.

[5] A. Bieberle, J. Kronenberg, E. Schliecher, "Design of a high-resolution gamma-ray detector module for tomography applications", Nuclear Instruments and Method in Physics Research, 2007, pp. 668-675.

[6] U.Hample, D. Hoppe, K.-H. Diele, J. Fietz, "Application of gamma tomography to the measurement of fluid distributions in a hydrodynamic coupling", Flow Measurement and Instrumentation, 2005, pp. 85-90.

[7] A. Bieberle, E. Schleicher, and U. Hampel, "Data acquisition system for angle synchronized gamma-ray tomography of rapidly rotating objects", Meas. Sci. Technol., Vol. 18, 2007, pp. 3384-3390.

[8] Alexander Mann, Boris Grube, "A sampling ADC data acquisition system for positron emission tomography", IEEE Transactions on Nuclear Science, Vol. 53, No. 1, 2006, pp. 297-303.

[9] Trevor York, Hugh McCann and Krikor B.Ozanyan, "Agile sensing systems for

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

tomography", IEEE Sensors Journal, Vol. 11, No. 1, 2011, pp. 3086-315.

[10] Rolf Clackdoyle, Frederic Noo, Junyu Guo, "Quantitative reconstruction from truncated projections in classical tomography", IEEE Transactions on Nuclear Science, Vol. 51, No. 5, 2004, PP. 2570-2578.

[11] Roger Steadman Francesco Morales Settano, "A COMS photodiode array with in-pixel data acquisition system for computed tomography", IEEE Journal of Solie-State Circuits, Vol. 39, No. 7, 2004, pp. 1034-1043.

[12] S.G. Castillo and K. B. Ozanyan, "Field-programmable data acquisition and processing channel for optical tomography systems", Rev. Sci. Instrum., Vol. 76, p. 95109, 2005.

[13] B. T. Hjertaker, S. A. Tjugum, E. A. Hammer, and G. A. Johansen, "Multimodality tomography for multiphase hydrocarbon flow measurements", IEEE Sensors J., Vol. 5, No. 2, 2005, pp. 153-160.