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ON THE DESIGN OF THE CHARGE PUMP PLL IN VIDEO DECODER

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ABSTRACT

By adopting the 0.35μ2P4M 3.3V standard CMOS technology created by SMIC company, this paper designs a kind of charge pump phase-locked loop (CPPLL) circuit with mixed-signal structure. By improving the phase and frequency detector (PFD), charge pump circuit (CPC), and oscillator circuit design of the PLL circuit, the clock signal used in the video decoder chips can have a more stable performance. The effective tracking range of PLL is 5 MHz ~ 7.5 MHz, the locking output is 6.75 MHz during which the clock jitter is less than 500 ps, the output waveform's duty circle is 50.1408%.

Keywords: *Charge Pump Phase-Locked Loop (CPPLL),Com Metal Oxide Silicon(CMOS),Video Decoder,Phase And Frequency Detector(PFD)*

1. INTRODUCTION

The main functions of digital video signal processing chip are to collect and resize the image in accordance with some requirements, and it can convert the video signals of PAL, SECAM and NTSC into the video format that is compatible with the ITU 601, thus can provide the video source for the video signal digital processing equipments. Rowlock, chroma separation and subcarrier reduction are three core technologies in the signal digital decoding simulation technology. Main functions of the rowlock is recover the exact HSYNC and VSYNC from the input signals, and it will produce the 27 MHz sampling clock which is in line with VSYNC and data as well as the black-out-signal parity field recognition signals. In the digital decoder chip simulation of video signal, the clock signal will be used as the the sampling clock of the front end of ADC module and the processing clock of the back end of the converted digital video signal[1].

2. SYSTEM FRAME OF THE CLOCK IN VIDEO DECODER

In a digital chip, it is common that different modules need different clock signals with different frequency, which can not be provided by the external crystals. Otherwise, the system will be huge and trival, and the area and power consumption of the circuit will be increased. The indirect frequency synthesizer made up of PLL is adopted when producing the high precision, high stability signal clock. The PLL is a phase error control system. By comparing the phase difference between the input signal and the vco output signal, the error control voltage will be produced, and the frequency of the vco will be adjusted, thus to achieve the same frequency of the input signal.

In the video processing chip, there is only a 24.576MHz input clock signal. However, to produce the accurate 27 MHz or 13.5 MHz clock, the phase should be strictly locked with VSYNC(the frequency of the VSYNC is 15.625 KHz or 15.750 KHz). Then, it shows that the clock signal frequency is referred by an input clock and the phase is at the same pace with another low-frequency reference signal. Therefore, the traditional simple PLL structure can not be applied into this research.Motorola company has developed a rowlock PLL that does not use external clock signal, which directly does the phase lock and frequency lock by reference to the color signal, thus produce the internal clock signal that has the same phase with the color synchronizing signal and the frequency is 13.5 MHz's [2]. The engineers in TI also developed a rowlock PLL, by referring to the the locked 27 MHz or 13.5 MHz clock signal of both the external input clock signal and VSYNC[3]. The PLL of the two structures has respective

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advantages and disadvantages. This article, on the basis of various literatures, adopts the figure 1 frame.

The framework includes frontal digital phase locked loop(DPLL), which mainly used to do the line synchronizing pulse contrast and phase discrimination. The backward analog phase locked loop(APLL) can compensate the DPLL's jitter features and and unstable duty circle of the output signal due to its good clock jitter feature. The two levels cascade and common adjustment can make it more stable, and the clock signal more precise. This paper introduces the design of charge pump PLL.

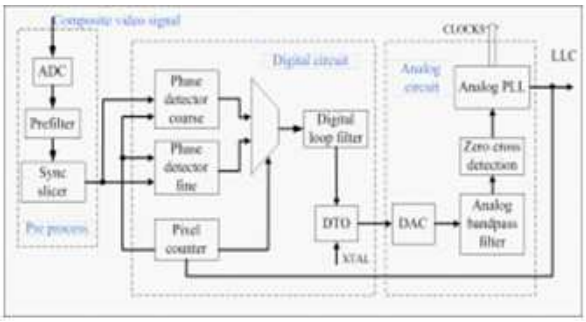

Figure 1 *System Frame Of The Digital Decoder Chip*

3. DESIGN OF THE CHARGE PUMP PLL.

3.1 Structure And Principle Of The System

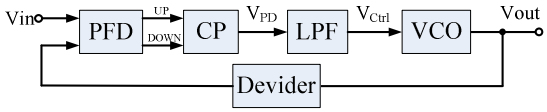

Figure 2 *Framework Of The Charge Pump PLL*

Figure 2 is the realization framework of the charge pump PLL with the frequency range of 5~7.5MHz. Due to the large gap of frequency between the onset feedback clock signal and reference clock, and in order to improve the capture problem, the PLL will detect the frequency in addition to the phrase detection. The largest output PLL frequency is 27MHz, thus the needed PFD speed is less than 20MHz. It has little restriction on working speed, so the common CON-PFD[4] is enough. The charge pump circuits VCO adopts the differential input structure of the amplifier structure, and the pump is controlled by logic control circuit. The VCO uses the four levels annular oscillator as to reduce the noise, meanwhile, it can get the complementary clock signal. The core design frequency of the VCO is 216 MHz. The CPPLL three order open-loop transfer function is:

$$H(s)=\frac{I_P}{2\pi}\frac{1}{N}\frac{K_{VCO}}{s}\frac{1}{(C_1+C_2)s}\frac{R_1C_1s+1}{R_1\frac{C_1C_2}{C_1+C_2}s+1} \quad (1)$$

Make

$$\omega_s=\frac{1}{R_1C_1} \quad (2)$$

$$\omega_p=\frac{C_1+C_2}{R_1C_1C_2} \quad (3)$$

The three order charge pump PLL's open-loop transfer function can be rewritten as:

$$H(s)=\frac{I_P}{2\pi}\frac{1}{N}\frac{K_{VCO}}{s}\frac{1}{(C_1+C_2)s}\frac{\frac{s}{\omega_s}+1}{\frac{s}{\omega_p}+1} \quad (4)$$

Make the ωμ as the units gain bandwidth of the charge pump PLL for the open-loop transfer function , in order to make the margin the biggest, set the zero ωz of the open loop transmission function H (s) is below the ωμ. And set the pole ωp higher than the ωμ with the same scale factor. Then,ωp=Xωμ,C1 、 C2 、 R1 are loop filter parameters and can preliminary work out them to do the system simulation. Among them, the ω p = X ω μ, C1, C2, R1 for loop filter parameters and can be preliminary compute the need to the parameters of the simulation system.

$$R_1=\frac{NX^2\omega_\mu}{\frac{I_P}{2\pi}K_{VCO}(X^2-1)} \quad (5)$$

$$C_1=\frac{\frac{I_P}{2\pi}K_{VCO}(X^2-1)}{NX\omega_\mu^2} \quad (6)$$

$$C_2=\frac{\frac{I_P}{2\pi}K_{VCO}}{NX\omega_\mu^2} \quad (7)$$

In this paper, the three order charge pump PLL will take the input the reference clock frequency as 6.75 MHz, the core frequency of vco output as 216 MHz, the vco voltage controlled gain

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as K_{VCO}=1138×2πMHz/v, charge pump current as 65 uA, the prescaler frequency N = 32. To ensure the stability of the charge pump PLL, and control the ripple of the voltage, the three charge pump PLL will be designed into narrowband PLL. The unit of open loop gain bandwidth is f_u =0.45MHz , ω_u =2π f_u =2.8Mrad/s, which is far less than one tenth of the reference signal frequency. Thus, the three order charge pump PLL can be regarded as a continuous time system. In order to have a certain ring opening phase margins and faster closed-loop to build time, the margin of the phase of the units gain bandwidth in the open loop transmission function will be taken as ϕ_m =51.3º,then the C1=4.845nf,C2=0.6nf，R1=1.38K。

3.2 The CMOS Realization Of Charge Pump PLL

The phase discrimination is an important component of the PLL, which contrasts the frequency and phase between the input signal and internal feedback signal. It's linearity, resolution, phase discrimination bandwidth and phase discrimination sensitivity will directly affect the system performance[5]. This research has no high demand on the PFD speed, so the CON-PFD method is adopted, the circuit implementation is shown in figure 3. It consists of the D triggers which composed by the RS latches, and the reset circuit made up by the SR. In order to eliminate the dead zone of phase discrimination, six SRs and resets are installed to delay. The advantages of this circuit are: no phase discrimination dead zone, the phase discrimination is highly sensitive, and has good linearity.

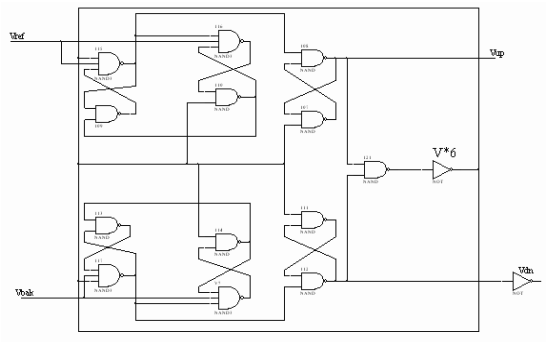

Figure 3 *Schematic Diagram Of PDF*

The charge pump uses similar structure as in literature [6]. In order to realize the dynamic adjustment of the charge pump current, the adaptive charge pump is used. The charge pump and loop filter circuit are shown in figure 4. In order to overcome the charge sharing, the unit gain op-amp will copy the output voltage to the leakage end of the current source in the process of in charge, and discharge[6].

This paper uses the flow control difference ring oscillator. The basic delay unit structure is shown in figure 5. M3 and M4 are load transistors. Difference structure is of high frequency, good common mode noise, environmental noise and the noise rejection capability. The difference delay unit is equivalent to a simple differential amplifier. The reverse loop oscillator has to adopt the odd level unit, thus the circuit will not be locked. But the difference ring vco can use the even level unit. As shown in figure 5, as long as one of the pole being reversed.

The center frequency of the voltage-controlled oscillator is 216MHz, thus the phase discrimination

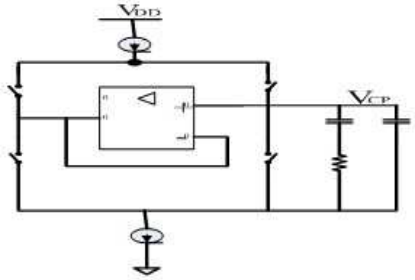

Figure 4 *Schematic Diagram Of Charge Pump And Loop Filter Circuit*

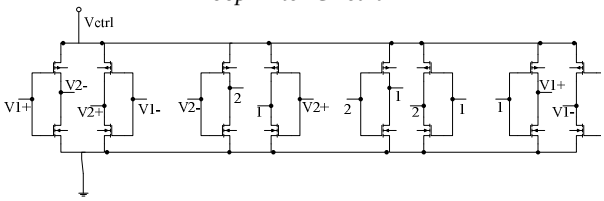

Figure 5 *The Principle Graph Of The Loop Oscillator*

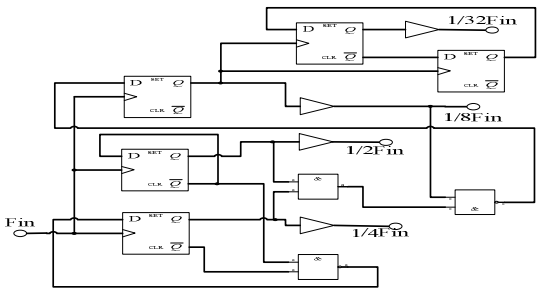

Figure 6 *The Schematic Diagram Of Frequency Dividing Circuit*

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4. SIMULATION AND TESTING OF CHARGE PUMP PLL

The system will mode and simulate in simulink, the simulation picture is shown in figure7, the locking process of PLL is shown in figure8.

Figure 7 *The Simulation Picture Of CPPLL*

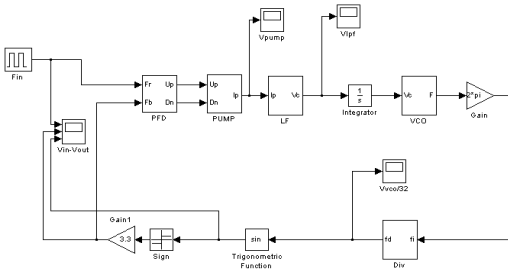

Figure 8 *The Locking Process Of PLL In CPPLL*

The circuit level simulation adopts the Spectre in candence, the output simulation picture of VCO is shown in figure9.

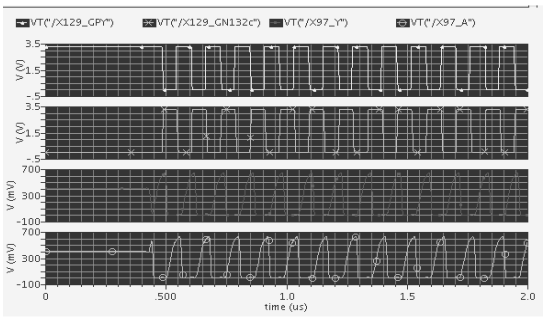

Figure 9 *The Oscillator Output After Reshape*

The simulation results of phase discrimination, frequency divider output and charge pump output are shown in figure 10,11 and 12.

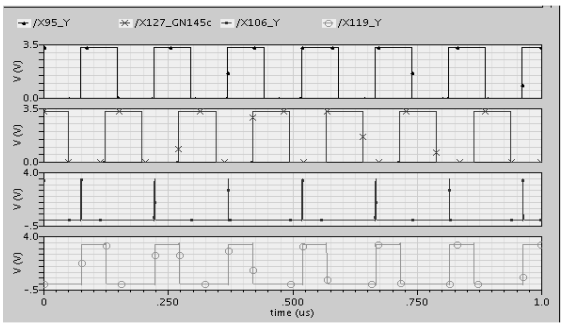

Figure 10 ***T****he Simulation Output Of Phase Discrimination*

Compared with the results in some published literature, as is shown in table 1, this design method has certain advantages in terms of the power consumption and relative dithering under the condition that the the process and the power supply voltage are close, though, the specific application and design index are different[6].

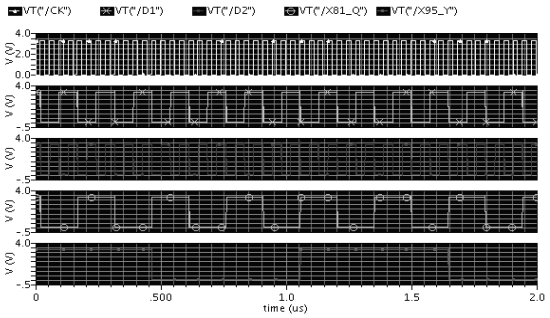

Figure 11 *The Simulation Output Of Frequency Divider*

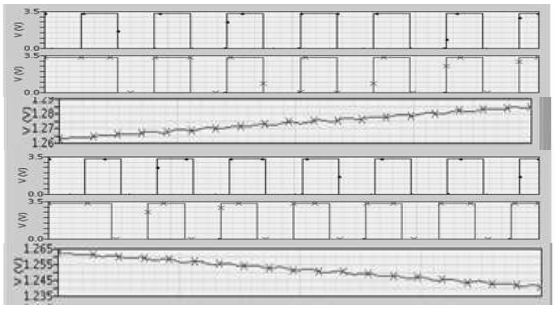

Figure 12 *The Simulation Output Of Charge Pump*

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Table 1 *Performance Comparison Between Different Design Methods*

Different design methods	size/ μm	power voltage/V	tuning-range of the oscillator/ M	Peak of Cycle jitter/ps	ΔT:T /%
literature[6]	0.18	1.8	116~1095	57	1.5
literature[7]	0.25	2.5	0.5~1000	290.9	1.8
literature[8]	0.35	3.3	1~1900	55	4
literature[9]	0.35	1.8	103~1030	110	>1.8
literature[10]	0.25	1.8	0.1~480	150	7
This paper	0.35	3.3	105~335	330	0.9

5. CONCLUSION

This paper puts forward the clock structure of the video decoder, and focuses on the design of charge pump phase-locked loop on this basis. Finally, the 27 MHz clock signal needed in video decoder is acquired. By improving the phase and frequency detector, charge pump circuit, and oscillator circuit design based on the traditional charge pump, a clock signal that in line with VSYNC is produced. Thus the clock signal used in the video decoder chips can have a more stable performance. By adopting the 0.35μ2P4M 3.3V standard CMOS technology created by SMIC company, and the simulink software in Matlab, the system level simulation is done, and the Spectre software in Candence is used for the circuit level simulation. Tests results show that the effective tracking range of PLL is 5 MHz ~ 7.5 MHz, the locking output is 6.75 MHz during which the clock jitter is less than 500 ps, the output waveform's duty circle is 50.1408%, which meets the design requirements.

REFERENCES:

[1] Karl Renner,Peter Chang.Color Phase-locked Loop for Video Decoder. United States Patent:6330034.DEC.11,2001

[2] US patent:clock generation for digital video signal processing apparatus,Patent number:6034735

[3] US patent:Horizontal Phase-locked Loop for Video Decoder, Patent no:6317161 B1

[4] PLarsson,CSvensson.Skew safety and logic flexibility in a true single Phase Clocked system.In Proc.IEEE Int.Symp.Circuits Syst,1995(2):941-944

[5] Xiao Jian, Li Dongcang, Sun Shuo, Zhang Fujia. On the charge pump PLL design base on the HDMI video signal receiving. Journal of Xi'an Oil University (Natural Science Edition) 2007 (22] 6:97-100

[6] Wei Jianjun, Li Chunchang, Kang Jichang. On the offset adaptive charge pump PLL. Journal of Sichuan University (Engineering Science Edition) 2010, 42 (2) : 188-190

[7] Jung Wooyoung, Choi Hyoungchul, Jeong Chanigwon. A 1.2 mW 0.02mm2 2GHz Current-controlled PLL based on a self-biased voltage-to-current converter[C].2007 IEEE International Solid-state Circuits Conference:310-312.

[8] Yan Jiefeng. Adaptive bandwidth PLL with compact current mode filter[C]. 2006 IEEE ISCAS. Greece,2006:3442-3445.

[9] Chen O. A power efficient wide-range phase-locked loop[J]. IEEE Journal of Solid-state Circuits,2002,37(1): 51-62.

[10] Qian Zhehong. Design of clock generator based on charge pump PLL for USB2. 0[D] Shanghai: Fudan University,2005.