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A PROPOSED UNDER-VOLTAGE LOCKOUT OF COMPENSATED TEMPERATURE COEFFICIENT THRESHOLD VOLTAGE WITHOUT COMPARATOR

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ABSTRACT

A proposed under-voltage lockout of compensated temperature coefficient threshold voltage without comparator is presented in this paper. The circuit achieves stability of threshold voltage without utilizing extra band gap reference voltage source and voltage comparator. In the temperature range of from -40℃ to +125℃, variation of only 30mV of the threshold voltage occurs. The under-voltage lockout circuit is designed and simulated with standard CMOS process with featured size of 0.6 μ m.

Keywords: *Under-voltage Lockout, Temperature Compensation, Band gap Reference*

1. INTRODUCTION

With the increasing popular demand of portable electronic devices powered by battery, many circuits such as LED driver, audio power amplifier and digital signal processing unit and so on are sensitive to fluctuations in supply voltage. Therefore, the steady power supply is particularly important than ever before. More particularly, when the supply voltage drops below a minimum specified operating voltage it will be destructive. Some circuits in the system may either be damaged or may exhibit unpredictable operation. The unpredictable operation may be especially critical in circuits that include processing engines such as microprocessors, microcontrollers, and digital signal processors, for examples. As a result, a need for power monitoring has become prevalent. The under voltage lockout (UVLO) circuit provides important detection of under voltage conditions in the power supply thus preventing malfunctions. UVLO circuits are commonly employed to monitor a power supply and to provide a signal representing the quality of the power supply. Initial application of power to an integrated circuit therefore begins with the UVLO circuit generating an output signal that initially indicates that the power supply is insufficient, such that power is prevented from being supplied to the remainder of the integrated circuit. In this way, the anomalous behavior and current consumption of connected circuits caused by low-voltage condition is prevented [1] [2] [3].

Typical UVLO circuits rely on comparison of the power supply voltage to a threshold voltage to determine whether the signal is of sufficient magnitude or not. Consequently, the UVLO circuit must be capable of generating a threshold voltage that is supply, temperature, and process independent and that can be used as a reference value to which the supply voltage is compared. In particular, band-gap reference voltage generator is often constructed to supply the stable and temperature independent voltage reference as the threshold voltage [4] [5].

In this work, a proposed under-voltage lockout of compensated temperature coefficient threshold voltage is presented. Without the comparator and band gap voltage reference, the complexity and power of circuit decrease dramatically. This paper consists of five sections. After the introduction of the background and necessity of UVLO, we advance the basic principles and characteristics of

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UVLO by reviewing the traditional structures in section 2. Then, the concept and realization for the proposed UVLO circuit are discussed in section 3. The simulation and discussion are presented in Section 4. Finally, Section 5 gives the conclusion for the whole work.

2. TRADITIONAL UVLO STRUCTURES

The UVLO is not a new device, and various embodiments are disclosed. In the applications of high voltage, the zener diode shown in Figure 1 is used as the reference voltage to monitor the power supply. However, for the voltage through a zener diode is more or less 6-7V, this kind of implementation is only suitable for applications of high power and high voltage systems [3]. With the development trend of lower voltage operation for the lower power consumption, this structure is not as popular as it before. Furthermore, the zener diode is not compatible with the modern standard CMOS process and increases the cost of realization. Therefore the method is not attractive for monolithic implementations.

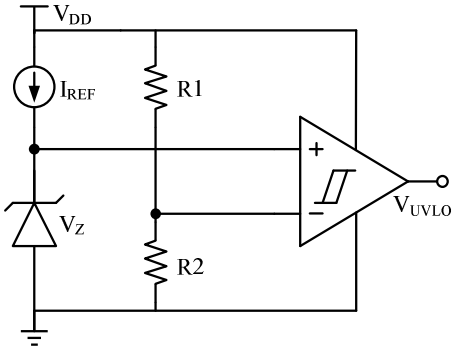

Figure 1 UVLO topology with zener diode [3]

P. Hong etc. designed a traditional UVLO circuit with comparator and reference voltage generator. The circuit is relatively complex and consumes relatively high power. Moreover, the threshold voltage is sensitive to temperature [4].

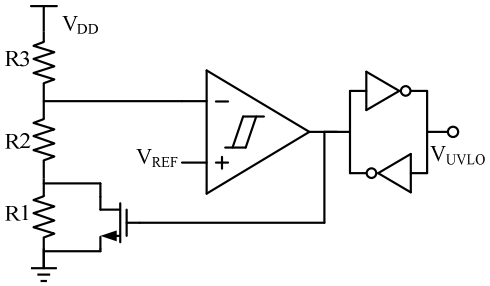

Figure 2 UVLO circuit in [4]

In [5], a UVLO cell for monitoring the battery voltage and change its modes of operation accordingly is fabricated with standard CMOS process. The circuit takes the advantages of low cost and low power consumption. However, the threshold voltage depends on the temperature heavily for the nature of the CMOS devices. Zhao Fanglan presented an UVLO circuit with zero temperature coefficient threshold based on the band gap invented by Brokaw, and the schematic diagram is illustrated in Figure 3. The hysteresis characteristic is realized by adjusting sampling resistor string ratio [6].

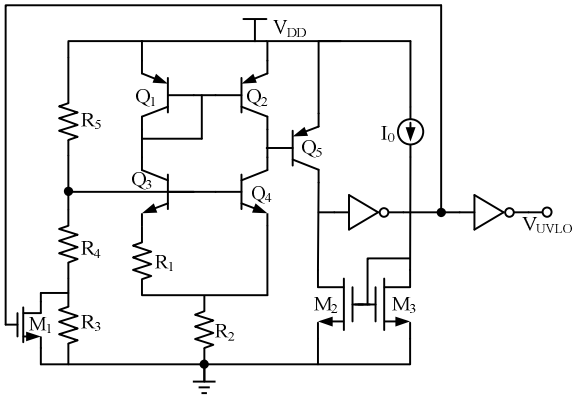

Figure 3 UVLO circuit in [6]

Another UVLO with temperature insensitivity threshold voltage is proposed in the literature [7]. The band gap reference voltage generator and comparator are compounded to form the circuit. Under the normal condition, the comparator acts as an operational amplifier to equalize the voltages. When the power supply decreases, the comparator can be used to realize under-voltage lockout protection.

3. TRADITIONAL UVLO STRUCTURES

In the design presented in this paper, the diode-connected NPN transistor Q_1 and resistor R_1 are used to detect the power supply voltage. M_1-M_2 and M_3-M_4 are current mirrors whose values determine the V_{UVLO}. The size ratio of Q_1, Q_2 and Q_3 are 1, 1 and 8, respectively.

The V_{UVLO} is determined by the drain current difference of M_4 and M_6. That's to say, the current difference between Q_2 and Q_3 determines the output voltage level. The reference current relative to power supply voltage can be derived like Eq. (1).

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$$I_0 = \frac{V_{DD} - V_{BE1}}{R_1} \quad (1)$$

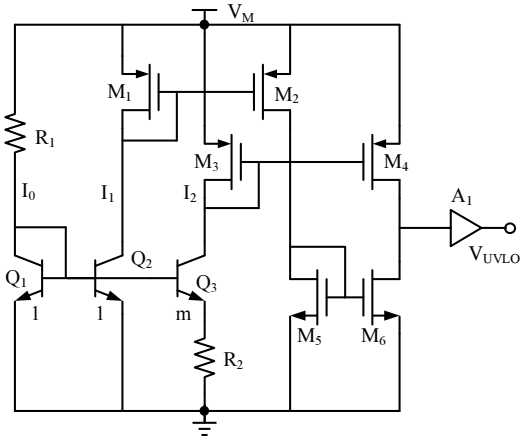

Figure 4 UVLO circuit presented in this work

The current mirror Q_1-Q_2 makes the current through Q_2 is the same as Eq. (1). The current through Q_3 can be achieved based on the band gap reference voltage generator as Eq. (2).

$$I_2 = \frac{V_{BE1} - V_{BE3}}{R_2} = \frac{V_T}{R_2} \ln \frac{I_{C1}A_3}{I_{C3}A_1} = \frac{V_T}{R_2} \ln 8 \quad (2)$$

As the power supply voltage is very low, the whole circuit turns off. When the power supply increases further, Q_1 will conduct the current leading to Q_2 turns on, but Q_3 keeps off state just for the R_2. Under the condition like this, M_4 turns off, and M_6 can conduct a little current, so the V_{UVLO} will be low. Assuming the ratios of all the current mirrors are the same, the output signal will be as follows.

When $I_0=I_1>I_2$, i.e. $I_{D6}>I_{D4}$, and M_6 will be pushed into linear operation region. As a result, the output will be low level.

When $I_0=I_2$, the threshold voltage is achieved with Eq. (1) and Eq. (2).

$$V_{DD,TH} = \frac{R_1}{R_2} V_T \ln 8 + V_{BE} \quad (3)$$

The $V_{DD,TH}$ is the threshold of power supply voltage, and the temperature characteristic of that can be calculated as,

$$\frac{\partial V_{DD,TH}}{\partial T} = \frac{R_1}{R_2} \ln 8 \frac{\partial V_T}{\partial T} + \frac{\partial V_{BE}}{\partial T} \quad (4)$$

As we know, the temperature coefficient of V_T is almost 0.085mV/℃, and that of V_{BE} is about -2mV/℃. The ratio between R_1 and R_2 will balance the temperature coefficient to be close to zero. Although there are some 2nd-order nonlinearities affecting the compensation result, the performance is good enough for almost all the applications. Once V_{DD} increases over the threshold, the output signal will change.

4. SIMULATION RESULTS AND DISCUSSION

The circuit is designed with standard 0.6μm CMOS process and simulated with the Specter tool. With the increase of monitored voltage, the output will turn around over the threshold. The curves in Figure5 and Figure 6 illustrate the threshold voltage vs. power supply and threshold voltage vs. temperature, respectively. The threshold voltage of the design is about 3.7V, and the variation of only 30mV is achieved in the temperature range of from -40℃ to +125℃. The temperature compensation is realized according to the curves in Figure 6.

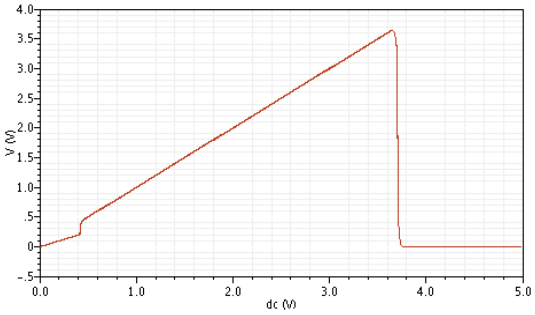

Figure5 Threshold voltage vs. power supply

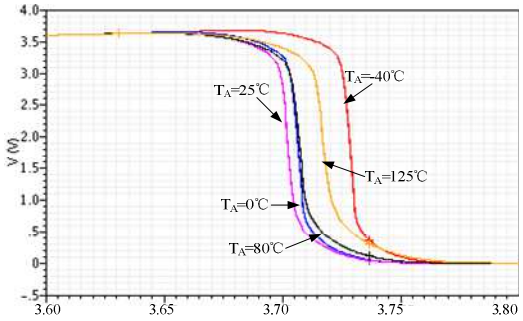

Figure 6 Threshold voltage vs temperature

5. SUMMARY

This paper presents a proposed under-voltage lockout of compensated temperature coefficient threshold voltage without comparator. The UVLO

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circuit is designed and simulated with standard 0.6μm CMOS process. The circuit achieves stability of threshold voltage without utilizing extra bandgap reference voltage source and comparator. The simulation results show that the variation of only 30mV of the threshold voltage occurs in the temperature range of from -40℃ to +125 ℃, and the temperature compensation is achieved.

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