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CHARACTERIZATION OF TUNNEL FET FOR ULTRA LOW POWER ANALOG APPLICATIONS

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ABSTRACT

In modern portable devices, the supply voltage is decreased to reduce the power dissipation. However as the supply voltage is scaled down below 0.4V, the normal MOSFET devices cannot be used due to lower $I_{ON/}$ I_{OFF} ratio which will reduce the static power dissipation. Hence for low power applications, Tunnel FET is used as alternatives due to their higher sub threshold swing, extremely low off state current (I_{OFF}) and excellent sub threshold characteristics. Hence Tunnel FET transistor has attracted a lot of attention for analog and RF applications. In Tunnel FET, the dynamic power dissipation will be decreased since the operating voltage is very low (0.4).

The power consumption becomes a major bottleneck for further scaling. The continued reduction of MOSFET size is leading to increased leakage current due to short channel effects. A promising alternative for MOSFET which does not suffer from these limitations is Tunneling FET.

In this work, characterizing the various parameters of Tunnel FET such as on current, off current, Transconductance generation factor for ultra low power analog applications.

Keywords: *MOSFET (Metal Oxide Semiconductor Field Effect Transistor), Tunnel FET.*

1. INTRODUCTION

Since the invention of the first electronic calculation machines, miniaturization has been a constant challenge to increase the speed and to improve the package density by the microelectronics industry. A far increasing number of new functions to the basic computing systems such as fast data computing, telecommunication, and several kinds of actuations which are collectively fabricated called integrated circuit or the "chip". The electronic device with increasing speed has a tremendous success, the Micro and Nano electronics by continuously introducing innovations in the fabrication process. The linear scaling in the CMOS technology in the deep sub micrometer regime gives rise to the short channel effects (SCEs). The analog performance parameters are greatly affected by the SCEs.

The **ITRS & TCAD** technology is used for device design. **ITRS(**International Technology Roadmap for Semiconductor). The aim of the Roadmap is to identify key, requirements and critical challenges to sustaining the conventional scaling of CMOS technology (i.e., according to Moore's Law). Technology Computer Aided Design (TCAD) can be a powerful tool for reducing the design costs, improving the device design productivity and obtaining the better device and the technology designs. Instead of going through an expensive and time-consuming fabrication process, the computer simulations can be used to predict the electrical characteristics of a device design quickly and cheaply.

2. SENTAURUS DEVICE:

It is used to simulate the electrical characteristics of the device like terminal currents, voltages, and charges are computed based on a set of physical device equations that describes the carrier distribution and the conduction mechanisms.

2.1. Sentaurus process:

Sentaurus Process is a complete and highly flexible, multidimensional, process modeling environment. The main file types used in sentaurus process are:

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1. Sentaurus Process command file (* .cmd)
2. Log file (* .log)
3. Structure file (has no extension)
4. TDR boundary file (*_bnd.tdr)

3. SENTAURUS STRUCTURE EDITOR:

Sentaurus Structure Editor is a structure editor for 2D and 3D device structures. Input and output files of Sentaurus Structure Editor are:

1. Scheme script file (.scm)
2. ACIS SAT file (.sat)
3. DF-ISE doping and refinement file (.cmd)
4. DF-ISE boundary file (.bnd)

Finally, Tecplot SV is used to visualize the output from the simulation in 2D and 3D, and Inspect is used to plot the electrical characteristics, as well as, analyzing the simulation results by a powerful GUI-driven technique.

4. JUSTIFICATION OF WORK:

In CMOS digital applications, the transistor efficiency is mainly determined by the on-current (I_{on}) and the off-current (I_{off}) requirements of the device. By scaling the technologies into sub 100 nm regimes, the drain induced barrier lowering (DIBL), the channel length modulation (CLM), the charge sharing, the gate tunneling and the band-to-band tunneling cause I_{off} to increase drastically, while I_{on} is not increasing significantly due to the reduced carrier mobility, and the source/drain parasitic. Hence, maximizing the I_{on}/I_{off} is the primary objective for the device design in logic circuits. On the other hand, the above 2D effects also degrade the transistor saturation current (I_{DSAT}), the transconductance (g_m), the transconductance generation factor (g_m/I_D), and the output resistance (R_o), which seriously limit the analog circuit performance in the scaled technologies.

This advanced performance of MOSFETs is attractive for the High Frequency (HF) circuit design in view of a system-on-a-chip realization, where the digital, the mixed-signal base band, and the RF transceiver blocks would be integrated on a single chip. Thus the performance of the scaled MOS devices in case of analog and RF applications. In a particular technology, the analog/RF circuit performance is affected by many other performance tradeoffs such as the signal to noise ratio (SNR), the signal gain-bandwidths, the power dissipation, the speed with each parameter in turn related to other. The analog/RF circuit quite complex when compared to its logic counterpart due to conflicting device performance requirements for the analog and digital circuits.

Hence, any suggested device design approach which reduces the leakage power dissipation with the decrease in the value of supply voltage (VDD), must be thoroughly evaluated for its ultra low power analog performance requirements to meet the performance of modern device circuits, which is the primary look out in this work.

5. SCOPE OF THE WORK:

This work has been analyzed thoroughly about the subthreshold analog performances of advanced Tunnel FET devices with 30nm gate length. Integrated Systems Engineering (ISE) - Technology Computer-Aided Design (TCAD) has been used for the realization and the analysis of all the devices used in this study. All the device parameters are set as per ITRS road map for the 100nm gate length.

In the case of the graded channel Tunnel FETs, the optimization of N channel and P channel TFETs with doping concentration is also shown. In the case of the DG TFET with the metal gate technology, the optimization of the length of the metals gates is illustrated with the detailed simulation results. Analog parameters like the transconductance (g_m), the transconductance generation factor (g_m/I_D), the early voltage (V_A), the output resistance and the intrinsic gain of all the devices have been investigated and compared with that of the conventional DG MOSFETs.

6. EXPERIMENTAL ANALYSIS:

This work focuses on the performance analysis of double gate TFETs implemented to study the ultra low power analog performance parameters in the 100nm gate length regime. Different forms of the tunnel FET are SOI TUNNEL FET, GREEN FET, IMOS. These three type is p-i-n diode structure. The tunneling effect is not so efficient. So as to overcome the limitations of the above devices used, we go for the structure of Double Gate Tunnel FET.

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6.1 Double gate tunnel FET:

The double gate tunneling field-effect transistor (DG TFET) is explored through two dimensional device simulation. The new tunnel FET designs is required, so that, the ION will attain without sacrificing IOFF. The device have the dimensions of gate thickness (3nm), channel length (50nm) and body thickness (10nm).

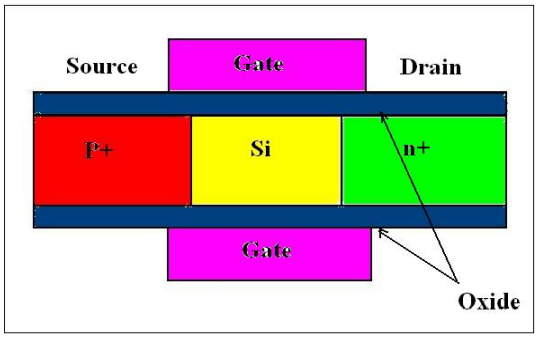

Fig:1 Device structure of DG Tunnel FET

The device structure is investigated, a lateral N type tunnel FET in a thin silicon layer, isolated from the substrate by a gate layer. The basic design is a gated p-i-n diode. The tunneling takes place in this device between the intrinsic and p+ regions. N channel DG TFET, the source and the drain are asymmetrically doped with the source being p-type doped and the drain n-type doped and it could be fabricated and employing a substrate doping concentration of 5e16 cm-3, a gate layer with an equivalent oxide thickness of 1.0nm and the gate work function of 4.05 eV. Doping has been optimized in order to create the maximum ON current, while keeping OFF current low. For these simulations, the doping levels where 1e20, 1e17 and 1e19 atoms/cm3 for the source, intrinsic and drain regions respectively. In our simulations, the source is grounded and the positive voltage is applied to the drain and the voltage is applied to the gate.

As the positive gate voltage increases, the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow. In the OFF state, the gate bias Vgs is zero and there is insufficient band bending tunneling to occur. As such, the leakage current of the device is extremely low and is due to the drift of minority carriers, similar to that of a reverse biased p-i-n diode. In the ON state, the gate induces sufficient band bending such that the tunneling barrier width ωT narrows to below 5nm, leading to significant band to band tunneling of electrons from the valence band of the p+ source to the conduction band of the n+ drain.

Thus, the sub threshold swing of the TFET beats the theoretical limit of 60mV/decade for a conventional metal-oxide-semiconductor FET at room temperature. In order to meet the requirement of the (ITRS) for low standby power technology and for better scalability, the DG TFET is simulated

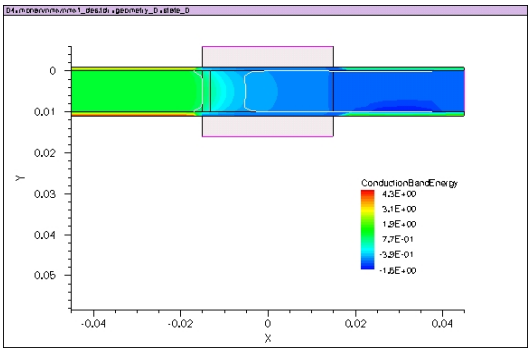

Fig:2 Conduction band Energy of a Simulated DG Tunnel FET

The band to band tunneling in a simulated device is illustrated in figure 2 and 3 where it is evident that as the gate voltage increases the band gap decreases which results in tunneling of electrons from the source to drain side.

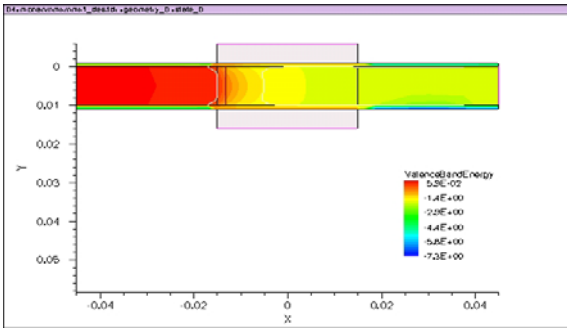

Fig:3 Valence band energy of a simulated DG Tunnel FET

From the following, we determine the electron density by varying the position along the channel length along the oxide layer and the resulting electron density is determined. The optimized DG TFET uses a gate oxide with a dielectric constant of 21. Since the threshold voltage of a Tunnel FET cannot be extracted using certain standard MOSFET techniques. But in double gate TFET we are using constant-current method, with a threshold current of 10-7 A/um.

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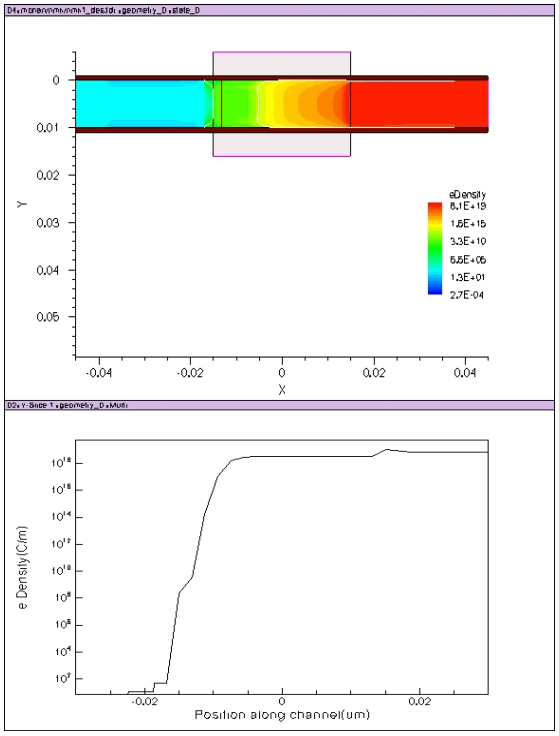

Fig:4 Electron Density of a simulated DG Tunnel FET

7. CHARACTERIZATION OF DGTFET FOR ANALOG APPLICATIONS:

The device structure of Double Gate Tunnel FET with Si as the source material is generated using Sentaurus Device tool in TCAD. In this generated device, we are characterizing the following parameters for analog applications.

The increase in gate voltage will gradually increase the Ioff value and the graph will be obtained as shown below. As the gate voltage increases from 0.3 to 1.1 V, the Ioff will gradually increase from 1.20E-012 to 3.00E-012 A and reaches the maximum value at 3.00E-012A.

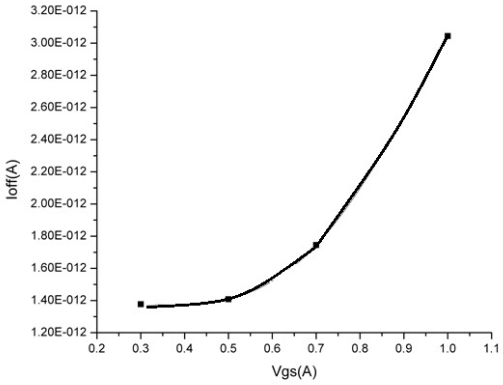

Fig:5 Simulated OFF Current as a function of Gate Voltage**.**

With the increase in the gate voltage, the ON current gets varied respectively. As the gate voltage is increased from 0.3 to 1.1V, the ION value gets decreased from the maximum to the minimum value (i.e) 5.00E-012 to 4.20E-012 as shown in figure 6.

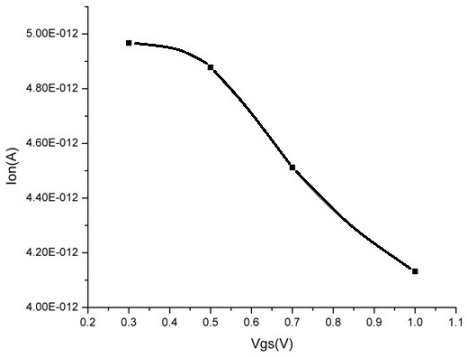

Fig:6 Simulated ON Current as a function of Gate Voltage.

The variation in the current ratio (ION/IOFF) is determined with the variation in the gate voltage (Vgs). As the gate voltage increases, the current ratio will be decreases from maximum value and reaches the lower value as shown in the figure 7.

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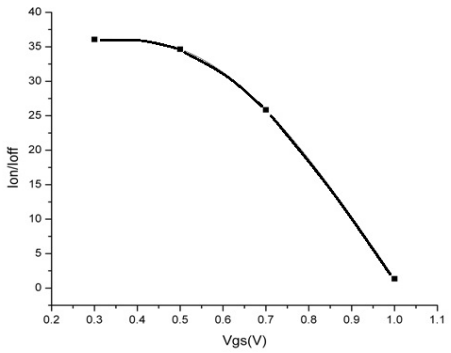

Fig:7 Simulated Ion/Ioff as a function of Gate Voltage.

The gate to source voltage is varied to obtain the variation in the transconductance, gm of the generated device as shown in Figure 8 for different drain voltages. The transconductance, gm is high for Vd=0.7V.

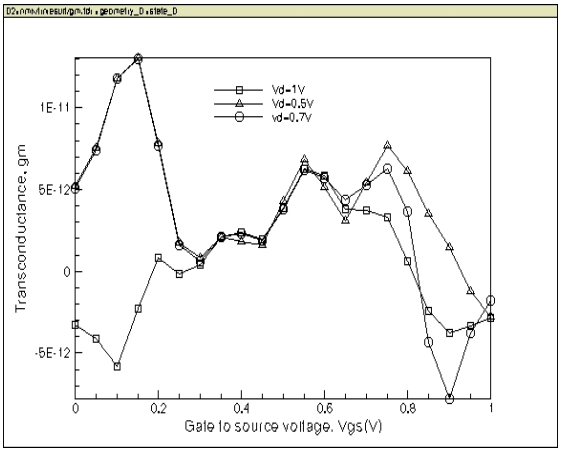

Fig:8 Simulated Transconductance as a function of Gate Voltage

The variation in the transconductance generation factor (g_m/Id) is observed with the increase in the gate to source voltage, Vgs(V) keeping the drain voltage constant with different values which shows that the gm/id is very low for higher drain voltages as shown in the following figure

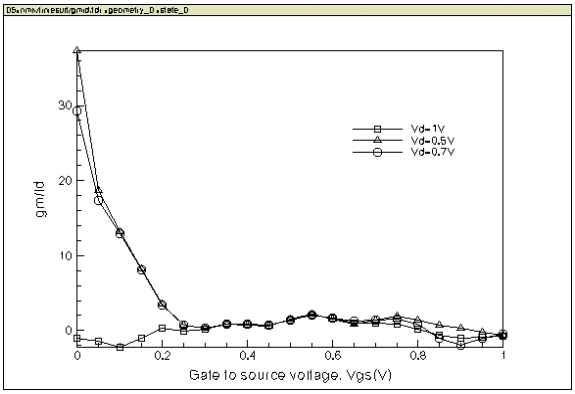

Fig:9 Simulated Transconductance Generation factor as a function of Gate Voltage

The drain current variation for various drain voltages as a function of Gate voltage is shown in figure 10 where it depicts that the drain current is improved if the drain voltage is increased.

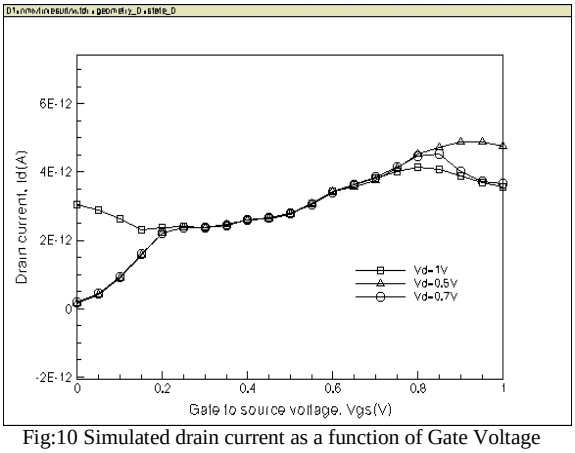

Fig:10 Simulated drain current as a function of Gate Voltage

8. SiGe TUNNEL FET:

In this work aim's to increase the ON state current (ION) with a SiGe source in order to improve the ION compared to conventional structure. IMOS failed to meet the ITRS requirement due the problems, like threshold voltage caused due to hot carrier injection. Inspite of excellent sub threshold swing (~30mv/decade) and high ION/IOFF ratio, the very low ION is the main issue with this device. To overcome this limitation, the high k-material is used as gate dielectric, which results in very high field and break down of the dielectric because the high k-material is lower than SiO2. For simulation of the device, a fixed oxide thickness of 2nm and channel length of 100nm is taken. The n- drain is doped 2×10^19 cm-3, p+ source is doped 1×10^20 cm-3 and the

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substrate is doped 1×10^16 cm-3.By using SiGe, instead of Si in tunneling region, a reduction in the band gap and thus an improvement in the drain can be achieved. Due to reversed biased p-i-n structure, the output impendence of the device is very high. Thus the leakage power dissipation ant to improve the ON current, SiGe source is used in the double gate TFET and which is characterized for ultra low power analog application

9. CONCLUSION AND FUTURE SCOPE:

In this work, the physics of optimizing DG TFET performance is discussed. Strong gate coupling at the center of the silicon film at the source is important for modulating the band-to-band tunneling. Increasing the silicon film thickness to a certain limit would increase the volume of thickness to certain limit would increase the volume of silicon for band-to-band tunneling and enhance the drive current. Above this limit, the on-state current decreases due to reduced gate-to-state current decreases due to reduced gate-to-channel coupling. For further improvement of ON current in this device, SiGe is used as source material in this double gate Tunnel FET.

Thus, an alternative TFET architecture is proposed to improve its performance (i.e) SiGe Tunnel FETs. The proposed device shows considerable improvement in the device characteristics compared to the conventional structure. An order of increase in the ON current of the devices is observed while maintaining the ION/IOFF ratio and the sub-threshold swing of the device. It will be shown that the incorporation of SiGe in Tunnel FETs leads to a significant improvement of the device characteristics that underlines its applicability in current CMOS technology. An additional improvement can be achieved by incorporating of high-k gate dielectrics, which lead to the occurrence of fringing fields. As a result these devices will be a vital candidate for ultra low power devices in which power dissipation is the most minimum.

ACKNOWLEDGMENT:

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