REVIEW ARTICLE: EFFICIENT MULTIPLIER ARCHITECTURE IN VLSI DESIGN

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ABSTRACT

Designing high-speed multipliers with low power and regular in layout have substantial research interest. The analysis is done on the basis of certain performance parameters i.e. Area, Speed and Power consumption and dissipation. Multipliers are considered to be an important component in DSP applications like filters. Therefore, the low power multiplier is a necessity for the design and implementation of efficient power-aware devices. In this paper we have analyzed and reviewed a few multiplier architectures based on their working principle, speed and power efficiency.

Keywords: *Multiplier, Modified Booth-Encoding, Carry Save Array Multiplier, Partial Products, Wallace Tree Multiplier.*

1. INTRODUCTION

Multiplication is a basic arithmetic operation which is present in many part of the digital computer especially in signal processing systems such as graphics and computation system. It requires more hardware resources and processing time than addition and subtraction requires. There is a continuous development in VLSI technologies and, the needs to develop process independent chip design tools are growing [1], [2], [3]. The use of hardware description language (HDL) for integrated circuit designing is good for the process design rules at the early stages of design [4]. Multipliers are the basic component in single chip digital information processors [5], [6]. With advances in technology, many scientist have tried and trying to design multipliers which offer high speed, low power consumption, layout regularity and hence less area or even combination of them in multiplier. The multiplier compiler design defined in [7] and [8] generate parameterizable layout for MOS technology, thus making them suitable for various high speed, low power, and compact VLSI implementations. However area and speed are two important conflicting constraints. So improving speed results always in larger areas. The number of gates per chip area keeps on increasing, while the gate switching energy does not decrease at the same

rate. So the power dissipation rises and removal of heat becomes difficult and expensive. The dynamic power of CMOS circuits is becoming a major concern in the design of devices. There are different multiplier structures which can be classified as Serial Multipliers, Parallel multipliers, Array multipliers, Tree multipliers and so on. Multipliers are categorized in relative to their architecture, applications, and the way of producing partial products and summing up of partial products to produce the final result.

2. WALLACE TREE MULTIPLIER

For real-time signal processing, a high speed and throughput Multipliers-Accumulator (MAC) is always a key to achieve high performance in the digital signal processing system. The main consideration of MAC design is to enhance its speeds. That high speed is achieved through this well-known Wallace tree multiplier. Wallace introduced parallel multiplier architecture [9], [10] to achieve high speed. Wallace Tree algorithm can be used to reduce the number of sequential adding stages. The advantage of high speed becomes an enhanced feature for multipliers having operand of greater than 16 bits. The Wallace tree was being constructed using carry save adder to reduce an N-row bit product matrix to an equivalent two row

matrix that is then fed into carry propagating adder to sum up those rows of bits and to produce the product. The carry save adders are those conventional full adders [11] in which carries are not connected and three bits of inputs are taken in and two bits are given as output. Instead of using carry save adders in this multiplier, full adders and half adders of 4:2 compressors and 3:2 compressors can be used in their reduction phase.

Generally the Wallace tree construction has many ways to implement. One way among them is considering all bits in a column and producing two bits as output for that column. Another way is to consider first four bits of a column and producing two bits which uses 4:2 compressors. And the other is considering first three bits in a column which uses 3:2 compressors. The Wallace Tree multiplier has an irregular structure [12]. Many different adder tree structures have been used to reduce the computation time of the multipliers. The computation time of the Wallace tree has achieved the lower bound of *O (log3/2 N)*. For n-bit Wallace tree multiplier, the number of steps needed is (log3/2(n/2) + 1). Wallace tree multipliers have significant complexity and timing advantages over traditional matrix multipliers.

The main disadvantage of Wallace tree multipliers is its irregular structure, making layout difficult and all adder blocks are active regardless of multiplicand size.

more area on the wafer [13], [14], [15] and needs greater cell interconnection wiring. Since an interconnection plays an important role in IC technologies this factor makes Wallace tree inappropriate for certain circuits [16], [17]. The main advantage of this multiplier is its Logarithmic circuit delay. In many FPGAs, Wallace trees do not provide any advantage over ripple adder trees. Due to irregular routing, they may actually be slower and may certainly more difficult to route. Adder structure used in this will increases for increased bit multiplication.

3. MODIFIED BOOTH MULTIPLIER

Booth encoding is a method of reducing the number of partial products required to produce the multiplication result. To achieve high-speed multiplication, algorithms using parallel counters like modified Booth algorithm has been proposed and used. This type of fast multiplier operates much faster than an array multiplier for longer operands because it's time to compute is proportional to the logarithm of the word length of operands. By recoding the numbers that are to be multiplied, Modified Booth multiplier allows for smaller, faster multiplication circuits. The number of partial products is reduced to half, by using the technique of Booth recoding [18]. Reduction in the number of partial products depends upon how many bits are recoded and on the grouping of bits.

Fig.1 Wallace tree multiplier

Delay is log (n). The Wallace tree multiplier has irregular interconnection which in turn occupies
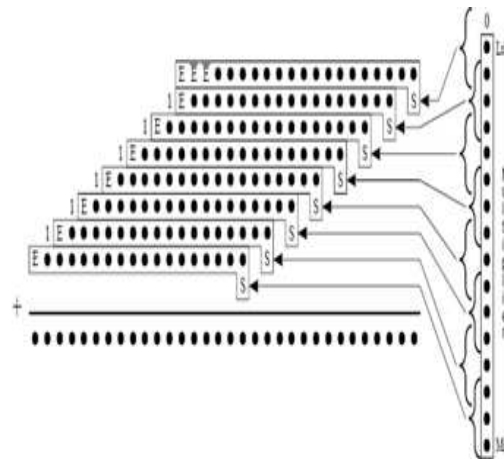

Fig.2 Modified Booth Encoder

The grouping considers each three bits of the multiplier bits starts from the LSB bit and the first considers only two bits. From the next it considers three bits in which one bit will be overlapped on the previous group.
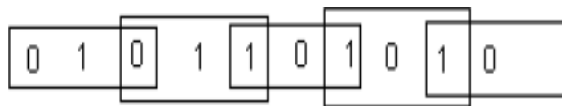
Fig.3 Grouping of bits from the multiplier term

Thus grouped multiplier will result in the production of bits between these five bits as follows as -2,-1, 0, +1, and +2.

Block	Re - coded digit	Operation
000	0	0
001	+1	+1
010	+1	+1
011	+2	+2
100	-2	-2
101	-1	-1
110	-1	-1
111	0	0

Table1. Recoding Table

The advantage of this method is making the number of partial products into half of the multiplier term size by grouping. The main disadvantage of the modified booth multiplier is its complexity of the circuit to produce partial product.
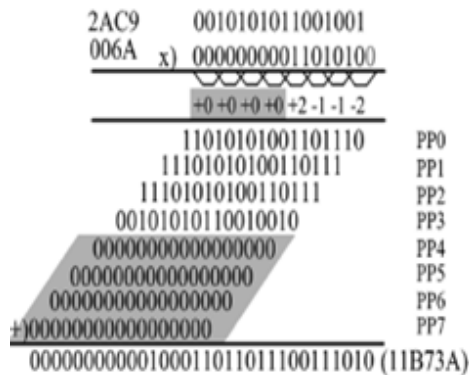

Fig.4 Example of Modified Booth Multiplier

4. MIXED STYLE MULTIPLIER

Low power VLSI Design is necessary to satisfy Moore's law and to produce consumer electronic goods with low power consumption and with high battery backup. Saving power is necessary in this modern world. Dynamic Power is the dominant property in the technology above 0.1m, while in smaller technologies Leakage Power is more important. Dynamic power dissipation is occurred as a result of charging the Load capacitances in a circuit. This dynamic power consumption of CMOS IC is calculated by adding the transient power consumption (PT), and capacitive-load power consumption (PL). For the past few years, different optimizations have been applied in the architecture in order to minimize the dynamic power dissipation in arithmetic circuits, and especially in digital multipliers [19], [20].
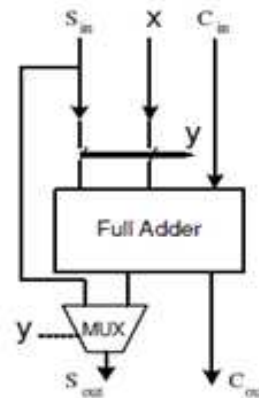

Fig.5 The FAB Cell

In this Mixed Style Multiplier, there are two parts of multipliers. One is array part and the other one is a tree part multiplier. The array part is chosen as Carry Save array multiplier which considered giving good result when combined with the bypassing technique. The design of low power combinational circuits is introduced using a technique of bypassing logic blocks when their function is not required. This bypassing is carried out using low delay and area overhead component like transmission gates. This technique offers great power savings by avoiding switching activity in the circuit which in turn produces dynamic power savings. This bypassing technique is done in the array part of the multiplier. The array multipliers are chosen for this bypassing technique since it has a regular interconnection which helps to skip unwanted blocks. The array multipliers have linear delay circuit [21].
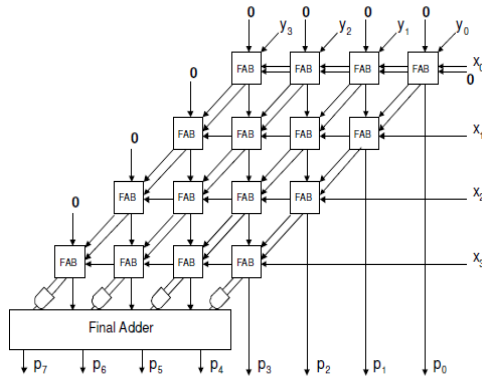
Fig.6 The 4x4 Carry-Save Array multiplier with bypass

The functionality of the of the Carry save array multiplier is $X=(xn-1,.....,x1,x0)$ and $Y=(ym-1,.....,y1,y0)$ are fed into FAB cell. The transmission gates in FAB cell lock the inputs of the full adder to prevent any operations when $y=0$ and the multiplexer propagates the sin to the sout. When $y=1$, the full adder works and produces sout. The second part is a tree part multiplier which has the advantage of logarithmic circuit delay and considered to produce results in faster way [21].
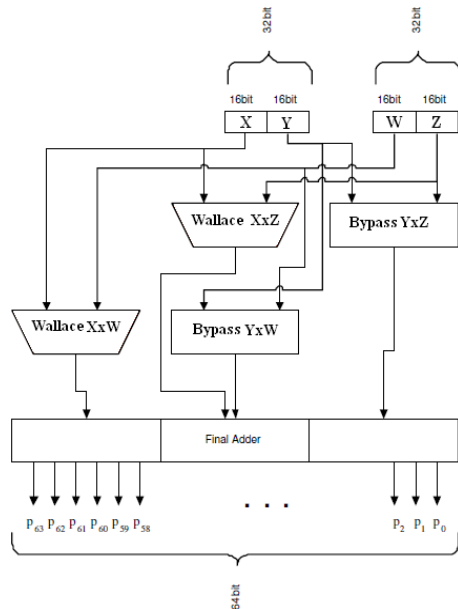

Fig.7 A 32 bit multiplication split in parts

The great timing advantage of the Wallace tree multiplier along with the great power advantage of the bypass scheme in the carry save array multiplier can be combined in mixed multiplier architecture. The 32 bit values can be multiplied by splitting them in two 16 bit. If the first 32bit value is (X, Y) and the second is (W, Z) four 32 bit partial products are generated. A = X x Z, B = Y x Z, C = X x W and D = Y x W. These four partial products are shifted and added together to produce the final 64 bit multiplication result [22]. The main operation behind these operand splitting is to use different multiplier architectures for each different partial multiplication. So, from A = X x Z and C = X x W performance is gained while from B = Y x Z, and D = Y x W power is gained, if half of one or both operands usually contains more no of 0s than 1s, this specific half should be passed through the bypass array multiplier for greater power advantages

This multiplier can give good results of power consumption and dynamic power savings but it is not sure give good results in the other parameters such as time and area. Therefore it's hard to implement Wallace tree in FPGA for its irregular and complex interconnection. By using a faster and efficient multiplier which possesses familiar interconnection model than Wallace tree multiplier can give better results than this architecture.

5. PROPOSED ARCHITECTURE

The Carry save array multiplier is considered to have good dynamic power savings by using the bypassing technique across full adders. It uses low power consumption components like transmission gate, multiplexer in the place of full adder therefore it reduces power consumption and it avoids the unwanted switching activity which in turn reduces the dynamic power dissipation. We can expect large amount power savings in carry save array multiplier. On the other hand, in all cases the proposed bypass architecture offers power savings ranging from 20% up to almost 60%.

A new architecture can be proposed by combining bypass carry save array multiplier with Modified Booth-Wallace tree multiplier it may produce results in a much faster way. Since Modified booth Wallace is considered to have best result in Area-Delay2 product (AD2) and Delay Product (DP) among some of the multipliers. Considering Modified Booth-Wallace tree multiplier in the place of Wallace tree multiplier may give good and fast results and will reduce power dissipation.
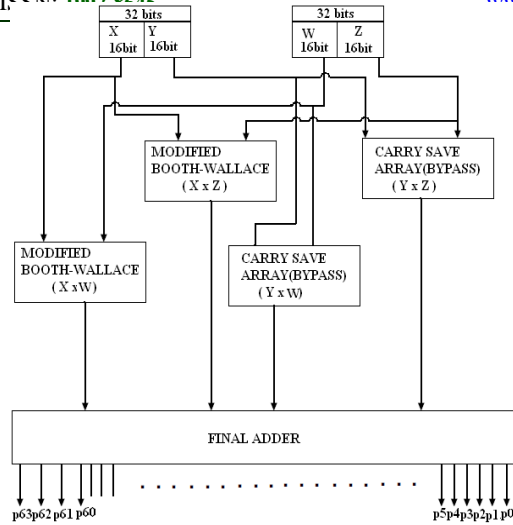
Fig.8 Proposed Architecture

6. RECOMMENDATION & LIMITATIONS

The multiplier which concentrates on all the parameters, time and area with power should be chosen. Changing this combination of multipliers may give better results. Since each separate multiplier has its own advantages based on the designer's considerations, it is better to use in combination than to use as single multiplier for more number of bits. Therefore, a new architecture of multiplier has been proposed by combining two multipliers based on the efficiency.

7. CONCLUSION & FUTURE WORK

Considering all facts of the multipliers above, combinations of multiplier can give good result for operands which have greater number of bits. Its dynamic power saving is a main advantage in Low power VLSI design world with great battery backup. This work can be further extended with the analysis of power and area when considered for ASIC implementation.

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