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ENTROPY ANALYSIS FOR ACHIEVING HIGH COMPRESSION RATIO

¹S.SARAVANAN, ²R.VIJAY SAI, ³R.SILAMBAMUTHAN, ⁴E.DEEPA, ⁵G.ELAKKIYA ⁶HAR NARAYAN UPADHYAY

^{1,2}Asst. Prof., School of Computing, SASTRA UNIVERSITY, Thanjavur, India -613402

^{3,4,5}M.Tech. VLSI, School of Computing, SASTRA UNIVERSITY, Thanjavur

⁶Assoc. Dean, School of Electrical and Electronics, SASTRA UNIVERSITY, Thanjavur

E-Mail: saran@core.sastra.edu, silambamuthan@gmail.com, hnu@ece.sastra.edu

ABSTRACT

Deciding test data volume is a major challenge in present System on Chip (SoC) design. Compaction of test data volume results in high compression ratio. Entropy analysis plays a vital role in such cases. Entropy is measurement of the amount of information contained in the data set. Entropy calculations tell the need of how much test data vector that can be compressed. This paper is based on finding entropy calculations to achieve maximum test data compression. Further, entropy study for unspecified bits (don't care bits) and complement method are also explored which result in high compression ratio. Entropy analysis for different symbol length partitioning is done. For the fixed-length symbol, one fill and zero fill algorithm is applied for unspecified bits, reducing the entropy. The proposed method is successfully tested on ISCAS89 which achieves maximum compression ratio

Keywords: Entropy Analysis, Unspecified Bit, One And Zero Fill Techniques, Test Data Compression

1. INTRODUCTION

In VLSI one of the major challenges is deciding the amount of test data volume especially in System on Chip (SoC) designs. The test cost of a chip is directly affected which in turn increases the testing time and memory requirements. Reducing the test data volume using compression techniques is the best approach for dealing this problem. The test data are stored in compressed form and used for Circuit under Test (CUT).

In the literature, several test data compression schemes have been proposed. To both test stimuli and test response, some of these schemes are applicable, while others consider compression of test stimuli or test response only. In this paper, we study the amount of test data volume needed and how much compression can be achieved.

To achieve compression, compression schemes can be regarded as an encoding of data into a smaller size than the original data. The output of the compression scheme is called as compressed data or encoded data. The sets of bits operated are called blocks. Depending on how test data are handled by the scheme, test vector compression schemes can be classified into different categories.

Fixed to fixed category is defined as scheme encoding into a fixed number of input bits into a fixed number of encoded bits. Fixed to variable category is a scheme that encodes a fixed number of input bits into a variable number of encoded bits. The other two possibilities include encoding a variable number of input bits into a fixed number of encoded bits, belonging to variable-to-fixed and encoding a variable number of input bits into a variable number of input bits into a variable number of encoded bits, belonging to variable-to-fixed and encoding a variable number of input bits into a variable number of encoded bits coming under variable to variable category. Among these categories fixed to fixed scheme is chosen in this paper for entropy analysis.

2. EXISTING METHODS

Various research literatures focus on the number of compression techniques. Entropy method is one among them which is effectively utilized to achieve high test data compression. Entropy is a measure of the uncertainty in a system. It tells about the minimum average number of bits

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that reproduce the transmit data and gives the theoretical limit on the maximum amount of data which can be compressed [1].

An example of a fixed-to-fixed scheme is conventional Linear Feedback Shift Register (LFSR) reseeding [2], in which each fixed size test vector is encoded as a smaller fixed-size LFSR seed. To fill more scan chains with fewer tester channels, each clock cycle fall into this category by using techniques that use combinational expanders with more outputs than inputs. These techniques use linear combinational expanders such as XOR networks as discussed in [3], as well as nonlinear combinational expanders discussed in [4] and [5]. In paper [4] there are two alternatives possible for techniques that do not have a complete encoding. Bypassing the dictionary requires adding an extra bit to each codeword to indicate whether it is coded data or not or either the automatic test pattern generation (ATPG) which should be constrained, so that it only generates test data that are contained in the dictionary as in [5].

The paper is organized as follows: The entropy analysis for test data is described in section 3. It also shows how to calculate entropy and compression ration based on partition the test data. Proposed method is described in section 4. It shows how to partition test data, filling unspecified bit with suitable specified bit and calculating entropy and compression ration. Experimental results are described in section 5.

3. ENTROPY ANALYSIS FOR TEST DATA

The entropy analysis for test data is based on dividing test data into symbols which is described below. For fixed-to-fixed and fixed-tovariable codes, the test data are divided into same symbol length. The value of entropy changes corresponding to the symbol length of the test data. Entropy is calculated for the given symbol length of the test data. This calculation will tell a theoretical limit on the maximum compression for the given test data.

This is explained by the following Table 1. The table shows that the test data are divided into 4 bits length. It shows total number of vector size is 4 and it contains 24 test data. It is partitioned into 6 groups each with 4 bit test data. Probability for given test data is calculated.

			-	-		
Vector1	0010	1111	1101	0000	0110	1100
Vector2	0010	1111	1101	0000	0011	0101
Vector3	1111	1111	1111	0011	0011	1011
Vector4	1111	1111	1111	0011	1100	1011

Table 1 - Test data divided into 4-bit

 Table 2- Probability Table for Symbol Length of 4

i	Symbol(X _i)	Frequency	Probability		
1	0010	2	0.0833		
2	1111	8	0.3333		
3	1101	2	0.0833		
4	0011	4	0.1667		
5	0110	1	0.0417		
6	1100	2	0.0833		
7	0101	1	0.0417		
8	1011	2	0.0833		
9	0000	2	0.0833		
Entropy = 2.83 Maximum Compression Ratio =29.13%					

In Table 2 the probability of occurrence of each unique 4-bit symbol is shown. Note that rather than the classical definition of probability as the chance of occurrence, the term "probability" here refers to the actual frequency of the symbol with respect to the total number of symbols in the data. The column "probability" is calculated by dividing the frequency with the total number of blocks in the test set, and the column "frequency" shows the number of times each symbol appears in the test set.

The test set entropy is calculated from the probabilities of occurrence of unique symbols using the formula $H = -\sum p_i \log_2 p_i$, where i=1 to n, and 'pi' is the probability of occurrence of symbol 'xi' in the test data and 'n' is the total number of unique symbols. This entropy is calculated and shown in the last row of Table 2. The minimum average number of bits required for each codeword is given by entropy. Thus, the maximum compression that can be achieved is given by (symbol length – entropy)/ (symbol length), which in this case is equal to (4 - 2.83)/4 = 29.13%.

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4. PROPOSED METHOD

In this section, the proposed method shows how to increase compression ratio using the following proposed algorithm. In this section, the proposed method shows how to increase compression ratio using the following proposed algorithm.

Steps for Proposed algorithm:

1. Test data partitioning and symbol creation

2. Take complement for similar sequence of zero's and one's among the partitioned test data vector

3. Calculate the value for entropy and maximum compression ratio from given formula

From the above proposed algorithm the Initial step needs to be considered for proper partition and its corresponding symbol length. The Table 3 represents the proposed method probability table, for symbol length of 4. That shows how the compression ratio is increased for the above Test Set (Table 1).

 Table 3-Proposed method of probability table for symbol
 length of 4

i	Symbol(X _i)	Frequency	Probability		
1	0000	10	0.4167		
2	0011	6	0.25		
3	0010	4	0.1667		
4	0110	1	0.0417		
5	0101	1	0.0417		
6	1011	2	0.0833		
Entropy = 2.14 Maximum Compression Ratio =46.55%					

5. EXPERIMENTAL RESULTS

This section describes the experiment performed to asses the efficiency of achieving entropy analysis for maximum compression ratio. This technique is based on partition and complement method. The proposed method is implemented using C language and tested with full scan version of the ISCAS89 benchmark circuits. Test patterns used in these experiments were obtained by using Mintest dynamic compaction algorithm [6]. All the provided test patterns target at 100% fault coverage.

In the zero filling the don't care bits are replaced by the zero's. Similarly in the one filling the don't care bits are replaced by the one's. The Table 4 represents entropy analysis of ISCAS89 benchmark circuits using ZERO filling technique. Similarly the Table 6 represents the entropy analysis of ISCAS89 benchmark circuits using ONE filling technique.

Table 4- Entropy Analysis using Zero Fi	lling
(Existing method [A])	

Circuit	Test Size	Symbol Length		
		4	6	8
\$5378	23754	47.63%	48.38%	51.29%
S9234	39723	46.84%	48.26%	48.58%
S13207	165200	57.04%	81.72%	82.20%
S15850	76986	65.49%	66.08%	66.77%

 Table 5 - Entropy Analysis using Zero Filling
 (Proposed method [B])

Circuit	Test	Symbol Length		
	Size	4	6	8
85378	23754	56.88%	52.19%	53.77%
89234	39723	50.60%	49.76%	49.73%
S13207	165200	60.73%	82.26%	83.48%
S15850	76986	68.67%	67.68%	67.91%

Figure 1 - Entropy analysis for Zero Filing



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Table 6 - Entropy Analysis using One filling [A]

Circuit	Test Size	Symbol Length		
		4	6	8
S5378	23754	48.43%	49.78%	21.73%
S9234	39723	41.54%	44.72%	51.03%
S13207	165200	78.18%	77.60%	78.89%
S15850	76986	56.45%	57.98%	58.48%

Table 7 - Entropy Analysis using One filling [B]

		Symbol Length			
Circuit	Test Size	4	6	8	
S5378	23754	56.27%	53.83%	53.12%	
89234	39723	49.50%	46.50%	46.60%	
S13207	165200	79.72%	78.27%	80.35%	
S15850	76986	61.39%	60.72%	59.95%	





6. CONCLUSION

One of the major challenges in SoC is the amount of test data volume required to achieve high compression ratio. In this paper entropy study is considered for realizing this requirement. Entropy theory calculates theoretical limitations for the amount of test data compression. This can be achieved with various fixed symbol length coding techniques. The proposed method deals with complement technique to attain high compression ratio, which is based on zero fill and one fill techniques. Experimental results for the ISCAS89 benchmark circuits proved that maximum compression ratio is significantly achieved.

REFERENCES:

- T. Cover and J. A. Thomas, *Elements of Information Theory*, 2nd ed. Hoboken, NJ: Wiley, 1992.
- [2] B. Könemann, "LFSR-coded test patterns for scan designs," in *Proc. Eur.Des. Test Conf.*, 1991, pp. 237–242.
- [3] I. Bayraktaroglu and A. Orailoglu, "Test volume and application time reduction through scan chain concealment," in *Proc. Des. Autom. Conf.*, 2001, pp. 151–155.

[4] S. Reddy, K. Miyase, S. Kajihara, and

- I. Pomeranz, "On test data volume reduction for multiple scan chain designs," in *Proc. IEEE VLSI Test Symp.*, 2002, pp. 103–108.
- [5] L. Li, K. Charabarty, and N. A. Touba, "Test data compression using dictionaries with selective entries and fixed-length indices," *ACM Trans.Des. Automat. Electron. Syst.*, vol. 8, no. 4, pp. 470–490, Oct. 2003.
- [6] LHamzaoglu and J.H.Patel,"Test set compaction algorithms for combinational circuits"*Proc of CAD*. Pages 283-289, Nov 1998