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TRANSITION BASED INPUT TEST VECTOR PARTITIONING FOR LOW POWER SWITCHING ACTIVITY

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ABSTRACT

Present complexity of System on Chip (SOC) has brought new challenges in low power design and testing. This shows that huge test pattern and its corresponding switching activity are one of the major problems. Due to this large number of test patterns the data transition time is also increased. More switching is also proportional to more number of transitions. This paper considers the problem of switching activity in scan based test pattern. This proposed approach is based on reducing the huge switching activity by partitioning the test vectors into groups. The number of transition is identified in each partition group. The groups having zero transition have lesser switching activities, so they are not considered equally with transition group for testing. Thus the test run time and number of switching is minimized. This in turn reduces the power consumption for testing. The proposed technique tested on ISCAS89 shows the significant reduction in overall switching activity of the test pattern.

Keywords: *Test Pattern, Transition And Non-Transition Pattern, Switching Activity*

1. INTRODUCTION

Today's System on Chip (SoC) complexity continues to grow in size and complexity. This evaluation showing two major drawbacks of testing are the area overhead and power dissipation. As per the above assessment the power dissipation is directly proportional to the amount of switching activity of the design [1]. This also increases test data volume and the cost of the manufactured chip testing in the semiconductor industry. This led to exponential increase in power consumption that has reached the limits of design reliability. This huge integrated complexity challenges the scan based testing of sequential circuits. The flip-flops used in scan based design have become one of the major power consuming devices. Shift operation for loading and observing the test data leads to excessive transition in the corresponding flip-flop. This excessive transition in primary input increases the power consumption and reduces correlation between consecutive test pattern. This also includes the unnecessary switching activities of circuit signals.

Power dissipation achieved in the test mode operation is much higher than normal mode of design operation [2]. In normal mode operation very small design portion of the flip-flops will change the value during each and every clock pulse. But in test mode operation huge number of flip-flops will change the value. Due to this huge change in flip-flops more switching activity is occurred. This increases the problem of huge heat dissipation and more transition time.

Each and every primary input contains the combination of '0', '1' and 'X' (unspecified). Thus it is possible to identify the specified bit and unspecified bit in the given test patterns. Specified bits are the collection of '0' and '1' combination. In unspecified bits, only 'X' is identified. These unspecified bits are more in test patterns compared with specified bits. Every unspecified bit is considered to specify by assigning random values of '0' and '1'. Thus this will lead to excessive of switching activity in scan based design.

2. POWER DISSIPATION

Two main sources of power dissipation are considered in CMOS circuits design. They are Dynamic power dissipation and (PD) and Static power dissipation (PS). The total power consumption said to be the addition of all the above two power consumption.

This is given as P = PD + PS [3]

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The dynamic power dissipation is one of the main dominating power dissipation in present CMOS technologies. It is achieved due to the switching of transistors in the design. This is composed of both switching power and short circuit current. Switching power is dissipated by the charging and discharging of the load capacitance at the output of the CMOS. Charging and discharging of the capacitance is results on logic transition. Thus huge charging and discharging will result on huge logic transition in the design. Short circuit current achieved by both pMOS and nMOS network are partially ON.

Static power dissipation is achieved due to sub-threshold conduction through OFF transistors, tunneling current through gate oxide and leakage through reverse-biased diodes.

3. EXISTING METHODS

The problem of reducing power dissipation in test data has been attended from several different angles in recent literatures. Many techniques for reducing power consumption during scan testing have been summarized [4].

Test data and its power dissipation are reduced by applying compression method [5]. Dual speed (DS) Linear Feedback Shift Register (LFSR) is used to reduce power dissipation [6]. This deals with slow speed LFSR and normal speed LFSR. Thus depending upon transition density DS-LFSR is used. Overlapping slice set technique is used in [7]. This paper shows that there is no transition in the overlapping block. This scheme is also used to reduce the number of specified bits and the number of transitions at the same time. Low power scan testing with compression technique is used in [8]. This paper represents unspecified bits to zero for achieve Golomb codes. But all the above said existing method needs extra hardware like compression, decompression, slow LFSR method. This will increase the complexity of the design.

The unspecified test patterns with random value will increase the transition switching. Thus this shows the proportionality of unspecified value with transition. This is also proportional to the time of the scan chain flip flops.

4. PROPOSED METHOD

In this section, the proposed method shows how to reduce the dynamic switching activity [9] in scan based designs. Testing the designs for low power switching activity depends on the number of transitions that occurs in the scan chain of the design. Due to unspecified and specified values of the test pattern, it is necessary to identify its corresponding transition. It can be identified into two types namely transition and non-transition test patterns. In transition pattern the test pattern is combination of '0' and '1' only. Thus there is a possibility of switching. In non-transition the test patterns is the combination of '0' with 'X' or '1' with 'X' or 'X' with 'X'. Thus no switching activity is performed.

Following example illustrates the selection procedure of the proposed low power switching scheme. Given test patterns T1 contain 16 test vectors with the combination of '0', '1' and 'X'. T1 = 0 0 1 0 1 1 1 X X X X 1 0 0 0 X. For example T1 contains the partition size as 4. Thus 4 partition with each 4 test vectors were separated as shown in this discussion. As per the proposed scheme the final given test pattern is grouped as 1 transition partition (T-P) and 3 non-transitions partition (NT-P). Unspecified values were considered for low power test vectors, by assigning the A-fill method. [10]

T1= | 0 0 1 0 (P1) | 1 1 1 X (P2) | X X X 1 (P3) | 0 0 0 X (P4) |

T1= | 0 0 1 0 (T-P) | 1 1 1 1 (NT-P) | 1 1 1 1 (NT-P) | 0 0 0 0 (NT-P) |

After identifying the transition and non-transition partition for a given test pattern, the next phase is to calculate the switching activity of test patterns. Scan chain length (L) and scan test pattern (TP) are considered for calculating switching activity. Scan test pattern is applied to each and every flip-flop. If the scan test pattern is applied to any flip-flop, it will activate one after another in the flip-flop like $TP_i=TP_{i,1}\ TP_{i,2}\ TP_{i,3}\ \ldots.TP_{i,L}$. It shows that $TP_{i,2}$ is scanned after $TP_{i,1}$ only. Thus scan test pattern depends upon the previous flip-flop. Weighted Transition Metric (WTM) is the difference between sizes of the scan chain to position of transition [11]. Power dissipation is applied to any two vectors by counting the number of weighted transitions as per equation (1)

This is denoted as by the following equation. $WTM = \sum ((L-j) . (TP_{i,j}\ XOR\ TP_{i,j+1}))$ -(1)

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Where $TP_{i,j}$ is the present scan test pattern and $TP_{i,j+1}$ is the next scan pattern in the design. If more number of scan test pattern is applied then WTM is also considered for Peak power (WTM_P) and Average power (WTM_A). Peak power is calculated by the maximum value of WTM in 'n' number of scan test pattern. Average power is calculated by summing all test pattern with the average of 'n' test pattern.

Following example illustrates the calculation procedure of WTM. Let the given test pattern set T contains 5 bit in one test pattern. Test vector (T) = 0 1 1 0 1. Its corresponding weighted transition metric WTM value is 7.

As per the following algorithm the value of WTM is calculated for test vectors. Initial test patterns for each vector are known as Vectorsize. Each test vector is separated with number of partition known as partitionsize. Total numbers of partitions were identified as 'n'. If the partition contained non-transition bit then include A-fill and no need calculate WTM. But if that partition contains transition bits then need to calculate WTM.

Algorithm PartitioningBasedWTM (Testvector, Vectorsize, Partitionsize)
Testvector – sequence of digits of size 'vectorsize'
Vectorsize – size of vector
Partitionsize – size of Partition

1. Partitionsize[ ] ← call split (Testvector, Partitionsize, n)
   /* Split vector into 'n' partitions */
2. for each partition p in partition [ ] do
   if p contains only ones or only zeros or combination with Xs
   action1= nontransition
   action2 = include A-fill
   call don't_do_wtm()
   elseif p contains the combination of zeros and ones
   action1 = transition
   call do_wtm()
   endif
   endfor

5. EXPERIMENTAL RESULTS

This section describes the experiment performed to asses the efficiency of achieving low power switching activity technique based on partition method. The proposed method is implemented using C language and tested with full scan version of the ISCAS89 benchmark circuits. Test patterns used in these experiments were obtained by using Mintest dynamic compaction algorithm [12]. All the provided test patterns target at 100% fault coverage.

By assigning the partition value as n=20 the total transition power is reduced to 94% compared with normal transition power as in Fig.1. Depending upon the transition and non-transition value the scan power is reduced significantly. Average power and peak power of scan based power consumption is reduced up to 98% in Fig.2. This proposed method is suitable for all the ISCAS89 benchmark circuits.

Table 1 shows the experimental result for non-transition partition (NT-P) power reduction. This shows considerable reduction achieved over normal test patterns. In Table 2 experimental results for Peak and average power for Golomb fill (GF [8]) is shown. Table 3 shows total and average power values of reduced power consumption using for different values of partition and compared with MT-fill [8].

6. COCLUSION

The present challenge of reducing power is the most important task in VLSI testing particularly in the field of scan cell test patterns. This paper proposes about transition and non-transition partition technique for minimizing transition switching activity in scan based design. It is seen that Weighted Transition Metric (WTM) reduces Average power as well as Peak power. Experimental results for the ISCAS89 benchmark circuits show that dynamic power is reduced significantly up to 94% in total power and 98% in average, peak power. Considerably, minimized power switching transition and low data transition time is achieved

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Table 3. Results on various values of partitioning

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APPENDIX:

ISCAS Circuit	n=20	n=40	n=60	n=80	n=100
S5378	51%	23%	21%	10%	34%
S9234	32%	21%	22%	25%	10%
S15850	46%	28%	26%	21%	20%

Table 1. Experimental results of non- transition partition (NT-P)

ISCAS Circuit	No of test pattern	No of bits per pattern	Total number of bits	Aver. Power GF [8]	Peak power GF [8]
S5378	111	214	23754	3336	10127
S9234	159	247	39273	5692	12994
S15850	126	611	76986	20742	81832

Table 2. Experimental results for Peak and average power for GF [8]

Circuit	MT-fill [8]	MT-fill [8]	n=20		n=40		n=60		n=80		n=100	
	Average	Peak	Average	Peak	Average	Peak	Average	Peak	Average	Peak	Average	Peak
S5378	2435	9531	99%	98%	97%	95%	95%	92.2%	92%	86%	88%	78%
S9234	3466	12060	98%	98%	98%	97%	94%	93%	92.2%	87%	89%	75%
S15850	13381	63478	99.2%	98.4%	97.6%	98%	94.2%	93.2%	91%	85.7%	86%	73.8%

Table 3 Total and average power values of reduced power consumption using for different values of partition and compared with MT-fill [8].

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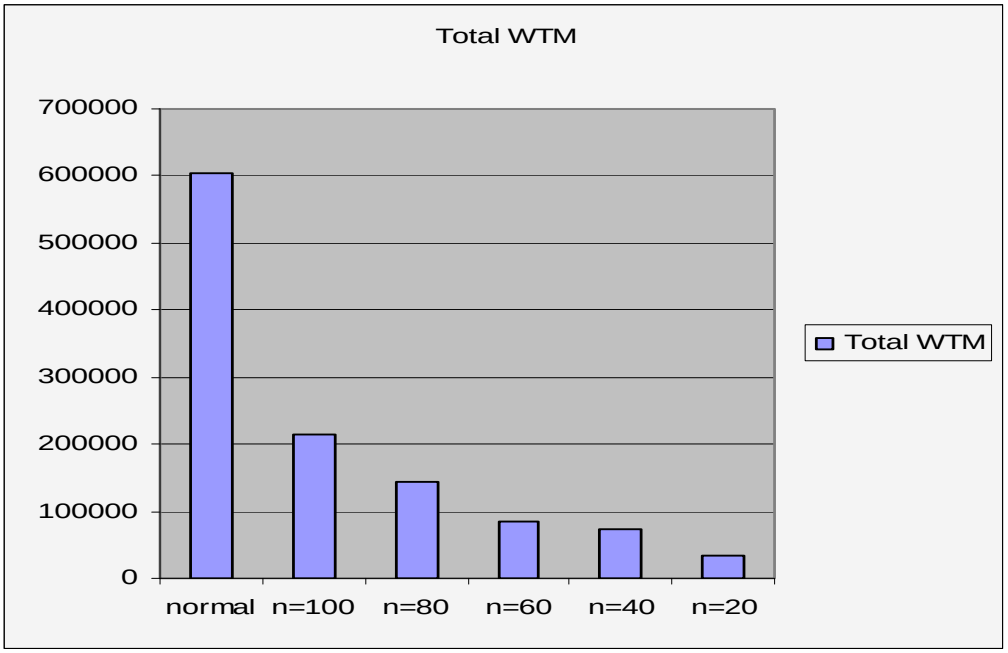

Fig.1 Total WTM for S5378

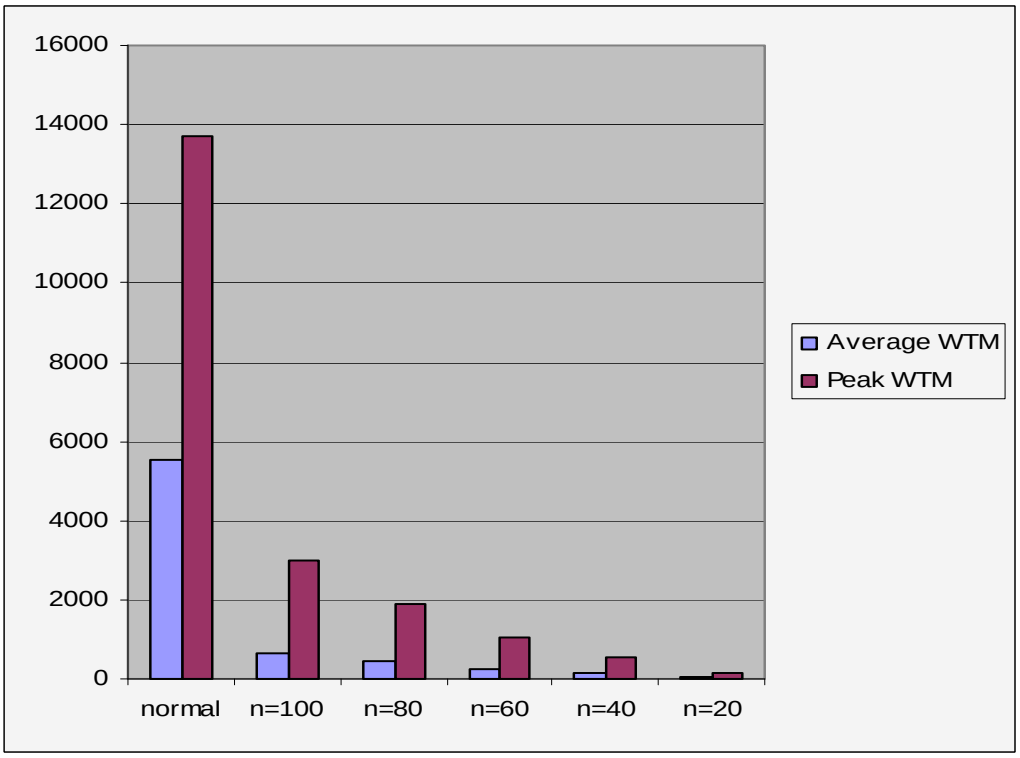

Fig.2 Average and Peak WTM for S5378