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FPGA IMPLEMENTATION OF SCALABLE BANDWIDTH SINGLE CARRIER FREQUENCY DOMAIN MULTIPLE ACCESS TRANSCEIVER FOR THE FOURTH GENERATION WIRELESS COMMUNICATION

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ABSTRACT

In this paper, design and implementation of 4G SC-FDMA transceiver on FPGA is done and explained. Long Term Evolution (LTE) is next generation mobile communication standard from 3GPP, it is based on OFDMA) in Downlink Transmission and SC-FDMA in uplink Transmission. SC-FDMA is based on Frequency Division Multiple Access scheme. When compared with other multiple access scheme, it deals with the multiple users in a shared communication systems. SC-FDMA is also called as linearly pre-coded OFDMA, in the sense it has the additional discrete time Fourier transform (DFT) processing in SC-FDMA. The main advantage of SC-FDMA over OFDMA is low Peak to average power ratio, so the power transmission is low when compared. This work proposes a run time reconfiguration architecture for the SC-FDMA. Where the bandwidth and sub carrier mapping schemes of SC-FDMA can be changed. Real time FPGA implementation results are captured in the Chipscope Pro Embedded Logic analyzer.

Keywords: *Orthogonal Frequency Division Multiple Access(OFDMA), Single Carrier-Frequency Division Multiple Access (SC-FDMA), Long Term Evolution (LTE), Discrete time Fourier transform (DFT)*

1. INTRODUCTION

3GPP standard is focused on next generation cellular systems called Long Term Evolution (LTE)[1-2]. The scalable bandwidth of LTE is 1.5MHz- 20MHz. The LTE features are high peak data rate, flexibility of spectrum usage, low latency times, higher capacity per cell, etc. LTE is based on OFDMA in the downlink and SC-FDMA [1-3] in the uplink. LTE adopted SC-FDMA technique which is used in the uplink transmission of high data rate.

Frequency division multiple access scheme is used in SC-FDMA and it deals with the multiple users on the basis of shared communication. SC-FDMA is same as that of OFDMA system except the additional DFT processing. Single Carrier Modulation and Frequency domain equalisation are the techniques used in SC-FDMA which is same as that of OFDMA, in overall performance and complexity of the system. The guard intervals with cyclic repetition are inserted between the blocks of SC-FDMA to efficiently eliminate time spreading between the blocks. The transmission bandwidth is divided into multiple subcarriers in parallel maintaining each subcarrier in frequency selective channel by utilising cyclic prefix or guard intervals. Utilisation of cyclic prefix prevents from the inter-symbol interference between the blocks of SC-FDMA. The linear convolution of the multipath channel is transformed into circular convolution, which enables the receiver to equalize each subcarrier present in the channel by scaling with a complex gain factor. The main advantage of SC-FDMA over OFDMA is low Peak to Average Power Ratio (PAPR). As it has got lower PAPR, the power efficiency is high.[4]

In the previous work of SC-FDMA transceiver the physical implementation of the process is not done in FPGA, whereas in this the implementation work is done and studied.

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The present work is concerned with the design and implementation of SC-FDMA transceiver for the 4th generation wideband communication on a single FPGA. The present work shows the schemes to change the bandwidth of the SC-FDMA transmitter at run time. The FPGA based implementation of subcarrier mapping and the relative hardware requirement is evaluated. The rest of the paper is organized as follow. Section 2 discusses about the SC-FDMA architecture and operation and section 3 discusses about the FPGA implementation process, section 4 gives implementation results and section 5 presents the conclusions and future scope.

2. SC-FDMA ARCHITECTURE

The transceiver of SC-FDMA is shown in the figure 1.It consists of following blocks, bit stream generation, bit to constellation mapping (QPSK), DFT, sub-carrier mapping, IFFT in the transmitter and the inverse blocks in receiver.

In the transmitter part of SC-FDMA, binary input signals are mapped into QPSK or QAM symbols. The modulated symbols $\{X_n\}$ are in the form of blocks each containing n symbols. The next step after the modulation is to perform N point DFT which transform the time domain symbols $\{X_n\}$ to frequency domain form DFT is a kind of discrete transform which is used in Fourier analysis. DFT transforms one function into another function which is called as the frequency domain representation $\{X_k\}$.[5]

DFT equation is represented as,

$$X_k = \sum_{n=0}^{N-1} x_n e^{\frac{-2\pi ikn}{N}} \quad \text{k=0,1...N-1} \qquad (1)$$

Inverse discrete Fourier transform equation is represented as,

$$x_n = \frac{1}{N} \sum_{k=0}^{N-1} X_k e^{\frac{2\pi ikn}{N}} \quad \text{n=0,1....N-1} \qquad (2)$$

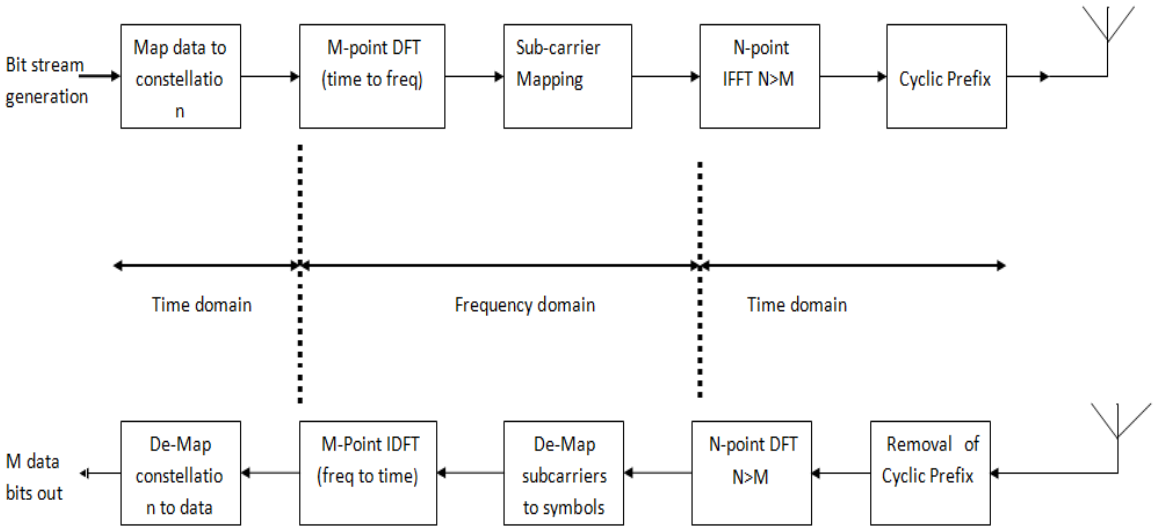

Figure 1 SC-FDMA Transceiver architecture

The DFT input is of finite sequence of real or imaginary numbers. The symbols formed in time domain from the QPSK are changed to frequency domain using DFT.

Sub-carrier mapping process done to the output the N-point DFT. Sub-carrier mapping is padding of zeros among the DFT outputs to match with size of IFFT in the systems. Depending on the bandwidth of the SC-FDMA number of subcarrier changes from the 72 (for 1.5MHz) to 1200 (for 20MHz).

The two types of sub-carrier mapping are[6]

1. Localised mapping
2. Distributed mapping

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Localised Mapping: The output from the DFT is mapped to a subset of consecutive subcarrier, confining only to a fraction of system bandwidth. In the localised mapping the zero padding process is done either at the first or last, but the outputs of the DFT will be placed in the sequence order without any interchanging.

Distributed Mapping: The output of the DFT is assigned, non-continuously to the sub-carrier, over the entire bandwidth. In this case the zero padding operation is performed by calculating the L-1 zeros and the output data from the DFT are stored according to the size. The zero padding is done equally over the entire bandwidth. It is also called as Interleaved Mapping.[7] Both subcarrier mapping procedures can be seen in the figure 2.

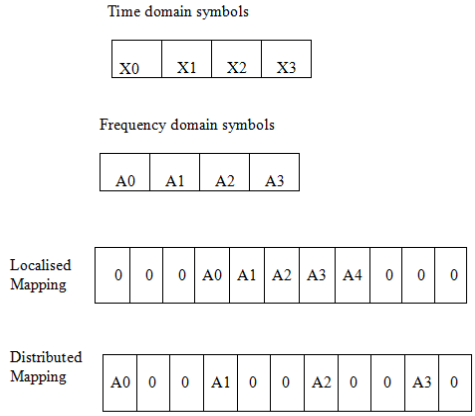

Figure 2 Sub carrier mapping

After the mapping process, the frequency domain signals are transformed to time domain using a N (M<N) point Inverse fast Fourier Transform (IFFT) process. The cyclic prefix block is present next to the IFFT block. The transformed data are transmitted to the receiver blocks. The inverse operation of each block takes place in the receiver part.

At first the cyclic prefix is removed, then the signal is converted to frequency domain using M point FFT. Subcarrier de-mapping is done. The de-mapped signal is given to the IDFT to get the time domain signal back. The IDFT output is given for QPSK or QAM demodulation. After the demodulation the receiver generate the final bit stream.

3. SC-FDMA IMPLEMENTATION ON FPGA

The SC-FDMA transceiver is implemented on the Xilinx Virtex-5 ML501 board using Xilinx ISE 12.1[8] design suite. The modulation scheme preferred for the system is QPSK.

First a LFSR is designed to work as the input bit stream generator for the transmitter. . LFSR is using 16 bit shift register whose input bit is linear function of its previous state. XOR is the only linear function of single bit so input bit of the shift registers are driven by XOR. The input bit stream is mapped into In-phase and Quadrature-phase symbols by tapping two MSB bits from the LFSR. Each QPSK real and imaginary symbol is of 16-bit size.

The 32-point DFT block is generated using Xilinx IP Core generator. The 16-bit output from the QPSK is given as the input for the DFT. The core generated DFT consists of scaling factor, xn_index, xk_index, fwd_inv and enable pins. The scaling factor, xn_index and xk_index is of 6-bit. If the DFT operation is of forward transform then the fwd_inv is given 1. when the xk_index starts counting the output of the DFT is generated.

For the implementation distributed sub-carrier mapping is selected. It was found that distributed sub-carrier mapping consumes less FPGA resources than the , localized subcarrier. In case of localized subcarrier mapping there is need of intermediate buffer memory which will store the DFT output until the all the zeros need to padded before the DFT output are padded. The sub-carrier mapping operation is done using a counter and multiplexer. Two 16-bit multiplexer are used, one for the real data and other for imaginary data .The counter output is given as the input for select line in multiplexer. Another input of the mux is given as constant zero value. The counter is a 2-bit counter and after the three clock cycles the output of the counter will be high. Than a multiplexer selects the input from the DFT otherwise a zero will be sent to IFFT block.

It is to be noted that in order to pad L-1 zeros between two consecutive DFT output, the counter will run at clock speed of L×DFT clock rate. In our implementation the DFT is working at the 50 MHz and taking L=4 as per the SC-FDMA standard than the counter and IFFT are working with 200MHz. the According to the counter output the selection process starts and the output is comprise of three

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zeros and on DFT output data. The IFFT blocks accept input data one more clock cycle after it is triggered to start. In order to provide the DFT output at right time at shift register is designed with one clock cycle delay and the output from the mapping process is given as the input for the shift register. The IFFT is fed with the output of shift registers.

The output from the shift register is given to the IFFT. IFFT block is generated using the IP core with the inclusion of cyclic prefix with size 32. The core generated IFFT consists of scaling factor, xn_index, xk_index, fwd_inv,cp_len and enable ,nfft,nfft_en ports. The scaling factor is of 8-bit, xn_index , xk_index, cp_len are of 7-bit. If the IFFT operation is of inverse transform then the fwd_inv is given 0. when the xk_index starts counting the output of the IFFT is generated. In order to runtime reconfiguration of FFT and IFFT from 2048 point to 128 point nfft port is used . The value of nfft is $\log_2$ (point size). This port is only used with run-time configurable transform point size. nfft_we is write enable for nfft (active high): asserting nfft_we causes the core to stop all processes and to initialize the state of the core to the new point size on the nfft port. This port is also only used with run-time configurable transform point size. The nfft port is 11 bit wide for the 2048 point FFT and IFFT. The value of nfft and nfft_we ports are controlled through the external controller to activate 2048,1024,512,256 and 128 value.

At the receiver side first the cyclic prefix is excluded by using an 32-counter which counts for 32 clock cycles and after that it sets high as output. After that FFT block coverts the signal into the frequency domain. The de-mapping process is done using a 3-bit counter. The de-mapping process is used to reduce the 128 point to 32-point according to the IDFT used in the receiver part. This counter starts counting the output from the 128-point FFT and gives the output as high when the output should be written. The shift register is used to delay for one clock cycle and the outputs are given to the IDFT.

The outputs from the shift registers are given to the IDFT and operation of IDFT is same as above specified DFT process. The 128-pint data are reduced to 32-point. The outputs from the IDFT is taken and the QPSK demodulation process is done. The relevant 0 and 1 is given as output according to the 16-bit data of IDFT for the real and imaginary. After the QPSK demodulation process is done a MUX is designed to convert In-phase and Quadrature phase demodulated bit stream into a single bit stream . The MUX need to operate at double the rate of the incoming data . Since the demodulated data is coming at the frequency of 200MHz the select line of MUX is operating at the 400MHz.Since 32 point IDFT generate a frame of 32 valid data at one time a 32-counter is used to show the data valid output as high till the all valid 32 data are received.

4. SC-FDMA IMPLEMENTATION AND RESULTS.

The XILIINX ISIM 12.1[9] simulator is used for the simulation and Chipscope Pro Embedded Logic analyzer [10] is used for tapping the signals going in and coming out from the FPGA in real time.
The Simulation results are shown in figure 3 to figure 5. Figure 3 show the subcarrier mapping it can be seen that out of four clock cycle three consecutive cycle the output is equal to zero but for last cycle the data is present to be fed to IFFT. Figure 4 shows the output of the transmitter. The transmitter and receiver are connected through the digital loop back. The combined transceiver output can be seen in figure 5. The data valid port is high when there is valid data at the output. From figure 6 to 8 the Chipscope pro results are given. Figure 6 shows the LFSR output in channel one and transmitter output in channel three and four. Figure 7 and 8 shows two instances of SC-FDMA signal. Table 1 shows the FPGA resource utilization summary:

Table 1. DEVICE UTILISATION SUMMARY

LOGIC UTILISATION	USED	AVAILABLE	%USED
Slice Registers	9757	28800	33%
Slice LUTs	8946	28800	31%
LUT-FF pairs	7731	10972	70%
IOBs	4	440	0%
Block RAM/ FIFO	2	48	4%
BUFG/ BUFGCTRLs	6	32	18%
DCM_ADVs	2	12	16%
DSP48Es	30	48	62%

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5. CONCLUSION AND FUTURE SCOPE

SC-FDMA Transceiver for the fourth generation broadband wireless communication is implemented on the single FPGA and the real time input and outputs are shown using Chipscope pro tool. In future a symbol equalizer will be added at the receiver side. In order to introduce software programmability of the SC-FDMA transceiver, it will be connected to an on-chip soft-core processor to control the operating frequency and bandwidth.

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SIMULATION AND IMPLEMENTATION RESULTS

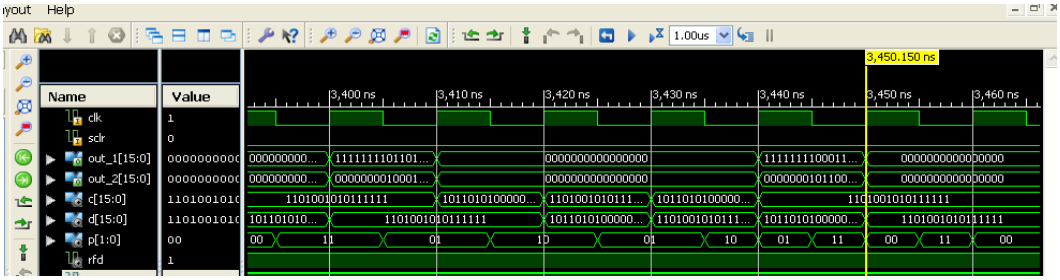

FIGURE 3 SUB CARRIER MAPPED OUTPUT FROM THE TRANSMITTER.

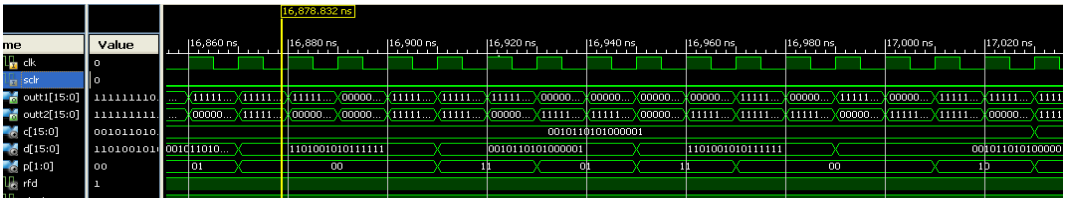

FIGURE 4 OUTPUT FROM THE TRANSMITTER

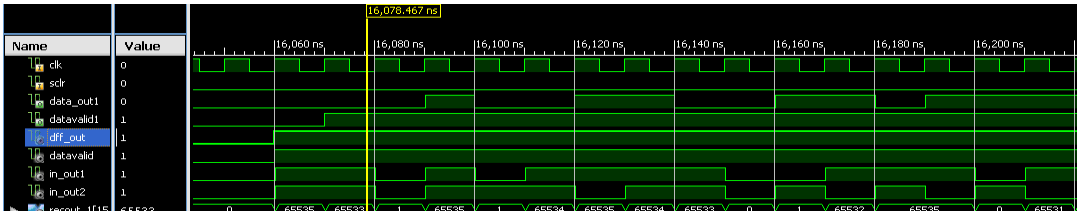

FIGURE 5 OUTPUT FROM THE TRANSCEIVER

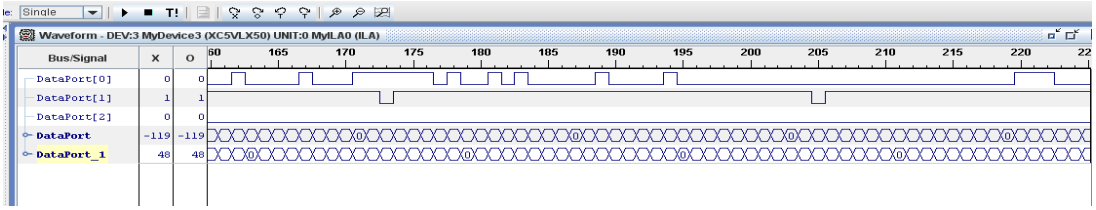

FIGURE 6 OUTPUT FROM THE TRANSCEIVER AS TAPPED BY CHIPSCOPE PRO

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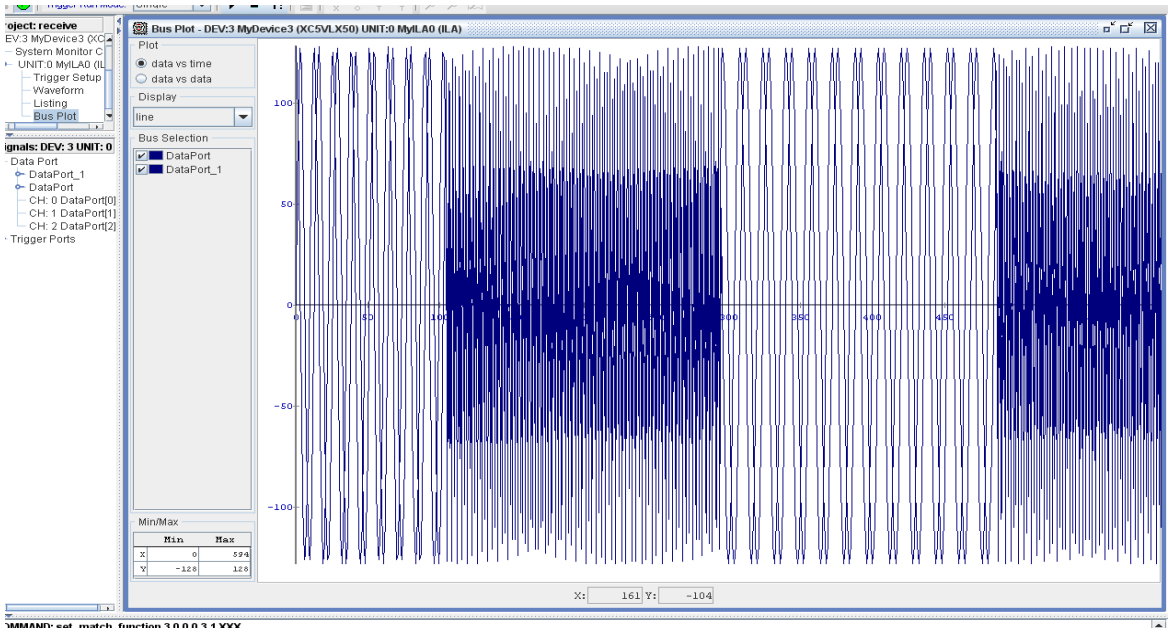

FIGURE 7 SC-FDMA SIGNAL AS TAPPED BY CHIPSCOPE PRO

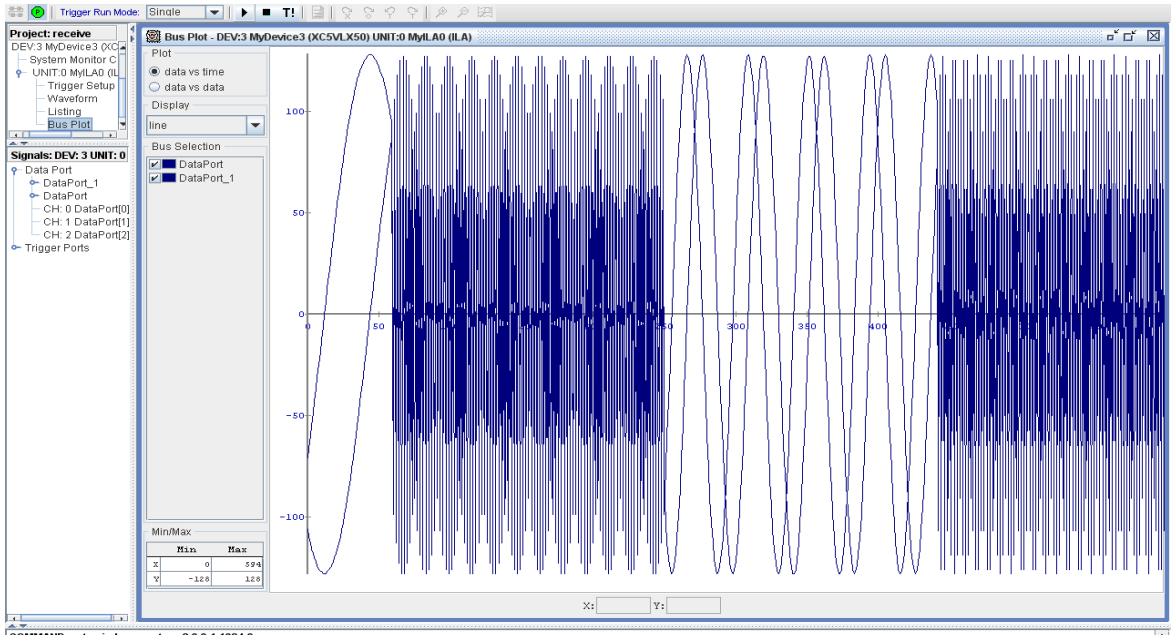

FIGURE 8 SC-FDMA SIGNAL AS TAPPED BY CHIPSCOPE PRO