COMPUTER SIMULATION OF CLASS D INVERTER FED INDUCTION HEATED JAR

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ABSTRACT

This paper deals with digital simulation of Class D inverter fed induction heater system. This system has an advantage like reduced volume and switching losses. The circuit operates under zero voltage switching. The circuit models are developed for the open and closed loop system and they are used for simulation studies. The simulation results of open and closed loop systems are presented.

Keywords: *Simulation, Class D Inverter, Induction Heater, Circuit, Simulation*

I. INTRODUCTION

Recently, with the progress of power semiconductor devices, new circuit techniques, and control schemes, researches about high-frequency circuits using advanced power devices such as MOSFET's and insulated gate bipolar transistors (IGBTs) have been many performed for high-power applications [1]–[18]. The various resonant inverters using power devices such as MOSFET's and IGBTs offer reduced switching loss by soft-switching technique and attractive possibilities in developing high-frequency operation, high efficiency, small size, and light weight. Induction heating (IH) has been a part of high-power applications and widely used in the industrial field, office automation field and electric home appliances. In particular, an IH jar, which is one of the IH applications, is used in home appliances as a cooker [3]–[5]. The requirements for the IH system are given as follows:

1) high-frequency switching;
2) high power factor;
3) wide load range;
4) high efficiency;
5) low cost;
6) reliability.

A high-frequency class-D inverter has become very popular and is more and more widely used in various applications. It must be effectively selected according to the applications in order to meet the inverter requirements under a high-frequency switching operation due to load specifications. In addition, one of the main advantages of the class-D inverter is low voltage across the switch, which is equal to the supply voltage. Thus, compared with other topologies (class-E quasi-resonant inverter, etc.) for IH applications, the class-D inverter is suited for high-voltage applications [1]. Generally, almost all IH applications use a variable-frequency scheme, pulse-frequency modulation (PFM), and pulse-amplitude modulation

(PAM) to control the output power [5], [6]. Between them, frequency modulation control is the basic method that is applied against the variation of load or line frequency. However, frequency modulation
control causes many problems since the switching frequency has to be varied over a wide range to accommodate the worst combinations of load and line. Additionally, in case of operation below resonance, filter components are large because they have to be designed for the low-frequency range. In addition, it is apt to audible noise when two or more inverters are operated at the same time with different switching frequencies. Besides, the soft-switching operating area of the zero-voltage switching (ZVS)–PFM high-frequency inverter is relatively narrow under a PFM strategy. Keeping the constant switching frequency and controlling the output power by pulse width modulation (PWM) are obvious ways to solve the problems of variable-frequency control. Therefore, class-D-inverter topologies using a PWM chopper at the input, phase-shifted PWM control, PWM technique, pulse width modulation–frequency modulation (PWM–FM) technique, current-mode

control, and a variable resonant inductor or capacitor have been proposed [7]–[11], [16]. The constant-switching-frequency operation supposes that each inverter in the applications is operating at the same frequency, making it necessary to control power without frequency variations, and this is highly desired for the optimum design of the output smoothing and noise filters. However, these control requirements and operating characteristics have considerable complexity due to the fixed switching frequency, which limits their performance [12]. In addition, if the system is operated with phase-shifted PWM control, the ZVS is not achieved at light load [13], [14]. To simplify output-power control, a full bridge zero-current switching (ZCS)–pulse-density modulation (PDM) class-D inverter is proposed [15]. The output power of the ZCS–PDM class-D inverter can be controlled by adjusting the pulse density of the square-wave voltage. However, when the output is controlled by the pulse density, like that in [15], the load current should be freewheeled, and then, the output voltage of the inverter becomes zero. As a result, the conduction losses of the inverter are caused by the freewheeling current during the freewheeling mode. Therefore, to solve these problems, this paper deals with a simple power-control scheme of constant frequency variable power (CFVP) for the class-D inverter in the IH-jar application without additional dev ices. When the class-D inverter operates at a fixed switching frequency that is higher than its resonant frequency, it can maintain ZVS operation in the whole load range. Thus, the switching losses and electromagnetic interference (EMI) are decreased. In addition, by adjusting the duty cycle of fixed low frequency, the output power is simply controlled in a wide load and line range. The advantages of a new power-control scheme are simple configuration and wide power-regulation range. It is easy to control the output power for wide load variation. In addition, the switches always guarantee ZVS from light to full loads, and a filter is easy to design by using the constant switching frequency. The proposed power-control scheme and principles of the class-D inverter are explained in detail. The theoretical analysis, simulation, and experimental results verify the validity of the class-D inverter with the proposed power-control scheme.

II. CLASS-D SERIES RESONANT INVERTER

A class-D inverter will be generally used to energize the induction coil to generate high-frequency magnetic induction between the coil and the cooking vessel, consequently, high-frequency eddy current, and, finally, heat in the vessel bottom area. The class-D inverter takes the energy from the input source. The dc voltage is converted again into a high-frequency ac voltage by the class-D inverter. Then, the inverter supplies a high-frequency current to the induction coil. Fig. 1 shows the class-D inverter system of IH jar. The class-D inverter consists of two switches *S*1 and *S*2 with antiparallel diodes *D*1 and *D*2, two resonant capacitors *Cr/*2, and an induction coil that consists of a series combination of equivalent resistance *R*eq and inductance *L*eq.

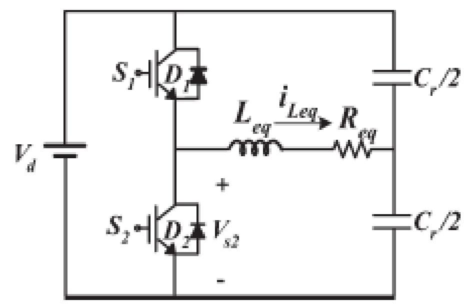

Fig.1. Class-D inverter system for IH-jar application.

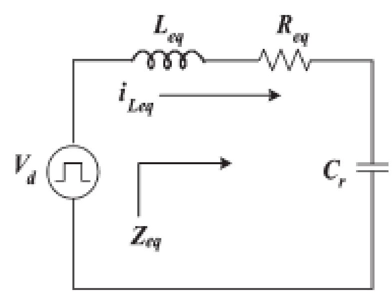

Fig.2. Equivalent circuit.

The dc input voltage is directly supplied into an inverter. Then, (S1, D1), and (S2, D2) are alternately used to administer a high-frequency current to the induction coil. Fig. 2 represents the equivalent circuit model of the class-D inverter. In particular, two switches are operated at square wave with suitable dead time between the two driving commands. The class-D inverter is operated above the resonant frequency, which means that the switches are turned on with ZVS. The steady-state analysis of the class-D inverter is based on the following assumptions.

1) All components are ideal.
2) The dc input voltage is constant in one switching cycle.

3) The effects of the parasitic capacitances of the switch are neglected.

A. Theoretical Waveforms of the Class-D Inverter

4) The load current is nearly sinusoidal because loaded quality factor QL is high enough

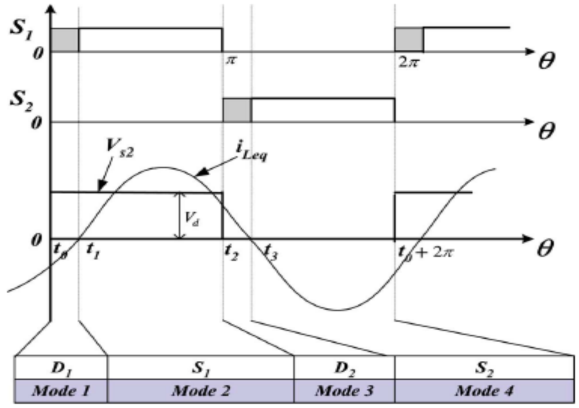

Fig.3. Theoretical waveforms of the class-D inverter.

Fig. 3 shows the theoretical waveforms including the switching signals, resonant tank voltage VS2, and load current iLeq. As shown in Fig. 3, if the switches are operated above resonant frequency, the series-resonant circuit represents an inductive load, and load current iLeq lags behind tank voltage VS2.

Therefore, load current iLeq alternatively flows through two paths,
which are Cr → Leq → D1 → S1 → Leq → Cr
and Leq → Cr → D2 → S2 → Cr → Leq.

B. Mode Operation of the Class-D Inverter

As shown in Fig. 4, four operation modes exist within one switching cycle.

1) Mode 1 ($t0-t1$).When $S2$ is turned off at $t = t0$, antiparallel diode$D1$ of $S1$ is conducted by negative load current iLeq. Then, the ZVS condition of $S1$ is obtained.

2) Mode 2 ($t1-t2$). At $t = t1$, as soon as antiparallel diode $D1$ of $S1$ is turned off, $S2$ is conducted and ZVS is achieved. During this mode, positive load current iLeq flows.

3) Mode 3 ($t2-t3$). At $t = t2$, $S1$ is turned off, similar to that in Mode 1, and antiparallel diode $D2$ of $S2$ is

conducted. During this mode, the ZVS condition of $S2$ is obtained.

4) Mode 4 ($t3-t0$). At $t = t3$, when antiparallel diode $D2$ of $S2$ is turned off, $S2$ is conducted and ZVS is achieved. During this mode, negative load current iLeq flows.

Therefore, the one-cycle operation of the class-D inverter is finished, and then, the class-D inverter continues to repeat from Modes 1 to 4.

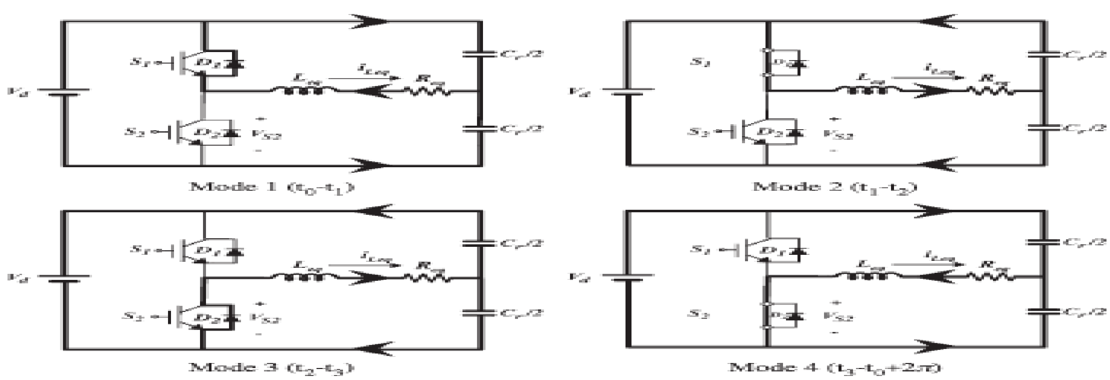

Fig.4. Operation modes of the class-D inverter

III Simulation results:

Class D inverter system is simulated and the results are presented here. Class D inverter circuit is shown in Fig 4.a.Scopes is connected to measure switch voltages and load voltage. DC input voltage is shown in Fig.4.b. Driving pulse for M1 and M2 are shown in Fig.4.c. Voltage across M1 and M2 are shown in Figs 4.d. and 4.e. respectively. Output current and voltage are shown in Figs 4.f. and 4.g. respectively.

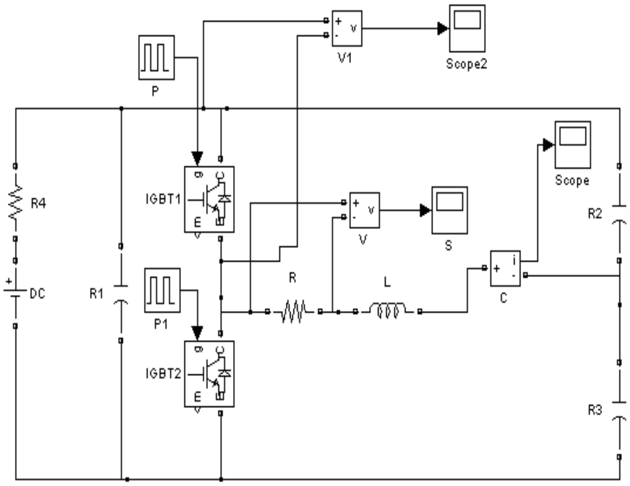

Fig.4.a. circuit diagram of Class D Inverter

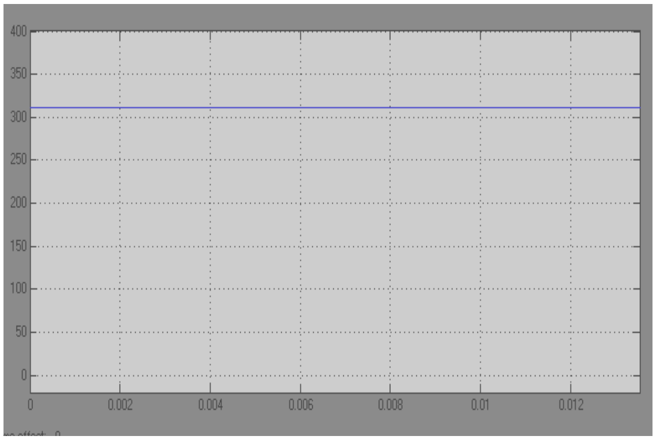

Fig.4.b. Dc Input voltage

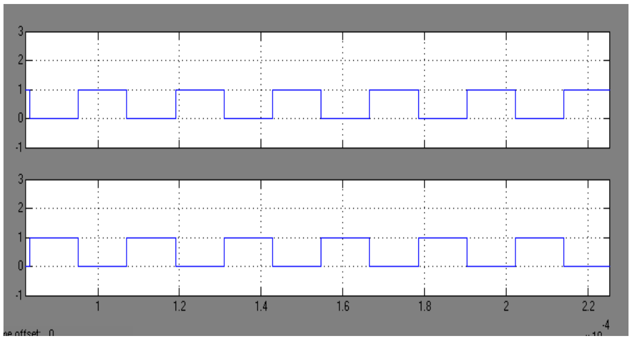

Fig.4.c. Driving pulses

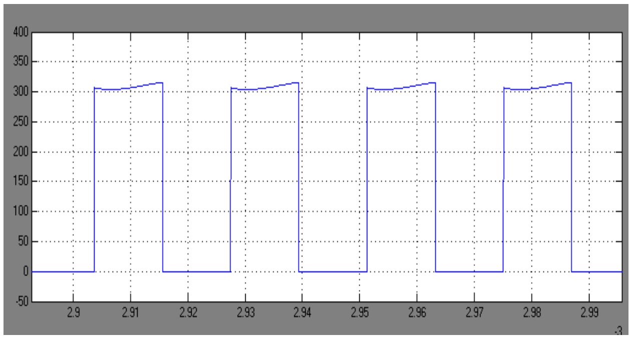

Fig. 4.e. Voltage across M2

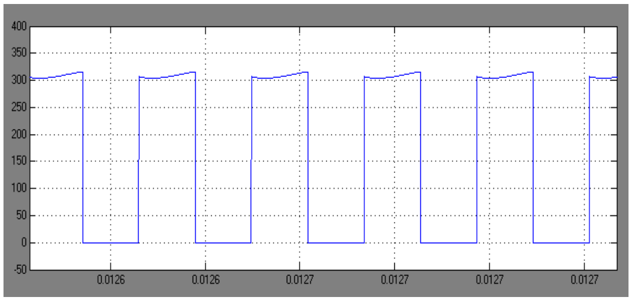

Fig.4.d. Voltage across M1

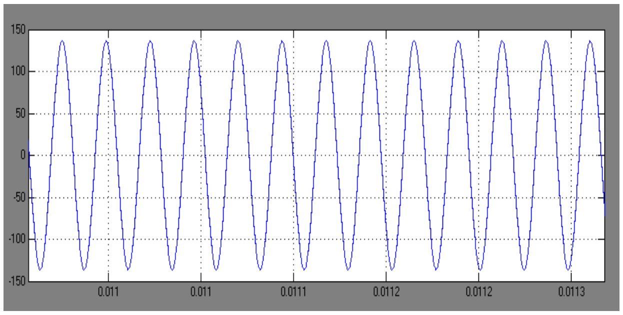

Fig. 4.f. Output Current

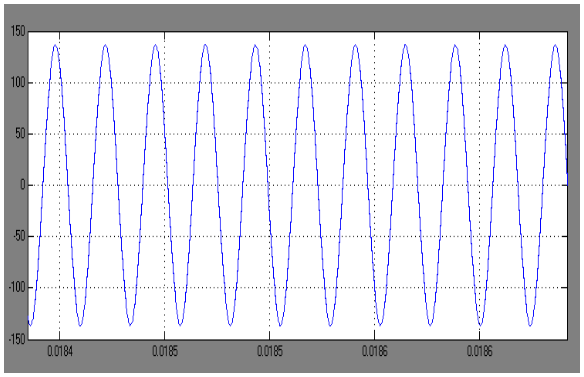

Fig.4.g Output Voltage

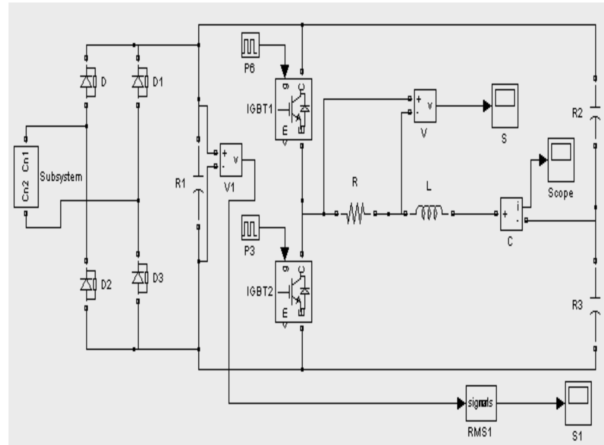

Fig.5.a Open loop system

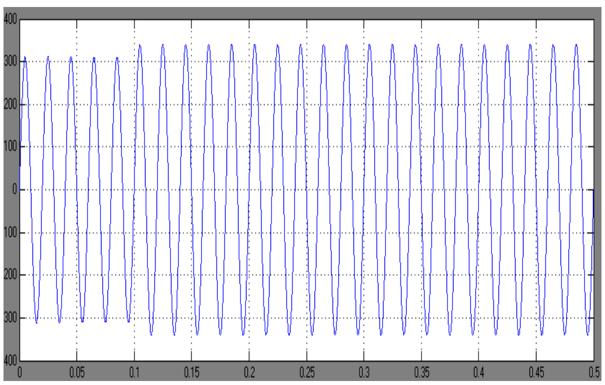

Fig.5.b. Input Voltage.

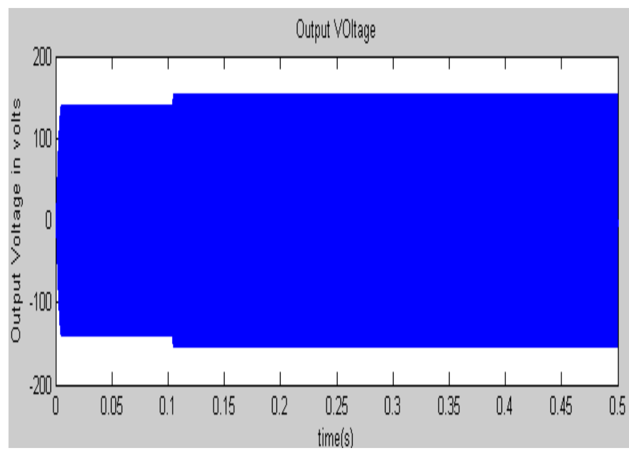

Fig.5.d. Output Voltage

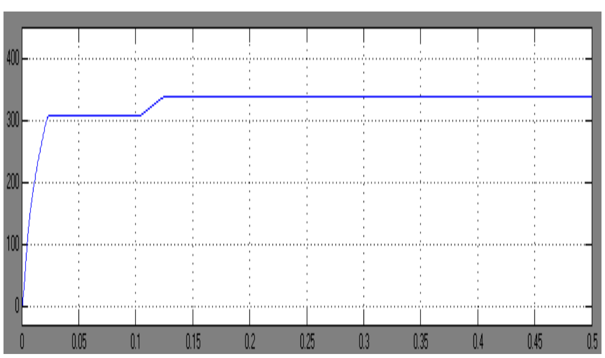

Fig.5.c. Rectifier output Voltage.

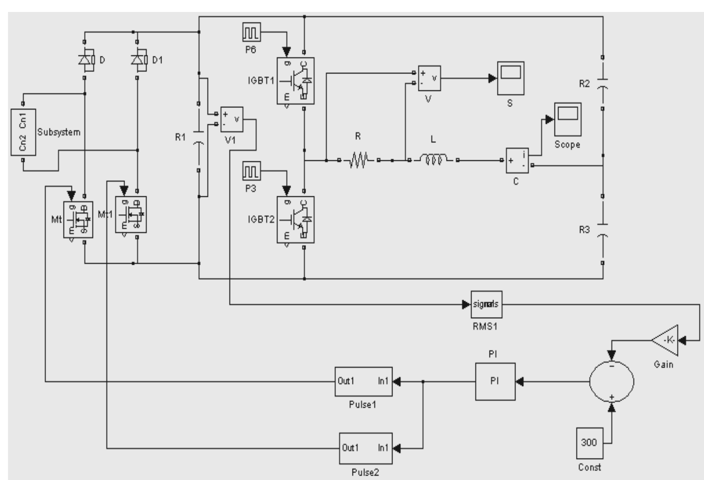

Fig.5.e. Closed loop Circuit diagram

Open loop system with a disturbance at the input is shown in Fig.5.a. A step change in input voltage is applied as shown in Fig.5.b. The output of the rectifier is shown in Fig.5.c. The output of the class D inverter is shown in Fig 5.d. It can be seen that there is an increase in the output when there is a disturbance at the input.

Closed loop circuit model is shown in fig 5.e. Dc voltage is sensed and it is compared with the reference value. The output of the PI controller adjusts the pulse width such that the output is brought back to constant value. Closed loop system uses a semi converter to maintain constant amplitude at the output. The output of the rectifier in the closed loop system is shown in Fig.5.f. The Ac voltage in the closed loop system is as shown in Fig.5.g. It can be seen that the closed loop system maintains constant voltage.

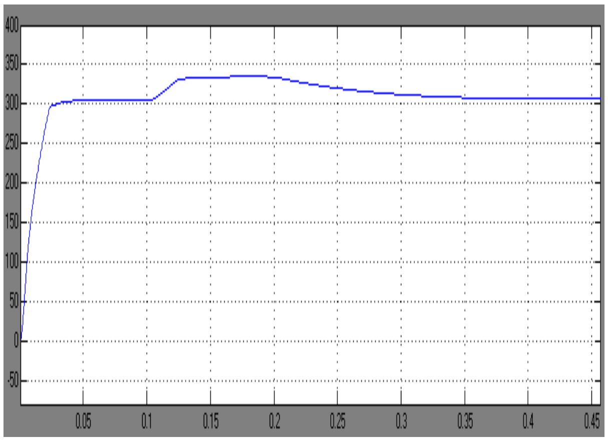

Fig.5.f. Rectifier output voltage.

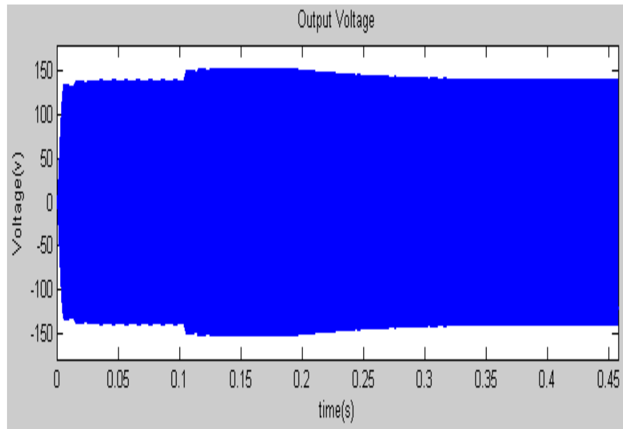

Fig.5.g. Output Voltage

IV CONCLUSION

A class D inverter fed induction heater is studied and simulated using Matlab Simulink. The simulation is done in open and closed loop using the models developed for open and closed loop systems. It is proposed to use a semi converter in the closed loop system to regulate the output voltage. The results of closed loop system indicate that it has reduced steady state error. The simulation results are in line with the predictions. This work deals with simulation studies. Hardware implementation is not in the scope of this work.

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