Journal of Theoretical and Applied Information Technology
15th May 2025. Vol.103. No.9

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

DESIGN AND ANALYSIS OF SPIN-BASED LOGIC GATES FOR ENHANCING COMPUTATIONAL EFFICIENCY

PRITI JAGATSING RAJPUT[1,2], SHEETAL U. BHANDARI[1], GUL FAROZ AHMAD MALIK[3]

[1]Department Of Electronics & Telecommunication Pimpri Chinchwad College Of Engineering, Pune, India.
[2]Department Of E&Tc Pimpri Chinchwad College Of Engineering & Research, Ravet, Pune, India.
[3]Department Of Electronics & Instrumentation Technology, University Of Kashmir, Srinagar, Jammu And Kashmir, 190006, India.

Email: [1]priti.Rajput21@Gmail.Com, [2]sheetal.Bhandari@Pccoepune.Org, [3]gfarozam@Gmail.Com

ABSTRACT

Spin transistors (Spin-FETs) are a promising way to solve problems with non-volatility, speed, and power consumption in standard CMOS technology. The Spin-FET electrical model using InAs channel material with 800 nm and 820 nm channel lengths is briefly explained in this paper. Spin-FET local geometry can be used to execute digital logic functions according to the experimental analysis. The local geometry of the spin transistor is designed using the Datta-Das concept and the spin injection and detection theory. It is implemented using the Verilog-A language on a Cadence platform. Transient and DC analysis for various channel lengths have been used to validate the results. The power consumption and capacitance of the complementary spin-FET and conventional CMOS have also been compared. This permits the inverter and buffer gate to function with a complimentary spin-transistor. In contrast to other research, our study presents XNOR and XOR gates that are built using a single gate SFET control input technique. However, our design improves computational efficiency by using a novel technique to regulate spin-based logic gates.

Keywords — *Spin-FET Modeling, Local Geometry, Beyond CMOS Technology, Single Gate Spin-FET, Logic Gates, Complementary Spin-FET.*

1. INTRODUCTION

The researchers pay more attention to finding alternatives for low power consumption in conventional CMOS. The International Technology Roadmap for Semiconductors [1], [2] emphasizes the quest for innovative technologies that can replace complementary metal-oxide-semiconductor (CMOS) technology with lower power consumption and variability. One of the most promising solutions to the power problem beyond current CMOS technology is spintronics, which harnesses the magnetic property of electrons for information processing[3], [4]. In the last 20 years, there has been much interest in research into spin-FET, a fundamental spin-based device described by Datta and Das [5], [6]. The fundamental idea behind a spin-FET is to regulate the spin current passing through a semiconductor channel by applying an additional electric field. Several groups had previously conducted experiments to realize this spin-FET[7], [8]. The potential of implementing such a device is also provided by several theoretical derivations [9], [10].

The objective of this research is to model and design a single-gate spin-based logic device that provides low energy consumption with limited delay and retains logic states without refresh cycles. The device works for low-power applications as well as nonvolatility. In this research, the electrical model has been developed for local geometry spin-FET to study the functionality of digital circuits using single gate spin-FET, which can be utilized for the digital design and modeling of logic circuits based on complementary spin-FETs using Computer Assisted Design (CAD) tool. Based on the Datta-Das theory[11] the theoretical derivations have been modeled using the Verilog-A language. Spin-FET channels were optimized with respect to the type of material used at the channel region. The DC analysis shows the variation in channel length and junction polarization, which gives optimal output voltage. However, the transient analysis proves the function works digitally for Ghz frequency. The local geometry model of spin-FET was used to perform a static simulation by creating a physical circuit. The parameters taken for the

simulation are based on calibrated models and verified by established literature [5], [10], [12], [13]. Numerous spin-based logic structures, including memory and the complete adder, have been proposed [8], [14], [15]. A spin-based inverter was constructed using the complementary spin-FET paradigm, utilizing the proposed local geometry electrical model [16].

Additionally, a logic circuit based on spin transistors can be designed for AND, NOR, and NAND logic functions using complementary spin-FET. The transient simulation confirmed that the logic function worked well. Based on the simulation results, the device's operation speed and power consumption are also discussed in the power analysis section.

It has been noted that when devices shrink in size, second-order effects become evident, and they enter the nano-regime. The channel length modulation, gate-induced drain-lowering, hot carrier effect, drain-induced barrier-lowering, velocity saturation, and other second-order phenomena come into play. These brief channel effects get so intense that they interfere with the devices' operating ability. Regarding technology, it is imperative that devices be further scaled in order to expand functionality, which will undoubtedly take a significant amount of work [17]. In light of this, the researchers have taken into account a number of potential technologies, materials, and geometries [18]. All the efforts were made in the proper order. The sole structural difference between a MOSFET and a spin-FET is that the latter has a drain terminal (Detector) and a source electrode (Injector), while the semiconducting channel is inserted between two FM metals [6], [19]. The polarization of the spin of the electron is used to process any information. The carriers at the source side are forced into the spin-polarized, semiconducting channel in a specific direction in a spin transistor. The electrons' spin polarization is assumed not to change as they move through the channel. When these electrons arrive at the drain terminal, the drain terminal will accept the electrons that have maintained their polarization of spin and reject any other carriers whose spin polarization has changed. Because of this, the spin-FET is typically ON while the gate terminal is not receiving any voltage [20], [21]. When a suitable voltage is applied at the gate (V_G), the Rashba effect creates a magnetic field in the channel that prevents electrons from being received at the drain when a potential difference is applied between the source (S) and the drain (D) due to the polarization of electrons is altered by the gate voltage. The application of gate voltage in this manner causes the spin-FET to switch OFF. Based on the Dresselhaus interaction and Rashba interaction (also known as the Datta-Das Transistor), several spin-based devices have been modeled and implemented [22].

The essential characteristic that sets the spin-FET apart is that it is a hybrid spin device that operates on both current and charge. This device is composed of three horizontal layers: a semiconducting layer that serves as the scattering zone, a ferromagnetic layer that acts as the source, and a second ferromagnetic layer that serves as the drain. An insulating material is placed across the channel, and a metal gate is positioned above the channel [6]. The spin transistor makes use of an electron's spin degree of freedom. An electron's spin can be oriented in one of two ways: either up or down [17]-[21]. Since charge only has magnitude, it is scalar in nature. When compared to the spin, a pseudo-vector has both direction and magnitude. Because of inherent bistable spin polarization, electrons in a magnetic field can incorporate the 0 and 1-bit representations, i.e., low and high levels. With an 800 nm channel length and InAs channel material, the paper emphasizes the static simulation of an electrical model of a single-gate spin-FET. InAs are particularly advantageous due to their high electron mobility and strong spin-orbit coupling, which are critical for the efficient operation of Spin-FETs. These properties enhance the performance of spintronic devices, making InAs an ideal choice for the proposed logic gate models. Both parallel (P-ST) and anti-parallel (AP-ST) spin transistors have been used to build the logic gates using the local geometry of the spin transistor. This approach provides unique insights into the design and functionality of logic gates that leverage the spin degree of freedom, offering potential advantages in low-power and high-speed applications.

The research work has been structured as follows: Electrical modeling of Single gate Spin Transistor is explained in Section I. The spin transistor's transient and DC analyses for various channel lengths and spin polarization are covered in Section II. Later on, a detailed description of complementary spin-transistors and their transient analysis has been discussed in section III. The spin-FET-based digital gates explained in Section IV and the transient time and power analysis have been summarized in Sections V and VI, Whereas Section VII deduces the conclusion.

2. DEVICE MODELING AND SIMULATION

The local geometry of the spin transistor model is shown in Fig. 1. The cadence platform was used to

Journal of Theoretical and Applied Information Technology
15th May 2025. Vol.103. No.9

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

construct the electrical model of the spin transistor using the Verilog A language. The Datta-Das [6] theory has been used to model this device. However, a complementary structure of local geometry has been implemented. Logistic gates were also designed using complementary spin-transistors.

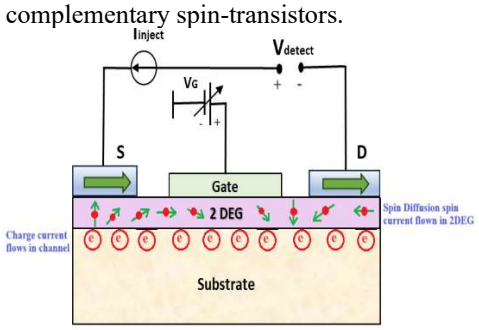


Figure 1: Structure of local geometry of Spin-FET

The P-ST and AP-ST depend on the magnetization direction of the source and drain. The detected voltage and injected current relationship have been given by further equation [10]

$$\frac{V_{detect}}{I_{inject}} = \pm 2R_N e^{\frac{L}{\lambda_N}} \prod_{i=1}^{2} \left[\frac{P_J\left(R_i/R_N\right)}{1-P_J^2} + \frac{P_F\left(R_F/R_N\right)}{1-P_F^2} \right] X \left[\left(\prod_{i=1}^{2} \left(1 + \frac{2\left(R_i/R_N\right)}{1-P_J^2} + \frac{2\left(R_F/R_N\right)}{1-P_F^2} \right) - e^{-2L/\lambda_N} \right) \right]^{-1} \quad (1)$$

Where '+' & '-' show the direction of magnetization, R_F= FM electrode Resistance, R_N= Resistance of Semiconductor Channel, R_1 & R_2 are the interface resistances between two junctions, P_J= Junction Polarisation current of interfaces, reflects the capacity of polarization at junctions, PF =Polarisation current of the FM electrode, In NFM, L stands for channel length and λ_N for spin-diffusion length, which is dependent on the channel material's property. Keep in mind that, under the following presumptions, equation (1) gives the Datta-Das theoretical model for detected voltage. (a) The FM1 & FM2 have a similar thickness & width b) The interfacial spin-flip scattering is disregarded for simplicity. (c) The FM and NFM material widths are significantly greater than their widths when taking into account the experimental geometry [13], [26]. Table I shows the default values.

Both contacts should be tunneling junctions to generate the maximal spin signal, R_1, R_2 >> R_N, as per the following analytical expression. This expression can be made simpler by stating:

$$\frac{V_{detect}}{I_{inject}} = \pm \frac{1}{2} P_J^2 R_N e^{-\frac{L}{\lambda_N}} \quad (2)$$

The structure for local and non-local geometry has been studied with the pure spin current and spin with charge current. Datta and Das proposed the heterostructure worked on the spin diffusion theory. The spin injection and detection are based on pure spin current, which is spin diffusion at the NFM layer from the FM layer to the NFM layer[16], [27]. The source terminal (FM1) acts as an injector, and the drain terminal (FM2) acts as a detector. However, due to the spin diffusion effect, the semiconducting 2DEG channel consists of pure spin-polarized current. The 2DEG forms a high spin-orbit interaction at the surface. The accumulation of spin-polarized electrons depends on the direction of magnetization at the source and drain side[27], [28]. This accumulation of electrons generates the voltage at the drain side due to the inequality of electrons at the channel and drain terminal. It is connected to the ground to reduce the influence of the circuit's charge current. Therefore, only spin injection and detection are considered [29], [30]. The magnetization direction of FM electrodes at the S & D side shows the parallel and anti-parallel spin-FET. The detected voltage and injected current relationship are expressed in equation 2 [10]. The spin precession angle, which is modulated by the gate voltage, VG, determines the output signal.

TABLE I
MODEL PARAMETERS FOR SPIN-FET

Parameter	Description	Default Values
m*	Effective mass of electrons	0.05X9.1X $10^{-31} kg$
$\hbar$	Reduced Planks constant	1.054 X $10^{-34} J.s$
P_J	Junction Polarization	50%
R_N	Channel Resistance	0.5kΩ
L	Channel Length	800 nm
λ_N	Spin-diffusion Length	1 µm
S_{type}	Type of spin-FET	1
φ	Phase shift correction	0
k_0	Fitting coefficient	0
k_1	Fitting coefficient	-3.4205 X 10^{-31}
k_2	Fitting coefficient	9.5775 X 10^{-31}

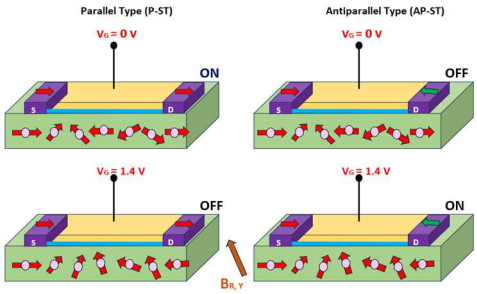
Nonlocal geometry allows for the absence of additional side effects, which makes it useful for spin physics observations. Local geometry should improve reading and cascade in an actual logic circuit. However, the local geometry and the traditional MOS transistor share the same current route. In [7], an all-spin logic device is presented using nonlocal geometry; the charge current is absent in such devices. However, cascading circuits in our transistor should require local geometry as nonlocal geometry gives significantly less output voltage, which is in the microvolt range; therefore, this

Journal of Theoretical and Applied Information Technology
15th May 2025. Vol.103. No.9

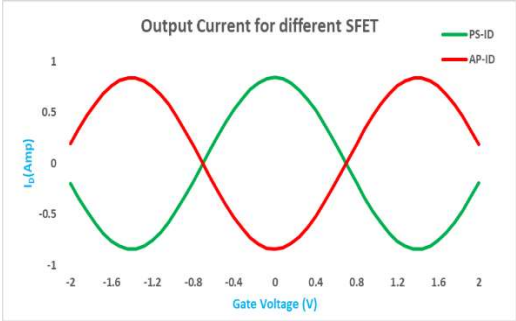
ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

geometry isn't sustainable for the cascading of the circuit. The first stage's nonlocal output voltage is insufficient to function as the second stage's input to produce enough output at the final stage. Additionally, the current path for a complex logic circuit is inaccessible if we use nonlocal geometry. By applying reasonable material parameters, the nonlocal signal is transformed into the local signal. A detailed description of the parameter values will follow.

At a given gate voltage, the spin precession angle in local and nonlocal signals should be the same for the InAs. In InAs, the output voltage gets a minimum and maximum value at $V_G = 0$ V & 1.4 V. For another heterojunction channel, the output voltages are obtained differently for the value of V_G [26]. Also, the vertical structure of InAs in the quantum well is 2 nm, whereas other heterojunctions have 6 nm to 20 nm, which confines the high mobility at the channel region[12]. In the channel region, we get maximum carrier density and mobility of electrons at 2-DEG for InAs. However, the spin relaxation time of electrons is also 1.61µm [12], [27]. The slight gate voltage shift is the only parameter that may be altered for the optimal curves. By modifying the carrier supply layer's doping concentration and the quantum-well structure, the gate voltage shift can be achieved in a practical device. The Spin-FET is typically an 'ON' transistor; therefore, it gives output voltage when the direction of magnetization of the electrodes is aligned in the same direction[16], [21]. Generally, P-ST is stated as ON transistors; we need to apply gate voltage to turn it OFF.



(a)



(b)

Figure 2: (a) Complementary spin-transistors operation mechanism. Where, $B_{R,y}$ is the Rashba effective field. (b) DC analysis of output current for different S-FET.

Fig. 2 shows the maximum output current and voltage at 0 V, and after applying a gate voltage, it shows a minimum current and voltage at 1.4 V for the channel length of 800 nm. Moreover, we can determine the ideal signals of the two transistors for the logic simulation using the adjusted experimental results. The P-ST exhibits ON (V_G = 0 V) and OFF (V_G = 1.4 V) states, while the AP-ST exhibits ON (V_G = 1.4 V) and OFF (V_G = 0 V) states.

The spin orientation of the electrons that arrive at the drain and the alignment of the detector's (drain's) magnetization vector define the channel conductance of a spin transistor. The spin orientation at the drain, which is determined by the spin precession angle, is the only variable that matters because the magnetization direction of the drain is fixed. The linear correlation exists between the spin precession angle (α) and the gate voltage (V_G) when the Rashba parameter is directly proportional to the gate voltage. Consequently, the P-ST's output current is maximum at minimum gate voltage, a function of the channel conductance[21].

However, it's more apparent that we get the maximum detected voltage for the local geometry of the spin-FET, which is suitable for the cascading connection for digital devices[31]. While non-local geometry causes more complexity for circuit design, and it fails to generate enough output voltage for any series connection, which is explained by Wang et al.[26]. The local geometry model is used under the same parameter settings. Fig. 1 shows the structure of local geometry. However, the experimental parameters are considered in this geometry by Ji Hoon Kim et al. [27]. Before entering the channel, the injected current is split into two parts: the charge current, coupled to the ground, and the spin-polarized current. Where injected current can be generated from any current source or source transistor. Which consists of charge current in addition to spin current.

3. COMPLEMENTARY SPIN-TRANSISTORS AND THEIR APPLICATION

For P-ST at Vg= 0 V, then Vout shows the maximum detected voltage, and the transistor operates in ON condition by delivering maximum current at the output, which is shown in Fig. 2 (a) & (b); vice versa for AP-ST, it works for Vg at 1.4 V while Vdc= 1V. It's confirmed that when electrons pass through a 2-dimensional electron gas in narrow-gap NFM material, the splitting of energy occurs without an external magnetic field. The electrons travel through the channel due to the internal magnetic moment of the electrons, which is influenced by the Rashba effect at the channel region. The inherent magnetic field and other factors cause energy splitting, which causes the spin-polarized electrons to undergo a phase shift. When compared to the Rashba effect, other processes' effects are less. Datta and Das deduce the phase shift's formulation as follows:

$$\Delta\boldsymbol{\theta} = \frac{2m^{*}\alpha L}{\hbar^{2}} \quad (3)$$

Where $\hbar$ = Reduced Planck's constant, $m*$ = electrons effective mass, and α = spin-orbit coupling coefficient. It is evident that the phase shift $\Delta\theta$ is directly correlated with the α, signifying the intensity of the Rashba effect. To regulate the $\Delta\theta$, an extra electric field provided at the channel can modulate the α. This technique accomplishes the modulation of gate voltage. For the spin-polarized current to be modulated efficiently throughout the channel, the phase shift needs to be at least half cycle, meaning that $\Delta\theta \geq \pi$.

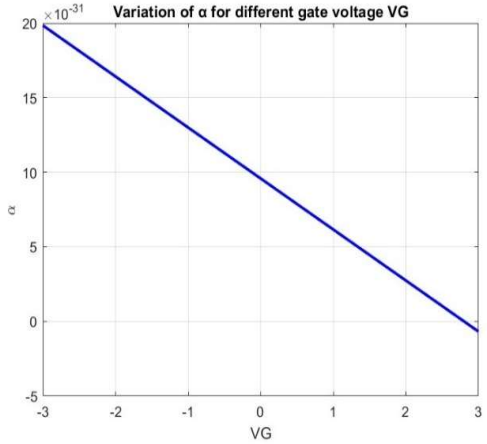


Figure 3: Relation Between Spin-Orbit Coupling And Gate Voltage

Fig. 3 shows the connection between α and VG is represented that the α is clearly dependent on the gate voltage, and it is approximately are [26], [28]:

$$\boldsymbol{\alpha = k_0 V_G^2 + k_1 V_G + k_2} \quad (4)$$

Where, the fitting correlation coefficients are represented by $k0$, $k1$, and $k2$. It is evident from Fig. 3 that the function of gate voltage (V_G) determines the spin-orbit coupling coefficient (α).

The behavior of the spin transistor can be expressed by the aforementioned equations after this model and the Datta-Das theory are combined[26]. The spin-FET's detected output voltage is found using equation (5):

$$\boldsymbol{V_{out} = S_{type}.I_{inject}.n_s.\cos\left(\frac{2m^{*}\alpha L}{\hbar^{2}} + \varphi\right)} \quad (5)$$

$$\boldsymbol{n_s = \frac{V_{detect}}{I_{inject}} = \pm\frac{1}{2}P_f^2 R_N e^{-\frac{L}{\lambda_N}}}$$

Using the CAD tool, the employing values are shown in Table I [26], [31].

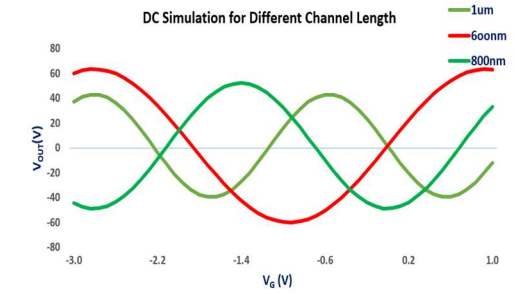
4. RESULTS AND DISCUSSION

4.1 Static Simulation of Spin-FET

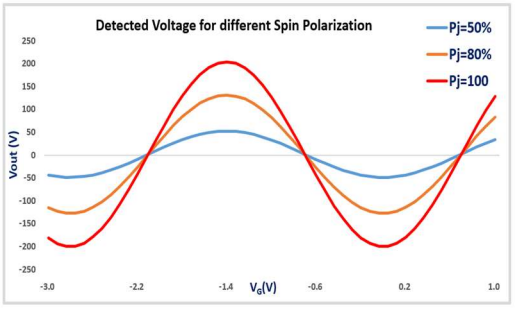
The theory of Datta-Das [6], [11] has been designed to perform static simulations for current and voltages done in this review. With the help of DC analysis, by selecting different channel lengths and channel resistance, we get maximum and minimum output voltage when V_G= 0 V and V_G=1.4v, respectively, for L=800 nm, which is suitable for performing logical circuit analysis. Fig. 4 (a) & (b) shows the output voltage for different channel lengths and spin junction polarization[32]. It is pertinent to mention that many functions have been implemented using a single device. For this, some changes were made in device parameters like channel length, junction polarization, injected current, etc. To obtain the different logic functions. Therefore, we get maximum or minimum output voltage according to variation in channel lengths as per circuit requirement. Several research groups have also verified that the electrical reconfigurable logic design without varying any parameter can be utilized for the implementation of two or three input logic functions [24], [33].

For an electrical application, the channel length must be optimally designed so that the detected voltage is either higher or lower in the absence of gate voltage, allowing the spin precession angle to be either odd or even multiples of gate voltage [34]. The detected voltage is also considerably influenced by channel resistance (R_N) and the length of the channel. The different channel length shows the different detected voltages; however, we require maximum output voltage for digital circuits to work. Therefore, the local geometry shows the maximum detected voltage as compared to the non-local geometry discussed by Wang G. et al. [26]. The

cascading operation of a digital circuit requires local geometry. To perform various logical functions with the optimum detected voltage to adjust the channel's lengths and resistance.



(a)



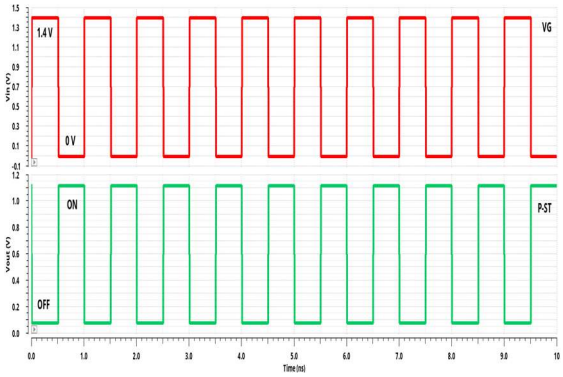
(b)

Figure 4: DC Simulation For Local Geometry Of Spin-FET (A) For Different Channel Lengths And (B) Different Spin Polarization.

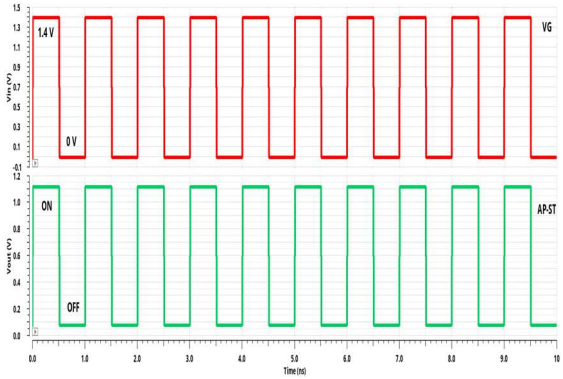
For maximum spin-orbit interaction, the 2DEG material is used in the channel. Fig. 4(b) shows the simulation result for various junction polarization (P_J). It is evident that a greater output detected voltage is a direct result of a higher spin polarization rate. In the case of local geometry, it's been observed that the 100% spin polarization rate gives sufficient output voltage to operate a cascading circuit operation using spin-FET. Additionally, the designed electrical model has performed well in functioning digital logic circuits.

4.2 Analysis of Complementary Spin-FET

With the help of Verilog-A language through cadence platform parallel and anti-parallel spin-FET transient simulation has been shown in Fig.5 (a) & (b), and their maximum detected voltage for both transistors has been calculated by using equation (5). We get maximum current at zero gate voltage (0 V) for parallel spin transistors. In contrast, for anti-parallel, we get minimum current and minimum voltage at 0 V. For 1.4 V for parallel spin transistors shows the minimum (OFF) output voltage and maximum (ON) output voltage at 0 V whereas, for anti-parallel spin transistor, it's vice-versa for 800nm channel length. We get the maximum output voltage for 100% spin polarization at the junction. However, the non-local geometry gets significantly less voltage to drive cascade spin transistors even if the 100% spin polarization[26]. This device is designed with Parallel and anti-parallel circuits to perform operations like PMOS and NMOS in CMOS circuits. Fig 5 (a) & (b) shows the transient simulation of spin-FET. The transient analysis of P-ST & AP-ST, respectively, for different magnetization directions at the drain side.



(a)



(b)

Figure 5: Transient Analysis (A) For Parallel (P-ST) Spin Transistor (B) For Anti-Parallel Spin-FET (AP-ST)

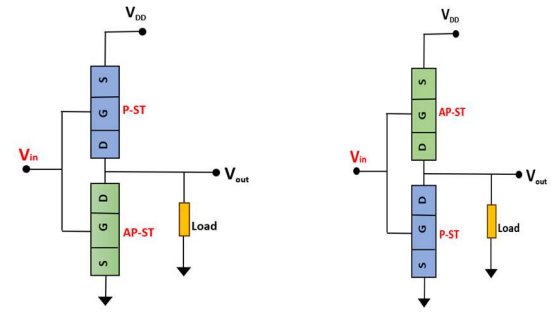
The expected results are calculated by applying the fixed load at the circuit. The complementary design using the spin-FETs is carried out by developing two complementary SFETs, one turning ON and the other turning OFF with a change in Gate voltage, which exactly works like the conventional CMOS design. The P-Spin transistor is ON when the gate voltage is 0 V, where OFF is 1.4 V. However, for an anti-parallel transistor, it works opposite, which is shown in Fig. 5 (a)&(b)

Journal of Theoretical and Applied Information Technology
15th May 2025. Vol.103. No.9

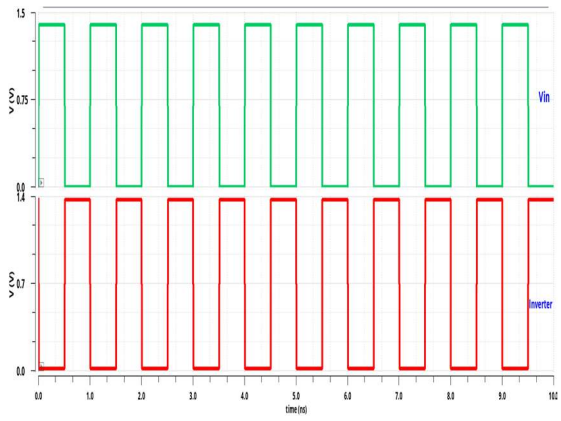
ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

4.3 Spin-FET Based Buffer & Inverter

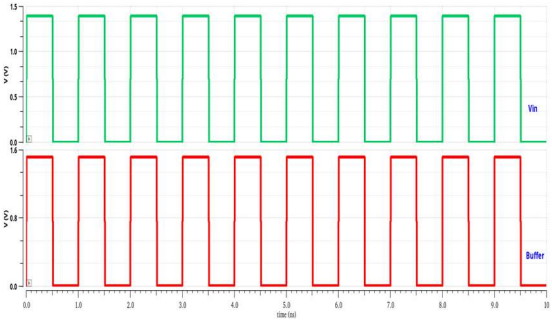
In the structure of spin-FET, both currents flow in the channel. The pure spin-polarized current passing through the 2-DEG varies by changing V_G; another is the charge current through the channel independent of V_G. An inverter and buffer gate employing complementary spin-FET is developed in Fig. 6 (a) & (b) [23] to confirm the functionality of the electrical model, and the associated simulation result is displayed in Fig. 6 (c) & (d). The outcomes prove that a local geometry model mimics the buffer and inverter functions and works well in the desired channel length with a frequency of 1 GHz. Using the transient simulation validates the spin-based electrical model's functionality, making it feasible to design and analyze the spin-FET-based circuits with the help of a complementary spin transistor



(a) (b)



(c)



(d)

Figure 6: Symbolic Representation Of (A) Inverter (B) Buffer Gate, And Simulation Results At 1Ghz Frequency For (C) Inverter And (D) Buffer Gate.

4.4 Spin-FET-Based Logic Circuits

H.C. Koo et al. [16]have reported their results for AND logic and NAND logic gates by using complementary spin-FET. Also, Wang G. et al. [26] have reported their work by using spin-transistor and design structures for NOR and AND logic using a CMOS transmission gate and spin-based inverter for 1200nm channel length. Using Verilog A with a cadence platform, the structure for local geometry spin-FET is designed, and the static simulation is performed. The transient simulation is obtained by applying the 1.4 V pulse with a 10ns trans period at the input, and the DC simulation is obtained by performing parametric analysis.

We designed XOR & XNOR gates which hasn't be explored in earlier research. The output signals for XOR & XNOR are performed for a channel length of 820 nm with injected current at 3.2 μA for control input X=0 V and X= 1 V. The structure for XOR and XNOR has been designed using Anit parallel spin-FET. Fig 7 (a) shows the design structure for XOR and XNOR gates. Where, Fig 7 (b) & (c) show the transient simulation for XOR and XNOR logic gates. To smoothen the output waveform, we require a CMOS-based circuit [31], [33]. The reduction in charge current causes the current to flow through the channel to be pure spin current, and due to that, it is performed under nonlocal geometry, which derives very low output voltages. [7], [16], [26], [35]. The output voltage offered at the V_{OUT} stage is very low. The lower drive capability of spin-FETs involves the clamping and/or amplification of signals before their application to the subsequent stage[31]. The truth table for logic gates is shown in Table II. V_A and V_B are inputs of gates; however, V_{out} are outputs for XOR, and XNOR *Gates.*

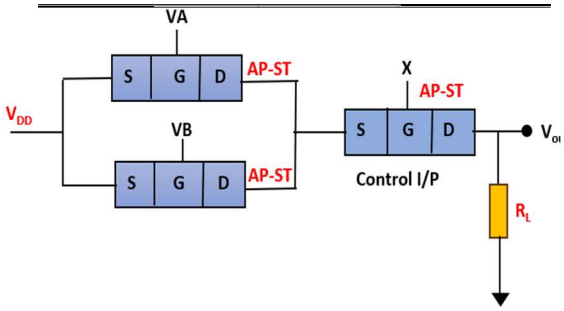
TABLE II

Journal of Theoretical and Applied Information Technology
15th May 2025. Vol.103. No.9

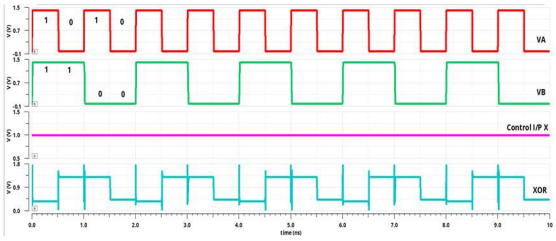
ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

XOR AND XNOR TRUTH TABLE

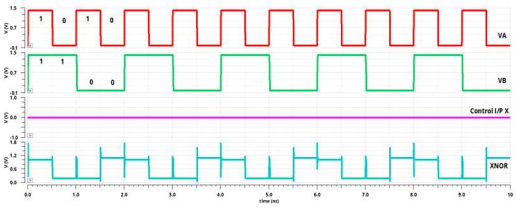
Inputs		*Outputs*	
VA	*VB*	*(VA⊕VB) X = 1*	*(VA⊕VB)' X = 0*
1	1	0	1
0	1	1	0
1	0	1	0
0	0	0	1



(a)



(b)



(c)

Figure 7: Symbolic Representation Of (A) Logic Gates (B) Transient Simulation For XOR Gate (C) Transient Simulation Of XNOR Gate.

This design has a relatively low ON/OFF ratio, considering the logical operation. The single gate spin-FET doesn't give a smooth output structure. Therefore, we need to go for multi-gate logic to perform digital operations. The low spin injection efficiency between the semiconductor channel and the ferromagnetic electrode is the primary cause. In the field of spintronics, interface engineering—such as oxide insertion—is presently receiving a lot of interest for increased spin injection. Lowering the stand-by current is another way to improve the ON/OFF ratio. We used an InAs-based quantum-well layer, which can be used to demonstrate gate-controlled spin precession; because of the high carrier density, the OFF-current is not zero. A novel quantum-well system with low carrier density and high mobility material needs to be considered. Combining spin with charge is another technique.

5. TRANSIENT TIME ANALYSIS

The transient simulation validates the functionality of the local geometry model, which proves its functionality and analyses its performance for circuit applications using this model. The inverter and buffer gate have been designed by using complementary SFET. The S and D act as injection and detection of electrons, respectively. A parallel spin transistor's drain terminal is connected to the anti-parallel spin transistor's drain with applied load R_L, which converts output voltage from output current. Fig. 6 (a) shows the structure of the inverter and buffer using complementary Spin-FET. Both the transistors' gate terminals are connected to the input pulse, with the source terminal of AP-ST grounded and P-ST connected to the DC supply. The simulated results for the inverter and buffer can work for **1** GHz frequency with a transit time of 4 ps.

The transient time calculation was done using the formula [36], considering the values shown in Table 1.

$$t = \frac{L^2}{2D} + \frac{L}{V_f} \qquad (6)$$

The delay required for carriers to cross the channel is given in equation (6). Where the default values are shown in Table 3, considering these values based on the verified ex periments done by H C Koo et al. [16], [28]. The first part of the equation shows the spin diffusive time, and the second term shows the equation's ballistic time (6).

TABLE III
DEFAULT PARAMETERS FOR TIME ANALYSIS

Parameter	Description	Default Values
D	Electron diffusion coefficient for InAs	$\leq 10^3$ cm^2.S^{-1}
L	Channel Length	800 nm
V_f	Fermi Velocity of Electrons	≈ C/300
C	Speed of Light	3 X $10^8 m/s$
W	Width of channel	40 nm

However, the obtained delay is about four picoseconds for complementary SFET; therefore, it works for the THz frequency. For high-performance digital circuits, the high-speed communication system requires a frequency range of several GHz to

fulfill the requirements of digital circuits. The quantitative simulation majorly depends on the length of the channel and the channel material used in the transistor. The delay time was calculated for InAs channel material.

6. POWER ANALYSIS OF SPIN-FET

The dynamic power consumption of the logic gates is estimated as $P = CfV_{DD}^2$. The total output power consumption for the inverter can be calculated with the total output capacitance offered by the inverter as $C = 2C_{DRAIN} + C_{LOAD}$ is the sum of the drain and load capacitances [16]. Therefore, the total power consumption for the inverter can be estimated by using equation (7)

$$P = (2C_{drain} + C_{load})fV_{DD}^2 \qquad (7)$$

Where, C_{DRAIN} = Drain capacitance, C_{LOAD} = output capacitance occurred by circuit, f = frequency, and V_{DD} = DC Voltage. For the conventional CMOS-based inverter, the $C_{DRAIN} \sim 1.15fF$, $C_{LOAD} \sim 6fF$, and $C_{GATE} \sim 1fF$ with 1 GHz signal frequency and 1V DC supply. Meanwhile, the spin-FET drain and source are made up of ferromagnetic material; therefore, no capacitance is produced. In the case of a spin-based inverter, the drain capacitance is neglected because the FM electrode is used instead of a doped semiconductor. Thus, it is shown that a significant amount of power will be saved compared to conventional CMOS design and spin-FET-based logic devices. The transient time of the proposed gate is also less than that of the traditional CMOS. Nearly about 30 % of power will be saved using a spin-based inverter by considering other identical conditions of the CMOS inverter. For XOR and XNOR logic circuits, the total capacitances offered by the CMOS circuit are expressed as

$$C_{XOR} = (8C_{GATE} + 8C_{DRAIN} + C_{LOAD})$$

$$C_{XNOR} = (8C_{GATE} + 8C_{DRAIN} + C_{LOAD})$$

Where, the Gate capacitance, drain capacitance, and load capacitance are assumed to be 1fF, 1.15fF, and 6fF. The power consumed by the CMOS XNOR Gate and XOR gates is more than that of spin-based logic gates [33]. Therefore, the total power consumption for a spin-FET-based NOR gate is 31.5 % less because the capacitance offered by Spin-FET are

$$C_{XOR} = (8C_{GATE} + C_{LOAD})$$

$$C_{XNOR} = (8C_{GATE} + C_{LOAD})$$

Therefore, for XNOR and XOR gates, dynamic power reduction in spin-based transistors is ≈ 31.5%. However, we required a doping process for CMOS technology to form n-channel and p-channel. The lithography process is necessary to create the source and drain. The doping process needs accurate implantation of ions for the source and drain area, which is a more complex process and limits device scaling. In spin-based transistors, FM materials are used for the formation of source and drain, and device scaling is more feasible than traditional CMOS. However, there are experimental challenges associated with realizing such devices, including the need for precise control of spin injection and detection, channel material, spin relaxation, and spin lifetime, which remains an area of active research.

7. CONCLUSION

Datta-Das theory has been used to simulate the static simulation of a single gate parallel and anti-parallel spin-FET-based electrical model using the Verilog A language. Complementary Spin-FET DC analysis has also been investigated utilizing the spin-injected current and detected voltage equation in Datta-Das theory. However, complementary spin transistors have also been used in circuit simulation. After DC and transient analyses of the logic circuits, the device is functional at 1 GHz operating frequencies to perform the digital operation. We have clarified how our study advances the field by integrating complementary Spin-FETs into logic gates, which has not been extensively explored in prior research. Although our work is based on numerical simulations, it provides new insights into the potential application of Spin-FETs in digital logic circuits, offering a pathway for future experimental validation and development. By taking into consideration complementary spin-FET and simulating logic circuits, the device performs well for logic gate conditions. It confirms that the local geometry can be used for designing digital logic circuits. An analysis using validated theoretical and experimental data has been carried out for varying channel lengths and injected currents. We created the XNOR and XOR logic using AP-ST for different channel lengths using transient simulation of the device. Compared to typical CMOS technology, the recommended logic gate circuits are used to reduce power consumption by about 30%. The implementation of logic gate simulations with experimentally collected parameters shows the potential of the spin-based logic device. Additionally, spin-based circuits can be used to show a device's digital architecture by utilizing complementary spin-based transistor structures that alter the channel's length and material properties.

REFERENCES

[1] Linda. Wilson, "'International Technology Roadmap for Semiconductors (ITRS).,'" *Semiconductor Industry Association*, 2013.

[2] B. Hoefflinger, "ITRS 2028-international roadmap of semiconductors," in *CHIPS 2020 VOL. 2: New Vistas in Nanoelectronics*, Springer International Publishing, 2015, pp. 143–148. doi: 10.1007/978-3-319-22093-2_7.

[3] W. Z. X. Zhang, Y. Zhou, M. Ezawa, G. P. Zhao, "'Magnetic skyrmion transistor: skyrmion motion in a voltage-gated nanotrack,' Sci. Rep., vol. 5, p. 11369, Jun. 2015.," vol. 5, p. 11369, 2015.

[4] V. K. Joshi, "Spintronics: A contemporary review of emerging electronics devices," *Engineering Science and Technology, an International Journal*, vol. 19, no. 3, pp. 1503–1513, 2016, doi: 10.1016/j.jestch.2016.05.002.

[5] P. Chuang *et al.*, "All-electric all-semiconductor spin field-effect transistors," *Nat Nanotechnol*, vol. 10, no. 1, pp. 35–39, Jan. 2015, doi: 10.1038/NNANO.2014.296.

[6] S. Datta and B. Das, "Electronic analog of the electro-optic modulator," *Appl Phys Lett*, vol. 56, no. 7, pp. 665–667, 1990, doi: 10.1063/1.102730.

[7] E. Villamor *et al.*, "Modulation of pure spin currents with a ferromagnetic insulator," Apr. 2015, Accessed: Jul. 29, 2021. [Online]. Available: http://arxiv.org/abs/1404.2311

[8] G. Yu *et al.*, "Room-temperature skyrmion shift device for memory application," *Nano Lett*, vol. 17, no. 1, pp. 261–268, Jan. 2017, doi: 10.1021/ACS.NANOLETT.6B04010.

[9] T. Nie *et al.*, "Enhancing electric-field control of ferromagnetism through nanoscale engineering of high-Tc MnxGe1-x nanomesh," *Nat Commun*, vol. 7, Oct. 2016, doi: 10.1038/NCOMMS12866.

[10] S. Takahashi and S. Maekawa, "Spin injection and detection in magnetic nanostructures," *Phys Rev B Condens Matter Mater Phys*, vol. 67, no. 5, Feb. 2003, doi: 10.1103/PHYSREVB.67.052409.

[11] B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, "Proposal for an all-spin logic device with built-in memory," *Nat Nanotechnol*, vol. 5, no. 4, pp. 266–270, 2010, doi: 10.1038/NNANO.2010.31.

[12] W. Y. Choi, H. J. Kim, J. Chang, S. H. Han, and H. C. Koo, "Ballistic Spin Hall Transistor Using a Heterostructure Channel and Its Application to Logic Devices," *J Electron Mater*, vol. 46, no. 7, pp. 3894–3898, Jul. 2017, doi: 10.1007/S11664-016-4909-3/METRICS.

[13] S. Takahashi *et al.*, "Theory of electrical spin injection: Tunnel contacts as a solution of the conductivity mismatch problem," 1990.

[14] Z. Wang *et al.*, "Nonvolatile boolean logic block based on ferroelectric tunnel memristor," *IEEE Trans Magn*, vol. 50, no. 11, Nov. 2014, doi: 10.1109/TMAG.2014.2329774.

[15] H. Dery, P. Dalal, Cywiński, and L. J. Sham, "Spin-based logic in semiconductors for reconfigurable large-scale circuits," *Nature 2007 447:7144*, vol. 447, no. 7144, pp. 573–576, May 2007, doi: 10.1038/nature05833.

[16] H. C. Koo, I. Jung, and C. Kim, "Spin-Based Complementary Logic Device Using Datta-Das Transistors," *IEEE Trans Electron Devices*, vol. 62, no. 9, pp. 3056–3060, Sep. 2015, doi: 10.1109/TED.2015.2451618.

[17] E. Yurchuk *et al.*, "Impact of scaling on the performance of HfO2-based ferroelectric field effect transistors," *IEEE Trans Electron Devices*, vol. 61, no. 11, pp. 3699–3706, Nov. 2014, doi: 10.1109/TED.2014.2354833.

[18] M. A. Kharadi, G. F. A. Malik, K. A. Shah, and F. A. Khanday, "Sub-10-nm Silicene Nanoribbon Field Effect Transistor," *IEEE Trans Electron Devices*, vol. 66, no. 11, pp. 4976–4981, Nov. 2019, doi: 10.1109/TED.2019.2942396.

[19] S. Datta, "How we proposed the spin transistor," Nov. 01, 2018, *Nature Publishing Group*. doi: 10.1038/s41928-018-0163-4.

[20] P. J. Rajput, S. U. Bhandari, and G. Wadhwa, "A Review on—Spintronics an Emerging Technology," *Silicon*, vol. 14, no. 15, pp. 9195–9210, Oct. 2022, doi: 10.1007/S12633-021-01643-X/METRICS.

[21] G. F. A. Malik, M. A. Kharadi, F. A. Khanday, and N. Parveen, "Spin field effect transistors and their applications: A survey," *Microelectronics J*, vol. 106, Dec. 2020, doi: 10.1016/j.mejo.2020.104924.

[22] S. Pramanik, S. Bandyopadhyay, and M. Cahay, "Spin transport in nanowires," *Proceedings of the IEEE Conference on*

Nanotechnology, vol. 1, pp. 87–90, 2003, doi: 10.1109/NANO.2003.1231721.

[23] K. : Lee, D., Fong, X., Roy, "'R-MRAM: A ROM-embedded STT MRAM cache,'" *IEEE Electron. Device L., 2013,* vol. 34, no. 10, pp. 1256–1258, 2013.

[24] M. A. K. F. A. K. Gul Faroz Ahmad Malik, "Electrically reconfigurable logic design using multi-gate spin field effect transistor," *Microelectronics J*, pp. 278–284, Jul. 2019, Accessed: Jan. 11, 2024. [Online]. Available: www.elsevier.com/locate/mejo

[25] Malik G., Mubashir A hmad, and et.al, "Simulation of Triple Gate Spin Field-Effect Transistor and its Applications to Digital Logic," in *2020 IEEE VLSI Device, Circuit and System Conference (VLSI-DCS), 18-19 July, 2020, ED MSIT SBC, Kolkata, India*, Department of Electronics and I.T.Unniversty of Kashmir and IEEE Electron Devices Society. MSIT Student Branch Chapter, Eds., Kashmir (J&K) India: IEEE Electron Devices Society. MSIT Student Branch Chapter, Jul. 2020, pp. 440–443.

[26] G. Wang, Z. Wang, … J. K.-I. T. on, and undefined 2017, "Modeling for spin-FET and design of spin-FET-based logic gates," *ieeexplore.ieee.org*, Accessed: Jul. 18, 2021. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/7929380/

[27] J. H. Kim, J. Bae, B. C. Min, H. J. Kim, J. Chang, and H. C. Koo, "All-electric spin transistor using perpendicular spins," *J Magn Magn Mater*, vol. 403, pp. 77–80, Apr. 2016, doi: 10.1016/J.JMMM.2015.11.056.

[28] H. C. Koo, J. H. Kwon, J. Eom, J. Chang, S. H. Han, and M. Johnson, "Control of spin precession in a spin-injected field effect transistor," *Science*, vol. 325, no. 5947, pp. 1515–1518, 2009, doi: 10.1126/SCIENCE.1173667.

[29] T. Sasaki *et al.*, "Spin Transport in Nondegenerate Si with a Spin MOSFET Structure at Room Temperature," *Phys Rev Appl*, vol. 2, no. 3, p. 034005, Sep. 2014, doi: 10.1103/PHYSREVAPPLIED.2.034005/FIGURES/5/MEDIUM.

[30] L. Te Chang *et al.*, "Electrical detection of spin transport in Si two-dimensional electron gas systems," *Nanotechnology*, vol. 27, no. 36, p. 365701, Aug. 2016, doi: 10.1088/0957-4484/27/36/365701.

[31] G. Malik, M. Kharadi, N. Parveen, F. K.-I. Circuits, & D., and undefined 2020, "Modelling for triple gate spin-FET and design of triple gate spin-FET-based binary adder," *IET*, vol. 14, no. 4, pp. 464–470, Jul. 2020, doi: 10.1049/iet-cds.2019.0329.

[32] S. K. Shelke, P. J. Rajput, and S. Bari, "Implementation & comparison of different oscillators for ISM and WI-FI band applications," *Proceedings of 2017 11th International Conference on Intelligent Systems and Control, ISCO 2017*, pp. 332–335, Feb. 2017, doi: 10.1109/ISCO.2017.7856011.

[33] G. Wang, Z. Wang, X. Lin, J. O. Klein, and W. Zhao, "Proposal for multi-gate spin field-effect transistor," *IEEE Trans Magn*, vol. 54, no. 11, Nov. 2018, doi: 10.1109/TMAG.2018.2831696.

[34] S. K. Shelke, V. N. Nitnaware, and S. Rode, "Design of ring oscillator with better temperature, supply voltage & process stability with 32nm FDSOI transistor for ISM band application," *Proceedings of 2017 11th International Conference on Intelligent Systems and Control, ISCO 2017*, pp. 311–313, Feb. 2017, doi: 10.1109/ISCO.2017.7856005.

[35] J. Kim *et al.*, "Spin-based computing: Device concepts, current status, and a case study on a high-performance microprocessor," *Proceedings of the IEEE*, vol. 103, no. 1, pp. 106–130, Jan. 2015, doi: 10.1109/JPROC.2014.2361767.

[36] S. Rakheja and A. Naeemi, "Interconnect analysis in spin-torque devices: Performance modeling, sptimal repeater insertion, and circuit-size limits," pp. 283–290, Apr. 2012, doi: 10.1109/ISQED.2012.6187507.