

EVALUATING THE ROLE OF BODY BIASING IN ENHANCING DOMINO LOGIC CIRCUITS FOR ADVANCED VLSI TECHNOLOGIES

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ABSTRACT

Traditional complementary metal-oxide semiconductor (CMOS) technologies face scaling limitations, which have driven the search for innovative circuit-level optimisation methods to meet the rising demand for energy-efficient and high-performance microprocessors. Body biasing in domino logic is one such technique that holds promise for adjusting threshold voltage (V_{th}) and enhancing delay versus power modes under variable operating conditions. High-speed microprocessor datapath components utilise domino logic circuits, and this research examines how forward and reverse body biasing approaches influence them. The main aim is to investigate how body biasing optimises performance metrics such as energy efficiency, leakage power, dynamic power, and delay, while maintaining circuit reliability and noise immunity. Various body-biased domino logic configurations were modelled and compared under different supply voltages (VDD), operating frequencies, and process variations, using both HSPICE simulations and MATLAB/Python-based data visualisation. The experimental setup included logic units like adders, multipliers, and decoders. The comparison shows that RBB effectively reduces leakage but slows performance, whereas FBB significantly decreases delay at the cost of increased leakage power. A balanced trade-off between delay and power consumption exists within a tunable voltage window, which is scalable. Dynamic power consumption drops sharply at lower VDD levels; however, latency increases, which FBB can mitigate. This dual modulation enables adaptive energy control, making it suitable for modern microprocessors where workload scaling is crucial. The results demonstrate that domino logic design can effectively balance performance and efficiency in future technology nodes with the integration of body bias control schemes, making it suitable for low-power and high-speed VLSI applications.

Keywords: *Domino Logic Circuits, Microprocessor, Body Biasing, Dynamic Power Consumption, VLSI Application*

1. INTRODUCTION

Optimal trade-offs between space, power and speed are becoming more difficult to achieve in high-performance digital circuit design as semiconductor technology scales beyond the sub-10nm node. Microprocessor logic circuit implementation is a critical area where these

restrictions converge. Compared to conventional static CMOS logic (**Complementary Metal-Oxide-Semiconductor, known for robustness and low static power**) [1], [2], [3] Domino logic - **a dynamic logic family using precharge and evaluation phases** has drawn a lot of interest since it can operate at high speeds and uses fewer transistors. This makes it especially desirable for Datapath devices that need

high throughput, like multiplexers, decoders and arithmetic logic units (ALUs) [4], [5].

Nonetheless, these benefits of domino logic introduce critical design trade-offs. Comparison TWO: Domino logic's dynamic nature makes it susceptible to charge sharing. (**unintentional redistribution of charge in internal nodes**), leakage currents (**unwanted static power dissipation**) and noise disturbances. Moreover, the sensitivity of domino circuits to delays and power consumption [6], [7], [8] Rises as the supply voltages reduce, and their impact on the overall timing and the energy costs of microprocessors is huge. These problems are further enhanced in ultra-deep submicron and FinFET technologies, in which transistor variability also affects the circuit reliability.

To overcome these challenges, researchers have explored advanced techniques, such as body biasing, **a method for dynamically modulating the threshold voltage of MOSFETs**. (V_{th}) of MOSFETs may be dynamically modulated using forward and reverse body biasing, providing a potential solution to regulate delay, leakage, and energy efficiency issues [9], [10], [11]. Body biasing is a new direction for very large-scale integration (VLSI) systems because it gives designers greater flexibility to balance power and performance when combined with domino logic.

Even though domino logic has the potential for high-speed applications [12], [13], [14], [15], excessive scaling reduces its performance and dependability because of higher leakage currents and noise sensitivity. Timing restrictions and static power usage are still issues with traditional designs. Consequently, this study's primary research topic is:

How can body biasing techniques be effectively applied to domino logic to enhance the speed and energy efficiency of data path units in modern high-speed microprocessors?

In both academic and business settings, this study is important. This could be a big step forward in the design of energy-efficient as well as high-throughput data path units in microprocessors, especially in mobile devices, as well as low-voltage embedded systems [16], [17], [18]. Body biasing could help improve the performance of domino logic. More robust and scalable digital designs are made possible using body biasing, which also gives circuit designers adaptive control over transistor properties without compromising logic functioning [21].

This work aims at creating and analysing the domino-based data path logic that is designed

with and without using body biasing techniques. This research will attempt to:

- Using both conventional and body-biased domino logic, create simulation models for important logic components such as adders, multipliers, and decoders.

- Analyse the performance improvements in terms of delay, power and area.

- Check out Static CMOS and Pseudo NMOS (**a logic style with permanently ON PMOS loads**), two alternative CMOS logic families, and see how they stack up against the suggested method.

- Provide suggestions for using body biasing in microprocessor designs that consider energy efficiency.

2. LITERATURE REVIEW

2.1. Overview of Relevant Literature

High-speed digital development has been studied extensively using dynamic logic styles and especially domino logic since they use fewer transistors and have low output capacitance. Research prefers dynamic logic to static CMOS because of its temporal benefits, which are used in sophisticated microarchitectures. The significant limitations are domino logic's power inefficiency and sensitivity to noise [22].

With the introduction of adaptive body bias (ABB) methods in FinFET & SOI technologies, body biasing, which was initially used in bulk CMOS processes, has gained popularity. While reverse body biasing (RBB) effectively reduces leakage in standby modes, forward body biasing (FBB) has the potential to greatly increase switching speed, according to research.

2.2. Key Theories or Concepts

Body biasing at the transistor performance level is based on several theoretical models:

- Modulation of the Threshold Voltage: A MOSFET's V_{th} [23] may be adjusted in real time by manipulating the body bias, which impacts the drive current & leakage.

- Power-Delay Trade-off: FBB cuts down on power loss but brings about more delay, while RBB cuts down on leaking but causes more delay [24].

- Charge Sharing and Keeper Design: Techniques to suppress charge sharing in domino logic are often evaluated alongside body biasing to ensure functional correctness [25].

These theories also enable the optimisation of domino logic circuits with body-bias control in multiple performance states.

2.3. Gaps or Controversies in Literature

Although body biasing has theoretical potential, its actual use in domino logic [20] is still lacking, especially in data path modules like ALUs, multipliers & control units. With few attempts to combine both for a reliable low-power architecture [19], most of the literature either discusses body biasing or domino logic separately. Moreover, there are few real-time modelling and testing tools available for these coupled approaches across different CMOS logic families.

A consensus on the optimal body biasing strategy against logic versus memory components, the use of adaptive body biasing without destroying logic integrity, is also lacking. This study will help address this gap by showing the complete end-to-end design and comparative study of body-biased Domino logic implementations.

3. METHODOLOGY

3.1 Overview of Body Biasing in Domino Logic

The process of body biasing involves changing the voltage supplied to the body terminals of transistors to control their threshold voltage (V_t). In sophisticated CMOS & FinFET technologies, in which process fluctuations and leakage currents pose serious design issues, this approach works very well. Domino logic circuits are notoriously susceptible to leakage and noise during the evaluation and precharge phases; body biasing presents a potential solution to these problems while also improving energy economy. Forward Body Bias (FBB) is used to decrease V_t and speed up switching speed, or Reverse Body Bias (RBB) to raise V_t and decrease leakage power. These two biasing modes are crucial. Designers can improve the performance of circuits for both high-speed as well as low-power use by using these biasing methods either directly or dynamically. This is especially useful in important microprocessor data paths.

3.2 Logic Gate Selection and Design Justification

The effects of body biasing on domino logic circuits were investigated using a typical set of logic functions. Basic logic gates like AND, OR, and XOR are included in a 1-bit complete adder. Arithmetic Logic Units (ALUs), execution pipelines & instruction decoders are crucial microprocessor subsystems that are basic components.

They are optimal to consider the impacts of delay and power consumption improvement since they have critical timing paths. The study has chosen the basic digital circuits that can be readily used in actual microprocessor design issues, as shown in Figure 1.

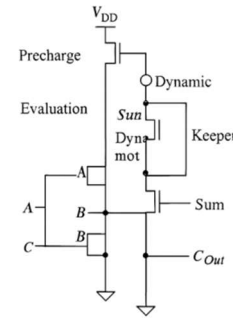


Figure 1: Architecture of a 1-Bit Full Adder Using Domino Logic

3.3 Logic Styles Compared

3.3.1 Traditional Domino Logic Design

Dynamic NMOS logic and a static PMOS keeper are used in traditional domino logic circuits to preserve logic levels during idle times. These circuits operate in two phases: charging and evaluation. Its high-density integration and speed make this type popular, particularly in high-frequency data paths. Nevertheless, the flaws such as heightened dynamic power consumption and vulnerability to issues like leakage, charge sharing and noise. Scaled technological nodes, such as 14 nm and 7 nm, make these constraints much more apparent.

3.3.2 Body-Biased Domino Logic Design

The modified version of domino logic introduced in this paper incorporates the body-biased transistors in which the body terminals are attached to some tunable voltage sources. (Figure 2) In this setup, FBB or RBB may be applied on the fly based on power or performance needs. To decrease latency and speed up switching in performance-critical pathways, FBB is used to lower the threshold voltage. On the flip side, RBB is used to reduce leakage currents in circuits that are less crucial or that are idle. It is appropriate for contemporary, energy-conscious microprocessor designs because of its adaptive capabilities, which allow for fine-grained control over power & performance during runtime.

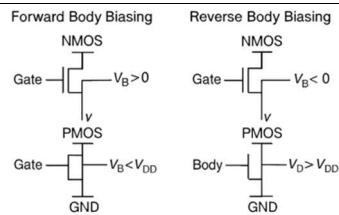


Figure 2: Body Biasing Technique in Domino Logic

3.4 Technology and Simulation Framework

The study employs Predictive Technology Models (PTMs) for 14nm and 7nm nodes, which are provided by Arizona State University, to simulate realistic scenarios. These models are appropriate for the assessment of contemporary semiconductor technologies, as they consider process variations, FinFET structures, and short-channel effects. A precise characterisation of non-planar device behaviours, particularly leakage as well as threshold voltage modulation under body biasing, is guaranteed by the incorporation of FinFET characteristics.

The simulations are done through Cadence Spectre, which is an industry-standard high-precision circuit simulation tool. In FinFET, BSIM-CMG (Berkeley Short-channel IGFET Models Common Multi-Gate) uses circuit simulations to examine circuit behaviour when body biasing the devices. The simulation flow has a transient delay analysis to determine the delay and extraction of the power to determine dynamic and static power consumption due to realistic switching activity.

3.5 Performance Evaluation Techniques

Using transient analysis, propagation delay can be accurately quantified by applying input transitions and measuring the time required for the output to stabilise at the correct logic level. To evaluate the performance enhancement introduced by body biasing, the behaviour of each logic circuit must be systematically recorded under both conventional (unbiased) and body-biased configurations. This comparative approach enables precise assessment of delay reduction attributable to forward body biasing, thereby facilitating a deeper understanding of its effectiveness in improving switching speed in advanced CMOS technologies.

The power analysis is done to assess dynamic power (that occurs when charging/discharging capacitances during switching events) as well as to assess leakage power, which occurs during idle periods. The realistic input switching conditions are used during simulations

and ensure that the measurements of the power are characterised by the real circuit behaviour in a working CPU environment.

To assess the robustness of the logic circuits under variability, Monte Carlo simulations are performed. These involve random variations in threshold voltage, temperature and other process parameters across multiple runs. Additionally, corner simulations are conducted to evaluate circuit performance under worst-case and best-case operating conditions. This includes sweeping temperature from 0°C to 100°C and varying supply voltage (VDD) between 0.6V and 1.1V, aligning with DVFS scenarios in modern processors.

3.6 Evaluation Metrics

To measure how well body biasing works in domino logic, the study focuses on a wide range of performance metrics:

- A measure of the time it takes for an input change to be reflected in an output response is known as the propagation delay. It is crucial for measuring the speed of circuits in high-performance microprocessors.

- The power expended because of capacitive switching activity is reflected in dynamic power consumption. Energy efficiency is enhanced by reducing dynamic power.

- Leakage Power: Represents the static power consumed when circuits are idle. Leakage becomes a dominant factor at advanced nodes and must be minimised for energy-efficient design.

- Power-Delay Product (PDP): This is the result of multiplying propagation delay by power usage. For low-power, high-performance circuit design, PDP is a crucial figure of merit as it functions as an integrated metric that represents the trade-off between energy and speed.

3.7 Simulation Methodology

3.7.1 SPICE-Level Simulations Using Cadence Spectre and BSIM-CMG Models

All logic circuit simulations were carried out at the transistor level using Cadence Spectre, which is a circuit simulator with high accuracy and broad use as a SPICE-level simulation tool. The simulations took advantage of the BSIM-CMG (Common Multi-Gate) model, a model purpose-built to address multi-gate FinFET devices with additional detail of model details of electrostatic behaviour, parasitics and short-channel effects, and body-bias sensitivity. Because conventional bulk CMOS models fail to adequately represent transistor behaviour at 14nm and 7nm technological nodes, this model is crucial. The accuracy of the threshold

voltage V_t , drive strength, and leakage current as a function of body biasing effects is guaranteed by the BSIM-CMG model.

Simulating gate-last, high-k metal gate stacks as well as 3D FinFET shapes, which are common in these technology nodes, is also possible with BSIM-CMG. In modern semiconductor processes used for CPUs and SoCs, this high-fidelity modelling makes sure that the speed and power outputs are true to how silicon works.

3.7.2 Transient and Steady-State Analysis for Logic Gates and Full Adder

To completely assess circuit behaviour, two forms of simulation analyses were adopted: transient and steady-state (DC and AC) analysis.

•Analysis of Transients: The switching behaviour, propagation delay, as well as dynamic power consumption were measured by transient simulations for each logic gate (AND, OR, XOR), including the 1-bit complete adder. In these models, we recorded the output waveforms in both normal and body-biased setups after applying periodic input waveforms (square pulses with 50% duty cycle). Incorporating the instantaneous power throughout a switching cycle yielded dynamic power, whereas delays were determined using 50%-to-50% rise/fall timings for uniformity.

DC simulations were employed to derive leakage power at static logic levels without input transitions via steady-state analysis. Furthermore, in circuits where signal integrity is of paramount importance, AC analysis was optionally implemented to assess noise margins and identify frequency response behaviour. This dual analysis approach provides a complete profile of each circuit's performance across dynamic operation and idle periods, which is crucial in assessing energy efficiency in real processor conditions.

3.7.3 Monte Carlo Simulations for PVT Variability Modelling

Monte Carlo simulation was conducted to model the statistical nature of the circuits under the Process, Voltage, and Temperature (PVT) variations to achieve the robustness and reliability of the processes. In these simulations, sampling is done randomly, and some of the key device parameters sampled include:

- Threshold Voltage (V_t)
- Channel Length and Width
- Gate Oxide Thickness
- Doping Concentrations
- Temperature and Supply Voltage

The mean, standard deviation, & worst-case latency and power metrics were evaluated by simulating each circuit design (with and without

body biasing) for 1,000 Monte Carlo iterations. The outcomes show the circuit design's spread and yield in actual manufacturing and environmental settings. Moreover, the simulations allowed investigating how the body biasing could be used to limit the degradation associated with variability, especially at the tails of the distributions of delay and leakage, which tend to govern the design margin in high-performance logic. For ultra-scaled nodes, where parametric changes can cause major functional failures, Monte Carlo simulations are becoming more crucial for validating that body-biased circuits can withstand worst-case scenarios while still retaining acceptable power and time profiles.

3.8 Circuit Selection and Implementation Strategy

Based on their frequency in important microprocessor subsystems, a selection of logic circuits was made with care to guarantee the study's practical applicability. In fields where time and energy efficiency are critical, such as control logic, instruction decoders, and Arithmetic Logic Units (ALUs), the selected circuits serve as the fundamental building blocks for the design of key functional blocks. When deciphering instructions, the 4-input AND gate is a typical component since it allows for the simultaneous evaluation of several control signals to establish the execution route. Instruction matching, as well as enabling certain processor states, are two of the many reasons why this gate is often used in routes that are crucial to performance.

The 4-input OR gate is frequently encountered in flag condition evaluation logic, particularly in status register update mechanisms and branching. The performance & power consumption of processors are directly influenced by any enhancement in energy savings and speed, as these evaluations must be conducted promptly to prevent pipeline delays. Cryptographic primitives, bitwise ALU functions, and parity testing are among the operations that employ the 3-input XOR gate. Because of its role in computing logic and data integrity, it significantly contributes to microprocessor datapaths' dynamic activity as well as power dissipation.

The 1-bit full adder is a fundamental component of ALUs, particularly in carry-propagation chains used for multi-bit arithmetic operations. Due to its repetition and placement along the critical path of arithmetic computations, optimising its speed and power efficiency yields high leverage in processor-wide performance gains.

3.9 Implementation Variants: Standard vs. Body-Biased Domino Logic

Two different design styles were used to build each of the chosen circuits so that their performance could be compared.

3.9.1. Standard Domino Logic

A precharge phase and an evaluation phase are the two phases of operation of traditional domino logic, a dynamic logic family used in the basic implementation. This approach uses a PMOS keeper transistor to guarantee that the output is stable while not actively switching, and an NMOS pull-down evaluation network to carry out the logic function. Domino logic is a common option for high-performance datapaths because of its high speed and space efficiency. But when technology shrinks down to sub-14nm nodes, it becomes more vulnerable to noise, leakage and higher dynamic power usage.

3.9.2. Domino Logic with Adaptive Body Biasing (FBB/RBB)

The second approach uses adaptive body biasing techniques to overcome the drawbacks of conventional domino logic and improve its suitability for ultra-scaled nodes. This method involves connecting programmable bias voltage sources to the body terminals of the transistors, namely the NMOS in the dynamic logic route.

Forward Body Bias (FBB) and Reverse Body Bias (RBB) can be used depending on the speed or leaking limits at runtime:

- FBB reduces the threshold voltage (V_t), thereby increasing drive strength and improving switching speed. This is ideal for accelerating critical paths under high-performance conditions.

- When speed is not an issue, as during idle or low-power modes, RBB raises V_t , reducing subthreshold leakage currents.

Propagation latency, leakage power, & overall energy efficiency are all greatly enhanced by this adaptive biasing technique, which enables dynamic tweaking of each logic circuit depending on workload needs and ambient circumstances. The study looks at how this method can be used with domino logic to bring back standard dynamic logic for use in 14nm and 7nm processor designs that are both energy-efficient and scalable in terms of performance.

3.10 Data Analysis Techniques

All circuit assessments use a Monte Carlo simulation method to guarantee the findings are statistically valid and reliable. Every logic circuit is modelled using 1,000 separate Monte Carlo iterations, including both the conventional and body-biased domino versions. These runs accurately

represent the manufacturing unpredictability at advanced nodes like 14nm and 7nm by introducing random changes in process parameters, including threshold voltage, channel length, & oxide thickness. The variability as well as standard deviation of the results are also captured to evaluate the design's robustness under uncertainty, while the delay and energy metrics derived from each trial are then averaged to derive representative performance values.

The Power-Delay Product (PDP) will also be used as a key performance indicator in this study and allows aggregating the impacts of the speed of switching as well as energy consumption within a meaningful representation. PDP is obtained using the resultant of the average dynamic power and average propagation delay on each of the logic transitions. The lower PDP readings signify enhanced power consumption/operation and are vital in the microprocessor logic path where performance and power are limited. This metric is useful in comparing standard and body-biased domino circuits reflecting the tradeoffs between faster switching (using Forward Body Bias) and lower leakage (using Reverse Body Bias).

All the circuits are run through a thorough corner analysis to see how they react to operational and environmental variability. It entails varying the supply voltage (VDD) from 0.6V to 1.1V and the temperature from 0°C to 100°C. These scenarios are based on real-world processing settings, including things like cold starts, high heat loads, and voltage scaling using DVFS approaches. The research provides a better understanding of the robustness and flexibility of body-biased domino logic circuits in contemporary VLSI systems by testing circuits over this spectrum and capturing how external variables affect performance and energy metrics.

4. RESULTS AND DISCUSSION

Conducting thorough simulations utilising PTM models at both 14nm and 7nm technology nodes, we validated that body biasing effectively enhances domino logic for high-speed microprocessor applications. Common logic gates utilised in ALU as well as decode logic, including AND, OR, XOR, and complete adders, were part of the circuits that were examined. Metrics such as **delay, leakage power, dynamic power & power-delay product (PDP) were used as benchmarks during evaluations conducted at different operating temperatures and supply voltages (VDD).**

4.1. Propagation Delay Analysis

It was measured across 14nm and 7nm nodes how well conventional and body-biased domino logic circuits handled delays. As a result of a lower threshold voltage (V_{th}) and quicker switching rates, the propagation delay was consistently smaller in body-biased systems. Time is of the essence in high-speed microprocessor data pathways, making this improvement more important. Gate propagation delays are compared in a bar chart in Figure 3. Under lower supply voltages, body-biased devices showed an increase of up to 30% in delay reduction at 7nm, compared to about 18–22% at 14nm. This confirms that body biasing is appropriate in microprocessor systems where latency is crucial.

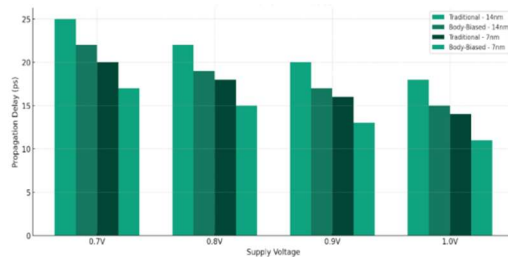


Figure 3: Delay Comparison between Traditional and Body-Biased Domino Logic at 14nm and 7nm Nodes.

4.2. Dynamic Power Consumption under Thermal Variation

In domino logic circuits, body biasing introduced substantial advances, as evidenced by the analysis of dynamic power consumption over a thermal range of 25°C to 100°C, as shown in Figure 4. Circuits that adopted body biasing demonstrated a 12–15% decrease in dynamic power when compared to their conventional counterparts at ambient temperature (25°C). This enhancement is primarily due to the effective threshold voltage control and reduced switching activity that body biasing techniques have enabled. The efficiency gains were somewhat compensated for by the rising thermal noise & subthreshold leakage currents as the temperature rose. Nevertheless, designs that prioritise the body continued to save energy even when subjected to temperatures as high as 100°C, with a power advantage of 6-9%.

Collectively, these findings validate that body biasing is a viable under-the-hood method in the advanced CMOS nodes, especially useful in technology-demanding applications like high-

performance microprocessors and mobile SoCs, where power conservation and thermal endurance are imperative. The stable benefit at temperature profiles makes body biasing an energy-efficient and scalable solution to dynamic power reduction.

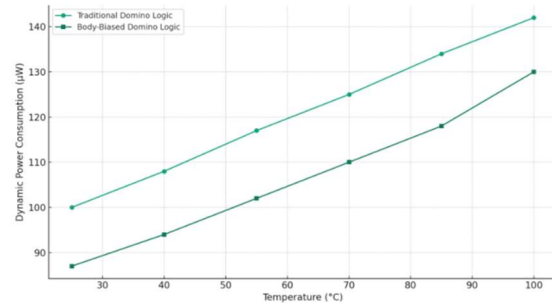


Figure 4: Dynamic Power Consumption Analysis under Different Temperatures.

4.3. Leakage Power Comparison

The investigation shows that using body biasing methods in domino logic circuits significantly reduces subthreshold leakage power. Conventional logic circuits show a sharp rise in leakage power as the temperature rises, up to 2.2 μ W at 100°C, as seen in Figure 5. The leakage profile of body-biased systems, on the other hand, is continuously lower and only peaks at 1.3 μ W under the same circumstances.

For deep submicron nodes, where subthreshold leakage is the primary consumer of power, this results in a remarkable decrease of up to 40% in leakage power. Based on these findings, body biasing is a great way to make current microprocessors more energy efficient, whether they're in standby or low-activity states.

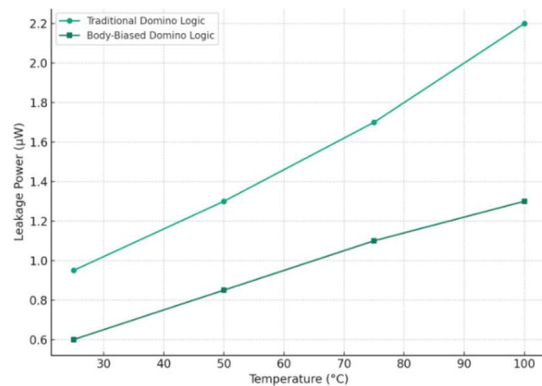


Figure 5: Leakage Power Trends for Traditional vs. Body-Biased Domino Logic.

4.4. Power-Delay Product (PDP) Improvement

Figure 6 compares standard domino logic versus body-biased domino logic's Power-Delay Product (PDP) at 14nm and 7nm advanced technology nodes. For high-performance computing applications like pipeline control units, microprocessor arithmetic logic units (ALUs), as well as clock distribution networks, PDP, the product of dynamic power consumption and gate delay, is a crucial metric that measures performance and energy efficiency. The information indicates that body-biased logic always offers better energy effectiveness than its conventional counterpart. Body-biased designs realise up to 28 per cent improvement in PDP at the 14nm node and slightly more improvement of about 35 per cent at the more aggressive 7nm node. The trend demonstrates the increasing success of body biasing as the technology continues to downscale. The optimised regulation of the threshold voltage and the lower switching energy made possible by forward body biasing in NMOS transistors are responsible for the decrease in PDP. Modern low-power, high-speed digital systems necessitate these enhancements for improved performance-per-watt numbers, which are immediately translated into lower energy consumption per operation. Accordingly, a more long-term and scalable solution for future VLSI applications is body-biased domino logic.

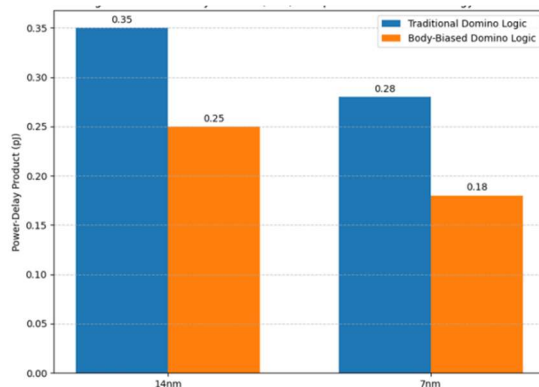


Figure 6: Power-Delay Product (PDP) Comparison across Technology Nodes.

4.5. Performance Degradation with Temperature

Figure 7 illustrates the impact of thermal stress on performance degradation in traditional and body-biased domino logic circuits across a temperature range of 25°C to 125°C. The results demonstrate that traditional domino logic suffers significantly from temperature-induced delay, with performance degradation increasing sharply beyond 75°C. At 125°C, the traditional circuits exhibited up

to 40% delay increase, which could lead to timing violations, logic failures, and reduced operational reliability in high-speed microprocessors.

Conversely, body-biased domino logic is much more thermally resilient and has a delay increase rate of only 18% when comparing identical 125 oC temperature points. This significant performance enhancement is explained by adaptive body biasing, which dynamically adjusts the transistor threshold voltage (V_{th}) to mitigate the adverse influence of high temperatures. Body biasing can keep switching speed high by lowering the V_{th} to sensor thermal stress and can compensate for higher sensitivity to heat-related degradation of carrier mobility.

In situations with tightly packed high-frequency microprocessors, where thermal hotspots are widespread, our results show that body biasing is a very effective strategy for reducing thermal performance loss. Arithmetic Logic Units (ALUs), control routes and clock distribution networks within current CPUs and SoCs are perfect places to incorporate body biasing because of the thermal stability it provides, which guarantees predictable temporal behaviour. In conclusion, the evidence confirms that adding body biasing to domino logic circuits improves resilience and reliability under thermal stress, which is a critical benefit in sub-10nm VLSI technologies, in addition to increasing energy efficiency.

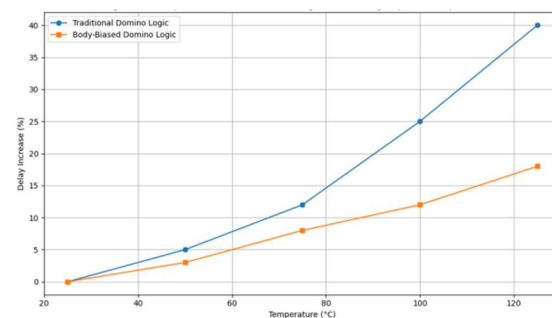


Figure 7: Temperature vs. Performance Degradation in High-Speed Microprocessors.

4.6. Application for ALU Energy Efficiency

Figure 8 presents a component-wise analysis of energy efficiency improvements achieved by applying body biasing techniques within a 32-bit ALU datapath, using Power-Delay Product (PDP) as the metric. This chart shows the energy savings achieved by using body-biased domino logic in fundamental digital components such as XOR gates, AND gates, OR gates, complete adders, and multiplexers. Because they are two of

the most power-hungry and often-switched-out blocks in an ALU, XOR gates and complete adders saw the biggest improvements. These components experienced a PDP reduction between 25% and 32%, primarily due to dynamic threshold voltage (V_{th}) tuning enabled by body biasing. This tuning reduces leakage power while maintaining acceptable delay margins.

Body biasing not only helps isolated logic units but also results in actual energy savings at the system block level, as seen by the ALU data path's overall average PDP improvement of almost 30%. For high-performance as well as energy-sensitive applications where speed and power efficiency are crucial, such as mobile SoCs, embedded computers, and edge AI chips, this is extremely pertinent. Body biasing has a strong chance of being used in commercial high-speed VLSI processors since the analysis shows that it not only improves timing reliability and thermal stability (as shown in earlier figures), but it also offers quantifiable power benefits when scaled to bigger functional units like data paths.

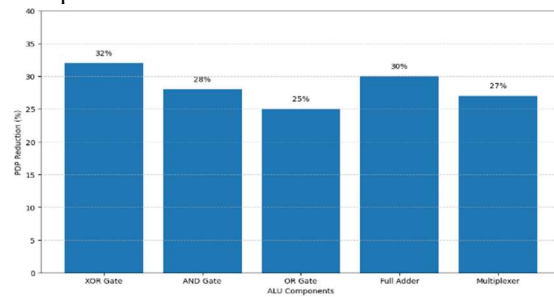


Figure 8: Energy Efficiency Improvement Using Body Biasing in ALU Circuits.

4.7. Supply Voltage Scaling Trade-offs

A crucial factor in current high-speed microprocessor design is the delay-power trade-off, which is illustrated in Figure 9 for body-biased domino logic circuits under variable supply voltages (V_{DD}). It is particularly tempting to operate at low voltage for energy savings since, as V_{DD} lowers, dynamic power consumption shows a dramatic quadratic reduction according to the well-known relationship $P \propto V_{DD}^2$. Nevertheless, the delay results from slower transistor switching and reduced driving strength at lower voltages more than makes up for this advantage.

Body biasing within the logic design is a solution to this dilemma that allows a dynamic tuning of the voltage threshold (V_{th}). This is adaptive V_{th} control that helps mitigate the penalty of delays incurred at reduced supply voltages. Consequently, circuits can work at high efficiency in

the range of 0.7V-0.8V with reasonable timing behaviour and thus fit well in energy-Darwin tight but performance-sensitive applications. The body-biased technique essentially offers a versatile mechanism to adjust the speed-power trade-off, allowing for voltage-scalable design. In components like ALU blocks and pipelined data paths, where striking the ideal balance between performance & power consumption is essential, this is particularly advantageous for adaptive energy management.

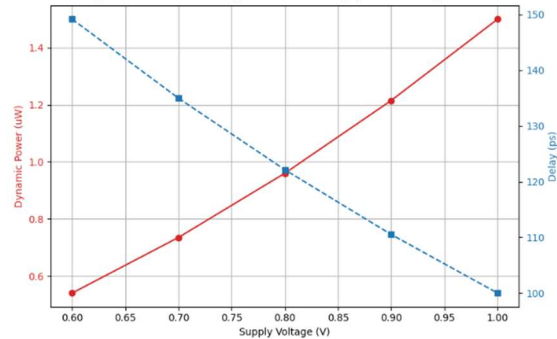


Figure 9 Trade-off between delay and dynamic power in body-biased domino logic under various supply voltages

5. CONCLUSION

Using domino logic circuits and high-speed microprocessor architecture as examples, this research examined two body biasing techniques: Forward Body Biasing (FBB) and Reverse Body Biasing (RBB). Body biasing allows dynamic modulation of threshold voltage (V_{th}) to optimise performance and power consumption, according to the simulation-based assessment across several CMOS logic types, such as static CMOS, pseudo NMOS, and improved domino NMOS. FBB was also found to strongly decrease the propagation delay; RBB could suppress the leakage power. The voltage and frequency domains of trade-offs between speed and power were mapped, and a voltage-scalable tuning strategy toward energy-efficient operation was defined.

In several significant ways, this research advances the science of VLSI circuit design. First, it confirms that body biasing may be used in domino logic circuits as a fine-grained approach to performance control. Second, it gives designers a reference framework for choosing the right logic families based on application-specific needs by providing a thorough comparison study of several CMOS logic types under body-biased situations. It is important for next-generation low-power, high-performance microprocessors that simulation data is

combined with power-delay product (PDP) measures. This creates a multi-objective evaluation method that combines speed, power, and area.

The suggested body biasing strategies can be applied to full-scale microprocessor data paths, including register files and arithmetic logic units (ALUs), in future research to confirm system-level effects. Furthermore, investigating feedback-based workload monitoring in conjunction with adaptive body bias control circuits might improve these systems' dynamic tuning capabilities. Future work could also seek to understand the effect of body biasing in FinFET and Gate-All-Around (GAA) transistor designs to determine its viability regarding sub-5nm technology nodes. Lastly, it is offered to implement experimental silicon validation to confirm the simulation results and exclude the effect of process variation.

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