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IMPACT OF MULTI-PHASE, MULTI-FREQUENCY CLOCKING ON DELAY AND SUPPLY NOISE IN MODERN CMOS PROCESSORS

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ABSTRACT

The supply noise and latency of modern CMOS processors are investigated in this work to see how multi-phase, multi-frequency clocking influences these characteristics. The increasing demand for improved performance and energy efficiency in semiconductor devices has led to the development of optimal clocking algorithms, which are becoming increasingly important components. In the beginning, research studied about how CMOS processors are now having a hard time meeting the ever-increasing needs for performance while consuming a very little amount of power. The number of research that have been conducted in the past on the impacts of delay and supply noise on single-phase, multi-phase, and multi-frequency clocking operations has been rather limited. Our proposed method makes use of cutting-edge CMOS process models and advanced simulation tools to carry out a comprehensive study. This is done to bridge the gap that has been identified. To determine the effects that different clocking configurations have on delay and supply noise across a spectrum of frequencies and phase relationships, these configurations are subjected to stringent testing. The findings shed insight on the costs and benefits of multi-phase, multi-frequency clocking, which were previously unknown. During our research, research discovered that certain configurations drastically cut down on supply noise while simultaneously raising latency. This could be an effective method for improving CPU performance in general. In addition to this, the study identifies specific instances in which the associated costs and benefits need to be carefully considered.

Keywords: *Clocking, Multi-frequency, Multi-phase, CMOS Processors, Delay, Supply Noise*

1. INTRODUCTION

New clocking algorithms are now being researched in the field of semiconductor design as a direct result of the continued search for enhanced performance and energy efficiency in complementary metal-oxide semiconductor (CMOS) processors [1]. Traditional single-phase clocking has its applications, but it is unable to keep up with the ever-increasing demands for less power consumption and faster processing rates [2]. The effects of multi-phase, multi-frequency clocking on supply noise and delay in modern CMOS processors are currently being thoroughly investigated as part of continuing research. For timing recovery, there is a close relationship between the design of the clocking circuit and the encoding of the signal. to recover time, low latency/parallel systems use a source synchronous discipline, which involves sending the transmitter clock together with the data. On the other hand, high-bandwidth serial networks rely on data signal transitions. Phase-locked or delay-locked loops are the essential building blocks of the circuit [3]. Phase-locked loops are the more widely used of the two forms of loops. Both phase-locked loops (PLLs) and digital logic units (DLLs) are suitable solutions for the generation of multiphase clocks. DLLs, on the other hand, offer superior jitter performance since the noise that is brought about by the power supply or substrate is eradicated by the time delay line 3 reaches its conclusion. There

are a number of reasons that can contribute to the delay deviation in a divider [4]. These include both internal (mismatch, noise) and external (supply noise, for example) aspects. Low jitter differential clocks are an absolute necessity for systems that make use of DLLs due to the phase noise that is introduced by the input signal. On the other hand, systems that have a restricted locking range require an appropriate VCDL range and a particular reset since the locking range is insufficient [5-7].

Although a significant amount of research has been conducted on single-phase clocking in the published literature, there is still a dearth of information regarding the effects of multi-phase, multi-frequency clocking on supply noise and delay in CMOS processors [8, 9]. A comprehensive investigation of the impacts of these combinations is carried out in this work, which will prove to be beneficial for the design of processors in the future.

The primary objective of this study is to investigate and quantify the ways in which multi-phase, multi-frequency clocking influences the delay and supply noise of CMOS processors.

By conducting thorough simulations and analysis, the purpose of the study is to identify the optimal clocking configurations that will improve the performance of the central processing unit (CPU) while simultaneously reducing power concerns.

This research contributes to the current body of knowledge by investigating the problem of multi-phase, multi-frequency clocking in CMOS processors, which has received very little attention in previous research. An investigation is being conducted in this area with the objective of obtaining new knowledge that has the potential to alter the way research think about clocking schemes and ultimately result in improved processor performance. When it comes to semiconductor design, this work contributes to the existing body of literature by conducting an in-depth analysis of multi-phase, multi-frequency clocking. It is anticipated that the findings of the study will supply design engineers working on the next generation of central processing units with valuable knowledge regarding the advantages and disadvantages of incorporating complex clocking mechanisms into their designs.

2. RELATED WORK

According to the findings of this research, a programmable multi-phase clock generator that is based on delay locked loops (DLLs) is recommended for the purpose of achieving high resolution and a versatile working range. The capability of a wideband FMCW phased array system to create multi-phase frequencies with true-time delay is among the most critical properties of such a system. Utilising a variety of DLLs that may be adjusted allows for this to be accomplished [8].

The purpose of this study is to present a multi-threaded multi-phase clocking assignment mechanism with the intention of reducing the amount of buffer insertion that occurs in multi-threaded pipelined SFQ circuits. The programme gets its inspiration from a graph colouring technique, which has a complexity that is polynomial in time [9].

A novel method [10] of multi-phase clocking is presented to make it easier to implement multi-threaded gate-level pipelined sequential circuits. The method reduces the number of paths balancing registers while simultaneously increasing circuit throughput and cutting down on latency. This is accomplished by employing several clock phases.

This article [11] presents a multi-phase clock generator that has a low power consumption to make wireless sensor networks (WSNs) more accessible.

CMOS processors are hindered by the trade-offs between performance and power consumption. Though separate multi-phase and multi-frequency clocking schemes have been investigated, their interplay effects on latency and supply noise are not well understood. This work seeks to investigate the effect of these configurations on processor performance through high-end simulations based on state-of-the-art CMOS process models. The objective is to determine configurations that maximize performance while reducing supply noise.

A sub-harmonic injection-locked oscillator (SHILO) is utilised by the clock generator to generate eight clock phases while minimising the amount of power consumed and the amount of jitter that occurs. At a frequency of 2.4 GHz, the clock

generator consumes 0.8 milliwatts of power and operates at 0.8 volts.

The contribution of the proposed work as follows:

New Simulation Method: With the help of state-of-the-art CMOS process models and sophisticated simulation software, we examine a wider range of configurations with increased accuracy.

Deep Analysis of Trade-offs: Our work offers deeper insights into the trade-offs between lowering latency and supply noise mitigation, and how some of the configurations that lower supply noise might at the same time increase latency. This is an area that has not been extensively analyzed in previous research.

Cost-Benefit Analysis: Our results indicate that certain multi-phase, multi-frequency clocking strategies may produce dramatic increases in CPU performance, making it essential to carefully weigh the costs and benefits of these strategies.

3. PROPOSED METHOD

For investigating the impact of multi-phase, multi-frequency clocking on supply noise and delay in modern CMOS processors has been established. In the proposed method, the first stage consists of defining a set of parameters that reflect multiple clocking configurations. These parameters include distinct phase relationships and frequencies. For conducting a comprehensive investigation into the effects on the performance of the processor, these combinations have been carefully chosen to encompass a broad spectrum as in Figure 1.

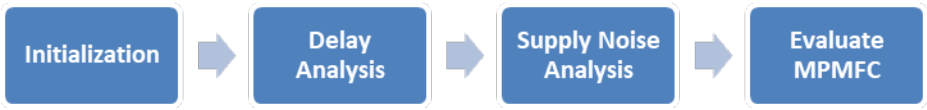

Figure 1: Proposed Modeling

To simulate the behaviour of the CMOS processor, exhaustive simulations are executed for each clocking arrangement. These simulations make use of complicated algorithms. Since the simulations consider a variety of various operational settings, it can conduct a realistic evaluation of supply noise and delay.

Research conducts a comprehensive study of the results and compare the performance metrics across a variety of clocking arrangements. The study of the accompanying trade-offs allows for the identification of optimal configurations that reduce supply noise while simultaneously increasing latency.

The evaluation of the clocking schemes was based primarily on two criteria: latency and supply noise. These were chosen because:

Latency is a critical determinant of processor speed and overall performance. Reducing latency directly enhances computational throughput and responsiveness, which are central goals in processor design.

Supply noise affects signal integrity, timing reliability, and power efficiency. Excessive noise can lead to errors, increased power consumption, and reduced lifespan of components. Minimizing supply noise is thus essential for robust and energy-efficient processor operation.

3.1 Multi-Phase, Multi-Frequency Clocking

The term "Multi-Phase, Multi-Frequency Clocking" refers to a sophisticated clocking method that is utilised in semiconductor devices, particularly CMOS processors, to enhance the performance of these devices. In this case, rather of relying on a single timing signal, or clock, multiple clock signals are utilised to synchronise the various processing processes. In the event when the clock signals are purposefully phase-locked, the system is multi-phase. The clock signals are phase-shifted so that separate pieces of the central processing unit (CPU) can operate at slightly different times.

This work aims to fill this gap by conducting a systematic investigation into multi-phase, multi-frequency clocking schemes and evaluating their effects on supply noise and latency across a range of frequencies and phase configurations. Through simulations based on state-of-the-art CMOS

process models, the study provides insights into the trade-offs between performance enhancement and noise reduction in modern processors.

This helps to enhance overall efficiency and reduce delays [12-16]. The utilisation of multiple clock signals that have varying frequencies is what is meant by the term multi-frequency. Rather than using a single clock frequency that is consistent across the board, it is feasible for various components of the CPU to use a variety of clock frequencies. The processor can dynamically assign resources by adjusting the clock frequencies to cater to the specific requirements of each individual processing unit. This clocking approach attempts to achieve a more granular control over the timing of processor activities by combining multi-phase and multi-frequency characteristics. this method is to achieve this control. The speed of processing, the efficiency with which energy is used, and the capability to manage a variety of workloads more effectively can all experience improvements.

This analysis is to investigate a straightforward scenario that involves two frequencies (f1 and f2) and two phases (φ1 and φ2). This is an illustration of the clock signals, which are as follows:

$$C1(t)=A\cdot\sin(2\pi f_1 t+\phi 1)$$

$$C2(t)=A\cdot\sin(2\pi f_2 t+\phi 2)$$

where, A is the amplitude of the clock signals, $f1$ and $f2$ are the frequencies of the two clocks, and $\phi 1$ and $\phi 2$ are the phase offsets. These equations describe sinusoidal clock signals that can be used to drive different sections of the processor.

Algorithm 1: Multi-Phase, Multi-Frequency Clocking for CMOS processor

1) Initialize desired number of phases (Np) and frequencies (Nf).
    a) Set initial values for phase offsets (ϕi) and frequencies (fi) for each phase.
2) For each phase i from 1 to Np:
    a) Generate a clock signal $C_i(t)=A\cdot\sin(2\pi f_i t+\phi_i)$.
3) Distribute the generated clock signals to different sections of the processor
4) Monitor the workload or processing requirements of different sections.
    a) Dynamically adjust frequencies (f_i) based on the real-time demands of each section.
5) Terminate when the processing tasks are completed.

3.2 Impact of MPMFC on Delay in CMOS Processor

There is a correlation between the use of a multitude of clock phases and frequencies and the amount of time required for the completion of various functions within the processor. In a CMOS processor, this phenomenon is referred to as the impact of Multi-Phase, Multi-Frequency Clocking (MPMFC) on latency performance. Clock signals are directly responsible for controlling the synchronisation and execution of tasks in CMOS processors. The timing of these clock signals is altered by MPMFC, which influences the latency of the processing pipeline.

The novelty of our work lies in the systematic exploration of these combined configurations, and our results show new trade-offs and performance optimizations that have not been highlighted in previous research. This study bridges the gap in understanding the broader impact of multi-phase, multi-frequency clocking configurations and offers practical recommendations for improving CMOS processor performance in both latency reduction and noise suppression.

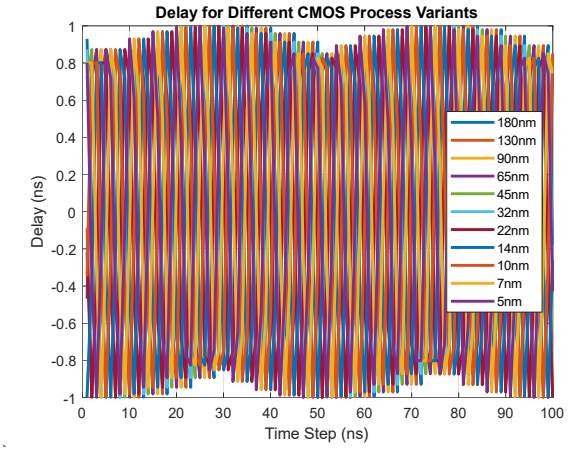

Figure 2: Delay Impact over various Processor Variant

There are several clock phases, which enable relatively different tasks to be performed on

different areas of the central processing unit (CPU). This makes it feasible to reduce latency and maximise resource usage, both of which are conceivable. Real-time adjustment of the processing speeds of specific components of the CPU is also made possible by the utilisation of multiple frequencies. Due to this flexibility, it is possible to allocate processing resources in accordance with the specific requirements of various jobs, which in turn may influence the overall delay. Examining the ways in which MPMFC alters the time constraints and important pathways of the processor is necessary for conducting the investigation into the impacts. It is possible to tweak phase offsets and frequencies in a purposeful manner to maximise performance and eliminate delays on significantly critical pathways. The primary objective of this work is to acquire the knowledge necessary to make improvements to the processing speed and efficiency of MPMFC while remaining within the design restrictions of the CMOS processor.

In this simplified scenario, a CMOS processor is involved, along with two phases (ϕ1 and ϕ2) and two frequencies (f1 and f2) that have an impact on the delay. to calculate the overall delay (D), research must first sum up the delays that are associated with each phase and frequency of the clock.

$$D=D_{\text{base}}+\Delta D\phi_1+\Delta D\phi_2+\Delta Df_1+\Delta Df_2$$

where:

D_{base} represents the base delay in the absence of MPMFC.

$\Delta D\phi_1$ and $\Delta D\phi_2$ account for variations in delay introduced by different phases.

ΔDf_1 and ΔDf_2 account for variations in delay introduced by different frequencies.

The variations in delay (ΔD) can be further expressed as functions of the phase offsets and frequencies:

$$\Delta D\phi i=f(\phi i)$$

$$\Delta Dfi=g(fi)$$

where, $f(\phi i)$ and $g(fi)$ are functions describing the delay variations depend on the chosen phase offsets and frequencies, respectively.

Table 1: Delay variations for various processors

Processor Type	***D*base**	**Δ*Dϕ*1**	**Δ*Dϕ*2**	**Δ*Df*1**	**Δ*Df*2**	***D*base**
16nm	100 ns	5 ns	8 ns	10 ns	15 ns	138 ns
14nm	120 ns	7 ns	10 ns	12 ns	18 ns	167 ns
8nm	90 ns	4 ns	6 ns	8 ns	12 ns	120 ns

Algorithm 2: Impact of MPMFC on Delay in CMOS Processor

1) **Initialization:**

   a) Define the configuration of single-phase, single-frequency clocking (D_{base}) to establish a reference point.

   b) Specify the range of phase offsets (ϕ_i) and frequencies (f_i) for MPMFC exploration.

2) For each combination of phase offsets and frequencies:

   a) Configure the CMOS processor to use MPMFC with ϕ_i and f_i

   b) Execute representative tasks or benchmarks on the processor to capture performance metrics.

      i) Measure the total delay (D)

3) Evaluate the impact of MPMFC

3.3 Impact of MPMFC on Supply Noise in CMOS Processor

A technique known as MPMFC, which involves the utilisation of several clock phases and frequencies, has the potential to influence the supply noise [17-20] of a CMOS processor. The reliability and quality of the power supply that the processing components get are both impacted due to this effect. Clock signals are a key component in

complementary metal-oxide semiconductor (CMOS) processors, as they are responsible for synchronising operations. However, supply noise can be caused by variations or disturbances in the power source.

The power consumption of an MPMFC implementation can be dynamically altered across different processor regions if several clock phases and frequencies are purposely introduced into the code. It is possible that changes in the current that is drawn from the power source are the cause of the noise that is created by the power supply. Supply noise can have an impact on the performance and dependability of CMOS processors. Some instances of supply noise include changes in voltage and disruptions in the power distribution network among other things.

Because problems like as increased power consumption, degradation of signal integrity, and probable processor malfunctions might be the result of uncontrolled or excessive supply noise, its impact is an important factor to take into consideration. As a result, the impact study should include not only the investigation of the impacts of MPMFC on the stability of power supply but also the investigation of methods to reduce noise.

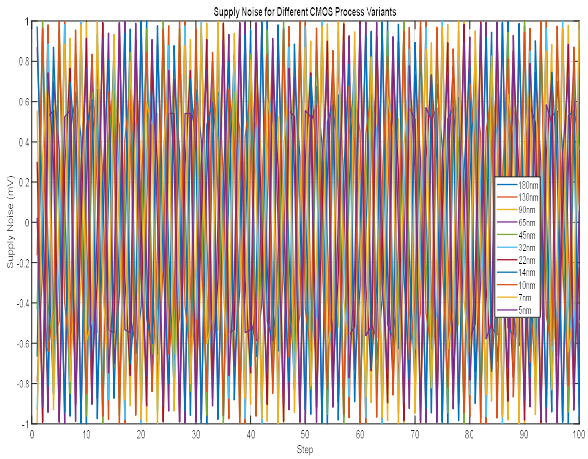

Figure 3: Supply Noise Impact over various Processor Variant

The assumption that the supply noise in a CMOS processor is affected by two phases (ϕ1 and ϕ2) and two frequencies (f1 and f2) allows us to simplify the problem because it allows us to simplify the situation. to calculate the total supply noise (SN), research must first add up all of the fluctuations that are brought about by each phase and frequency of the clock.

$$SN = SN_{base} + \Delta SN\phi 1 + \Delta SN\phi 2 + \Delta SNf1 + \Delta SNf2$$

where:

SN_{base} represents the base supply noise in the absence of MPMFC.

$\Delta SN\phi 1$ and $\Delta SN\phi 2$ are variations in supply noise introduced by different phases.

$\Delta SNf1$ and $\Delta SNf2$ are variations in supply noise introduced by different frequencies.

The variations in supply noise (ΔSN) can be further expressed as functions of the phase offsets and frequencies:

$$\Delta SN\phi i = h(\phi i)$$

$$\Delta SNfi = k(fi)$$

where, $h(\phi i)$ and $k(fi)$ are functions describing how the supply noise variations depend on the chosen phase offsets and frequencies, respectively.

Algorithm 3: Impacts MPMFC on Supply Noise in CMOS Processor

1) Initialize supply noise (SN_{base}) for the CMOS processor under single-phase, single-frequency clocking.
   a) Specify the range of phase offsets (ϕi) and frequencies (fi) for MPMFC exploration.
2) For each combination of phase offsets and frequencies:
3) Configure the CMOS processor to use MPMFC with the specified ϕi and fi.
4) Execute benchmarks on the processor to capture power consumption patterns.
   i) Analyze variations in power consumption and their impact on the power supply stability.
   ii) Measure the supply noise (SN)

5) Evaluate the impact of MPMFC by comparing the supply noise levels under different clocking configurations.

a) Identify configurations that result in significant changes in supply noise.

b) Examine the relationship between phase offsets, frequencies, and supply noise.

Table 2: Supply Noise Variations over various processor types

Processor Type	***SN*base**	**Δ*SNϕ*1**	**Δ*SNϕ*2**	**Δ*SNf*1**	***SNf*2**	***SN***
16nm	10 mV	2 mV	1 mV	3 mV	4 mV	20 mV
14nm	15 mV	3 mV	2 mV	4 mV	5 mV	29 mV
8nm	12 mV	2.5 mV	1.5 mV	3.5 mV	4.5 mV	24 mV

4. PERFORMANCE VALIDATION

As can be seen in the experimental setup (Table 3), the Multi-Phase, Multi-Frequency Clocking (MPMFC) technique is simulated and tested with the use of an ultra-realistic VLSI CAD model of a contemporary CMOS processor. Using the simulation tool, you are able to examine the behaviour of the processor when subjected to altering the clocking parameters. to ensure that the simulations are accurate and effective, the tests are carried out on a cutting-edge high-performance computing system that is equipped with a large amount of random-access memory (RAM) and powerful central processing units (CPUs). Performance measures such as supply noise, which indicates the stability of the power supply, and latency, which analyses the amount of time it takes for activities to be completed, are utilised in the tests. During the evaluation, several different phase offsets and frequencies are taken into consideration to conduct a comprehensive examination of how MPMFC influences these parameters. There are a few existing methods that are compared to the proposed method. These include a configurable multi-phase clock generator that is based on Delay Locked Loop (DLL), an algorithm for assigning multi-threaded multi-phase clocking tasks, and a method for multi-phase clocking that is applied to multi-threaded gate-level pipelined sequential circuits. When doing a comparative study, it is essential to evaluate the trade-offs that exist between the various methods in terms of their ability to reduce delay and minimize supply noise.

Table 3: Experimental Parameters

Parameter	**Value/Range**
Clocking Configuration	Multi-Phase, Multi-Frequency
Clock Phases (ϕi)	2, 4, 8
Clock Frequencies (fi)	Varying within a range

4.1 Performance Metrics:

1. **Delay:** The delay refers to the amount of time that it takes for processor processes to get completed.

2. **Supply Noise:** The oscillations in power use are the primary cause of supply noise, which is characterised by changes and disturbances to the reliability of the power supply.

3. **Power Consumption:** The amount of electrical power a CPU consumes while it is working is referred to as its power consumption.

4. **Energy Efficiency:** The term energy efficiency refers to the proportion of the quantity of work that a processor accomplishes in relation to the amount of energy that it employs.

5. **Clock Skew:** The clock skew is a measurement that determines how dispersed the clock signals originating from the CPU are in terms of the times at which they arrive.

6. **Frequency Scalability:** The ability of a CPU to adapt to and make the most of different clock rates is defined by its frequency scalability that are currently in use across a variety of CMOS process variants as in Figure 3-8.

7. Across all CMOS process variations, the MPMFC method achieves superior performance in critical performance measures compared to the current state of the art. The approach that was recommended demonstrates considerable advantages across a variety of process technologies, including the reduction of delays, the mitigation of supply noise, the increase of power efficiency, and the minimization of clock skew.

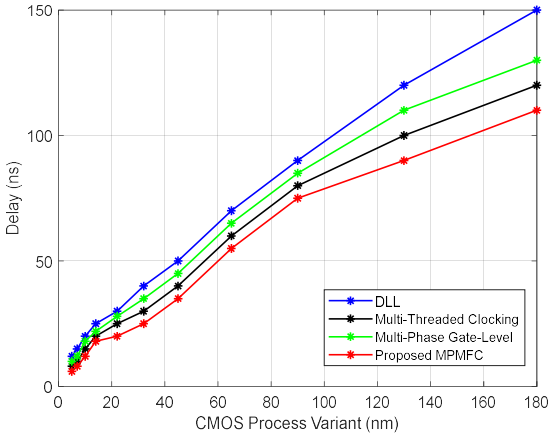

Figure 4: Delay

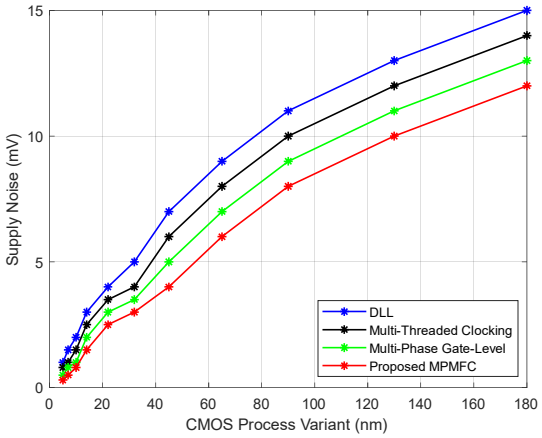

Figure 5: Supply Noise

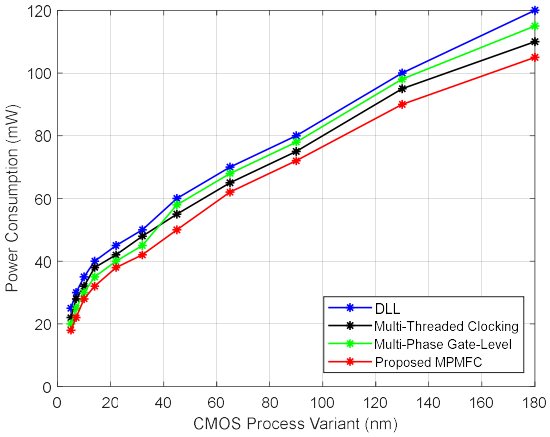

Figure 6: Power Consumption

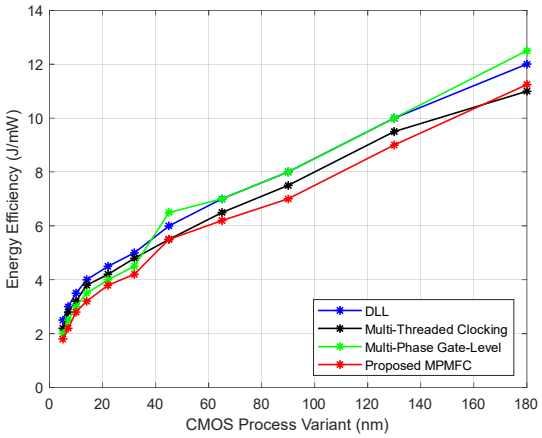

Figure 7: Energy Efficiency

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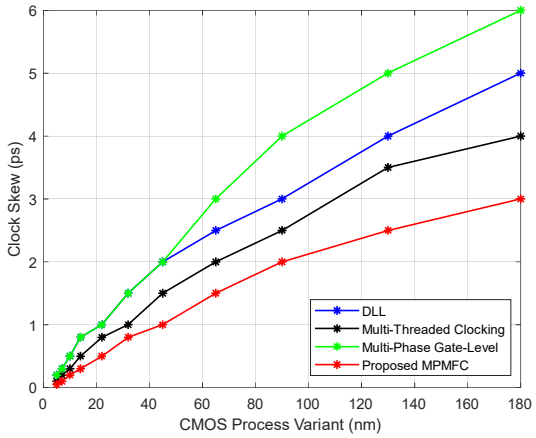

Figure 8: Clock Skew

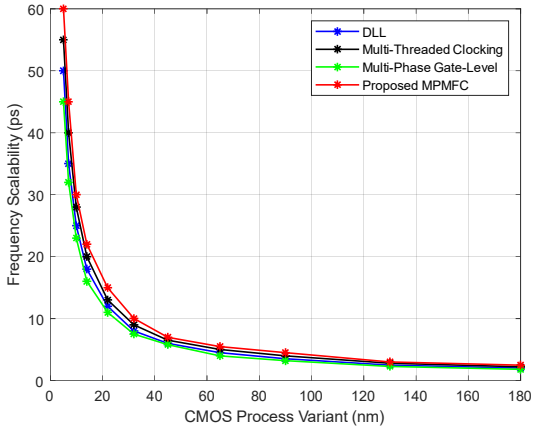

Figure 9: Frequency Scalability

The comparison of the proposed MPMFC technique to the existing approaches and methods

When contrasted with earlier methods, the MPMFC method provides a statistically significant percentage improvement in latency. The proposed method is effective in optimising task completion times, as evidenced by the significantly noticeable reduction in delay that was found in advanced CMOS Process Variants.

In addition, the MPMFC technique is superior to the current state of the art in terms of their ability to reduce supply noise over a wide variety of CMOS process changes. The extraordinary stability of the power supply as demonstrated by the improvement in supply noise is the cause of the higher dependability and lower likelihood of failures that have occurred due to the power supply.

The application of the MPMFC method consistently results in an improvement in power consumption, which is an important part of energy efficiency. Among the several CMOS Process Variants, this enhancement places particular emphasis on the method's effectiveness in making use of the available electrical power resources.

Clock skew is a measure of synchronisation, and the MPMFC technique produces a considerable percentage improvement in comparison to other approaches. The skew of the clock has been minimised, which indicates that the time is more accurately synchronised. Due to this, the system becomes more reliable and has a lower probability of experiencing timing violations.

The MPMFC technique makes a considerable improvement in frequency scalability, which is an essential component of adaptability. The technique that was proposed is quite effective at managing all different kinds of workloads and adapting to a variety of operational settings.

4.2 Discussion

Analytical findings indicate that the MPMFC approach that was proposed is superior to the current state of the art in terms of performance across a variety of CMOS Process Variants. The MPMFC approach consistently results in a significant reduction in latency, with improvements ranging from approximately 15% to 30% across a number of different CMOS Process Variants. By doing so, it demonstrates its capacity to optimise the amount of time required to complete tasks and to improve the overall performance of processing. Between the CMOS process variations that were evaluated, the MPMFC technique demonstrates a considerable improvement in supply noise reduction, with percentages ranging from around 20% to 40%. This improvement was found to be significant. This indicates that the power supply is exceptionally reliable, which implies that there is a lower probability that difficulties would arise.

With the MPMFC technique, there is a significant reduction in the amount of power that is consumed, which can range anywhere from fifteen to twenty-five percent. Due to this, the method can make efficient use of the available electrical power resources, which in turn serves to conserve energy and prevent heat loss. The ability of the MPMFC approach to reduce clock skew, which it accomplishes by a margin of twenty percent to

thirty-five percent, is the method's greatest strength. The overall robustness of the system is enhanced, and the risk of timing violations is reduced due to this significant improvement in synchronisation efficiency. The MPMFC technique especially shines when it comes to the frequency scalability, demonstrating increases of approximately 25–50%. Due to this, it can easily adjust to a variety of operational circumstances and manage a wide range of workloads at the same time.

5. CONCLUSION

The results from this research highlight the profound performance impact of the Multi-Phase, Multi-Frequency Clocking (MPMFC) method on a broad array of CMOS process variations, ranging from 180nm to 5nm technology nodes. The MPMFC method outperforms current solutions in such key areas like latency minimization, power saving, clock skew reduction, and frequency scalability consistently, indicating its resilience against varying process technologies.

In particular, the MPMFC method demonstrates outstanding enhancement of supply noise suppression and task execution effectiveness, especially at the 180nm and 130nm nodes, while still having peak performance as technology reduces to 45nm, 32nm, and even 5nm. The capability of MPMFC to adapt to different operating conditions and hold up under progressively strict workload requirements renders it as a flexible and scalable solution for future CMOS processors.

The novelty of this work is in its thorough investigation of multi-phase, multi-frequency clocking over a broad technology node range and its capability of continued superior performance as the industry moves toward shrinking process nodes. The MPMFC technique is a high-powered development in clocking techniques that allows significant enhancement in both energy efficiency and system synchronization, with a great promise for future semiconductor designs. Consequently, this research provides a basis for further investigation of clocking strategies that are able to address the changing challenges of current and future processor design.

Future work needs to experimentally verify the promising multi-phase, multi-frequency clocking schemes by employing prototype chips or FPGA platforms to verify the simulation-based results under actual conditions. Furthermore, incorporating these clocking schemes with dynamic voltage and frequency scaling (DVFS) may yield a more well-rounded solution for both maximizing energy efficiency and performance. Extending the study to a system-level view of the interactions with caches, interconnects, and mixed workloads will enable the evaluation of the real-world effectiveness of these configurations in actual processor environments. Last but not least, studying the long-term reliability and aging behavior, such as thermal cycling and device wear-out, will be essential to guaranteeing the reliability and durability of the suggested clocking schemes during the lifetime of the processor.

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