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HIGHLY RELIABLE ULTRA-LOW POWER AND LATENCY OPTIMISED FIN-FET BASED 9T SRAM

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ABSTRACT

The limitations of CMOS at smaller scales have increased the demand for alternate nano-devices. There are a number of suggested devices, including FinFET, TFET, and CNTFET. FinFET stands out as a promising device that has the potential to replace CMOS due to its low leakage in the nano meter range. Today data storage very much important in daily life. So, for this we required sophisticated electronic devices for storage purpose. So, we have to design basic SRAM Cell because of SRAM has less static Power compared to DRAM. To strike a better balance between the improved transistor circuit design and the increased storage capacity required by modern electronics, a new technology known as FinFET has been created. The loss of gate control over the channel causes many problems for CMOS devices, including higher production costs, higher ON current, short channel effects (SCEs), lower reliability and yield, higher leakage currents, and so on. This idea proposes a unique FinFET based 9T SRAM cell that uses a single ended bit-line design for near-threshold read/write operations. This eliminates the need for a boosted power supply and writes aid circuitry. As well as improving write-ability, write power, and write time, turning off both M4 and M5 transistors in write mode also removes write and read limits on the size of the semiconductor device. By using a transmission gate with a low threshold voltage (Vt) as the access transistor, both write-ability and write-time were dramatically enhanced.

Keywords: *System-on-chip, read static noise margin, write access time, leakage power, Carbon Nano Tubes, 9TSRAM*

1. INTRODUCTION

The current trend in consumer electronics is toward ever-smaller form factors. The current market trend Favors tiny and portable products. CMOS is used in nearly every electronic device, and advances in CMOS scaling have made miniaturization a reality. These days, every single one of the smart devices available is incredibly portable. There are many different kinds of circuits inside these devices, but the processor and memory are present in every single one. When we consider a portable gadget, we can see that it seems sense that storage space would be limited. Because of this need for lightning-fast performance, SRAM and similar memory have become standard. While miniaturization of CMOS has made scaling possible, it has also introduced new challenges, such as those related to the devices' power consumption and reliability. SRAM Memories' performance matrix includes the dimensions "power" and "stability," both of which are crucial. High power consumption, leakage current, stability, process fluctuations, etc. are just some of the problems that have been identified and addressed by the scientists.

One of the main worries was that the scaling down of device size would reduce the threshold voltage of CMOS devices, yet this drop in supply voltage was necessary. One such solution is subthreshold operation [1], in which the device is put into function at a voltage lower than its threshold; however, it has been shown to negatively impact the stability of 6T SRAMs. Other variants of the SRAM cell, such as the 7T, 8T, 9T, and 10T SRAM cell, were developed to replace the standard 6T SRAM cell in order to improve stability criteria and cut power consumption. The relevance of data storage in modern society is growing rapidly. Memory is essential for lowering the power consumption of any electronic or digital device. For better system performance and efficiency as a whole, "more data in less space" is a valuable concept to keep in mind. The acronym "SRAM" refers to the semiconductor memory that we typically utilised. The term "Static Random Access

Memory" is an abbreviation. SRAM memory's high store capacity and quick access time make it a viable option for many VLSI chips. Whereas the term "static" implies that it does not require frequent updating, DRAM does. Both of these storage options belong to the RAM (Random Access Memory) category. In this study, we examine the difference between 7-transistor SRAM and 6-transistor SRAM in terms of power consumption. Because of this, 7 transistors have higher power dissipation than 6 transistors.

6T SRAM has a power dissipation of roughly 2.991mW, while 7T SRAM dissipates about 3. 183Mw.The portability and low power consumption of SRAM make it a popular choice for usage in portable devices. In this work, we use DSCH to design the schematics of 6T SRAM, 7T SRAM, 8T SRAM, 9T SRAM, and 10T SRAM, and MICROWIND to design the layouts. In the past, semiconductor manufacturers relied almost exclusively on silicon-based fi eld effect transistors (FETs). However, as the transistor size enters the nanometer regime, silicon-based transistors face many challenges. The gate losing control of the channel, excessive power consumption even when doing nothing, difficulties in choosing a proper oxide material, an inability to diminish oxide thickness appropriately, and other short channel effects (SCEs) are all examples of such issues. The VLSI (Very Large-Scale Integration) method has been the standard integration approach for many years. The phrase "Very Large-Scale Integration" (VLSI) describes the method by which an IC (Integrated Circuit) is created by packing millions of transistors onto a single chip. New, cutting-edge technologies have emerged as a result of developments in VLSI, speeding up circuits and reducing design limitations. Miniaturization has become the norm for electronic devices. These days, every new Smart Gadget (SG) is miniaturized for easy portability. Memory and processing circuits are ubiquitous in such devices. Memory is becoming increasingly important in modern designs. In current technology, memory takes up more than 85–90% of the chip area. SRAM and DRAM, two types of memory, significantly improve SSD (Solid State Drives) performance. However, faster and more dependable memory is required for a variety of integrated devices. For VLSI applications, SRAM [1-2] is crucial because it provides both low power consumption and great performance. Reliability issues such leakage, process variations, and SCEs arise as a result of the rapid growth of CMOS [3] design. However, CMOS scaling [5-6] introduced process variations that negatively affected SRAM despite its superior speed, reliability, and low power consumption. The scaling of dimensions is made feasible by the miniaturization of CMOS, but this in turn causes problems with stability and power consumption. The fundamental issue with CMOS devices is that threshold voltage also scales as supply voltage is increased. Moore's law has allowed CMOS scaling to become a nano-scale system [7]. This has necessitated the development of CMOS substitutes such FinFETs [8, 9], TFETs (Tunnel FETs) [10], and CNTs (Carbon Nano Tubes) [11, 12]. Because of its many advantages over CMOS, FinFET technology [11, 12] has been chosen as the successor. In order to reduce the amount of power that is wasted as heat, many low-power approaches can be employed. These include variable threshold CMOS (VTCMOS), multi-threshold CMOS (MTCMOS), self-controllable voltage level (SVL), stacking, and power gating. At first, conventional CMOS design techniques are used to create SRAM. However, this still results in problems, such as increased leakage current and power dissipation, which diminish SRAM performance. The memory must have low power consumption, fast access time, and low leakage current. For this reason, FINFET-based SRAM cells should be used instead of CMOS-based SRAM cells [13]. When compared to CMOS-based design architectures, FinFET design significantly decreases SCEs [14]. It is also important to reduce the leakage characteristics of SRAM cells in order to boost cell stability [15].

1.1 FinFET Technology

FinFET technology is one of the most practical types of FET available now. To put it another way, this expedites the analog and digital execution and simulation of transistor applications. FinFET's small size, strong performance, low production costs, and low power consumption make it a promising technology for application in nanoelectronics of the future. FinFETs can be used to replace the bulkCMOS transistors. Because of its low leakage current or standby power, this technology is a viable alternative for the development of memory subsystems [20]. In Fig. 1, we see a schematic depiction of FinFET. The many perpendicular channels in a FinFET structure are meant to evoke the 'Fin' of a fish, hence the name. It is a substrate-based multi-gate device (MGD) with a different name. A double gate configuration results when the gate is placed on two, three, or all four sides of the channel. In silicon, the 'Fin' is produced by the source or drain area. Multi-gate transistor is another name for FinFET. The FinFET model encompasses the subsequent areas: Oxide

gate (SiO2) area Concentrations of highly doped poly-silicon Fin made of low-doping silicon The source-drain interface is highly doped.

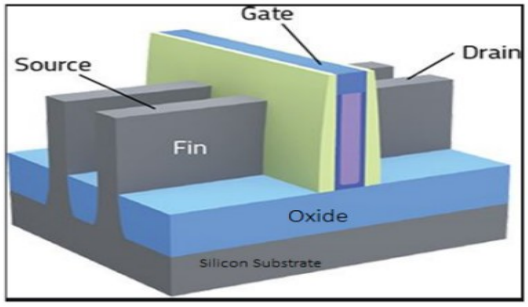

Figure 1: Structure of FinFET

1.2 SRAM Memory

Data stored in static RAM remains unchanged until the memory is powered. In SRAM, periodic refreshing is not required. The data is lost if the device is unplugged since it is volatile. Each bit is stored in SRAM using bi-stable latching circuitry. SRAM is a type of random-access memory that has several applications. The components of an SRAM array are as follows: Lines for bits, sense, words, rows, columns, and storage. Words are collected from a large pool of candidates in a single row. Each address contains both a row and a column. A single memory row can be accessed using the row address, whereas a single memory column can be selected via the column address. The storage cell, also known as a bit-cell or 1-bit memory cell, consists of a latch circuit that can be set to either of two different primary states. The information in the storage cell takes the form of logical ones and zeros. A single SRAM cell can operate in one of three distinct states. Put on hold or standby (idle circuit). Data Request (Please Read) Update the content by writing. Two identical inverters cross-coupled and wired in series make comprise a single SRAM memory cell, along with two access transistors [23]. To perform a read or write operation, a word line (WL) must be employed, which activates the access transistors that link a cell's columns of complementary bit lines (BL). This circuit topology has a number of benefits, including low static power dissipation (SPD), moderate energy consumption, low leakage current, and quick data access.

1.3 Existing Method

The 9T memory cell shown in Figure 2 is now in use. Two inverters are connected in a cross configuration using pass transistors. The bitline complement is connected to both inputs of the access pass transistor. In order for data to be written into the memory cell and read out via the BL or BLB (bitlines), the gates of access pass transistors TN3 and TN4 must be linked to the WL (word line).

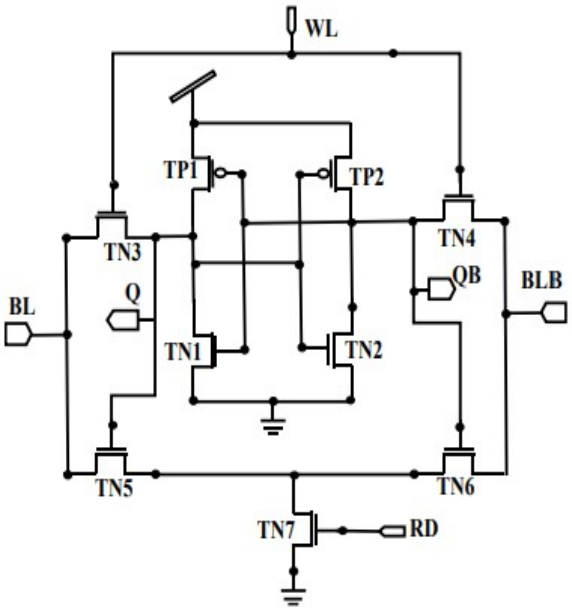

Figure 2: 9T of SRAM cell

The 9T SRAM in Action Numerous studies have been conducted on the 9T SRAM cell, focusing on its many performance factors. Based on CMOS technology, many different types of SRAM (6T, 7T, 8T, 9T, 10T, and 12T) have previously been designed. The 9T SRAM cell is the primary subject of this paper due to its superior performance in terms of excluding area. The 9T SRAM cell consists of a bottom and an upper sub-circuit. As can be seen in figure 1, the upper subcircuitry of a 6T SRAM cell in a small-sized device consists of TP1, TP2, NM1, NM2, NM3, and NM4, whereas the lower subcircuitry consists primarily of TN5, TN6, and TN7. The 9T SRAM cell uses five transistors for the access pass transistor. The data in the upper sub-circuitry is controlled by a write signal (W), which acts on two access pass transistors (TN3 and TN4). The 6T SRAM cell's lower sub-circuitry now includes three access pass transistors: TN5, TN6, and TN7, all of which are used for the bit line's write operation. Information stored in nodes Q and QB can be retrieved using access pass transistors TN3 and TN4. The 9T SRAM proposed by Singh et al. [9] was compared to the 45nm SRAM design that is currently in use. The group settled on a PDP raise of 36%. Separate hardware modules control the SRAM's read and write operations. The read word line (RWL) controls the flow of the read process. Column-

based write word-lines (WWL) are controlled by the NM3 and NM4 access pass transistors. The two-stacked read port is enabled by the row-based high RWL and GND if QB = '1', which discharges the RBL and causes the sense amplifier to detect Q = '0'. For the number 1, you must reverse the procedure. RBL receives a minimal precharge of 0 V from the VDD and WWL. The cross-coupled inverter is cut off from the external connector when WWL, WBL, and WBLB are all held LOW and the latch has no intrusive effect [10]. The cross-coupled inverter's data determines how long RBL can stay at VDD after being discharged. As a result, the reading stack served as a middleman in the process of retrieving data from the latch. By maintaining RWL at a LOW level when asserting WWL, the read circuitry is disabled and the writing process can proceed. As soon as the WWL is asserted, the data is loaded via the WBL and WBLB, and precharging begins to initiate the write process. Once the WWL signal has been asserted, the access pass transistors NM3 and NM4 have been turned on, and the cell's word bit line is ready for reading or writing data. Therefore, information is deposited into the cell at its proper nodes.

2. RELATED WORKS

Researchers have proposed numerous methods for constructing SRAM cells. In this section, we take a quick look at a handful of significant Static RAM cell designs and provide our thoughts on them. Small power Static RAM with BL accuse recycling for read/write operations was presented by Byung-Do Yang [5]. The proposed SRAM design relied on the BL charge recycling mechanism and the hierarchical BL architecture. The proposed technology decreased SNM deterioration by 17% and cut read and write power usage by 84%. Besides, 145MHz isn't enough for operational speed. W. Kang et al. [9] presented a Magnetic Tunnel Junction-based non-volatile SRAM proposal. The MTJ device's MAP was created by them. Better results in terms of accumulated power, latency, and dependability disquiet were achieved by employing switching strategies. The system's primary flaw is that it requires a higher amount of switching power to operate. The first TFET-based 8T SRAM cell was developed by A. Makosiejet al. [10]. The 8T SRAM cell has no architectural limitation due to the half-selection problem that prevents it from working in any mode at 1V supply voltage. The layout of the cells allows for the utilization of lengthy word lines with bit interleaving. The main downside of the Static-RAM design is that significant leakage power develops anytime the supply voltage increases. A massive presentation, voltage scaling of 162 Mb Static RAM range was proposed by E. Karl et al. [11] and implemented in 22nanom eter tri-gate bulkiness hardware. High-Density Cells (H-DCs) measuring 0.092 m and Low Voltage Cells (LVCs) measuring 0.108 m were both produced using 22 nm tri-gate technologies. This is the primary handicap of the really high. [23] Using the 18nm cds_ff_mpt process design kit, Cadence Virtuoso was used to compare traditional 6T, 7T, and 8T SRAM cells. Many difficulties, including the short channel effect and manufacturing variability, beset CMOS as it moves towards the nanoscale realm. [24] Using SG and LP-IG mode, we analyzed 8T FinFET SRAM for leakage power and stability concerns. To improve the reliability and efficiency of the circuit, the LP-IG mode is implemented.

In this paper, Alireza Abbasi (2022) proposes a non-volatile static random-access memory (NVSRAM) based on a pair of six-FinFET memcapacitors (6T2MC). The two memcapacitors in this configuration serve as a form of non-volatile memory. The suggested cell is resistant to power-off data loss and provides vastly enhanced read/write operations over earlier NVSRAMs. Read and write operations at specific nanometric feature sizes are used to gauge the new NVSRAM design's performance. The planned 6T2MC cell is also compared to the 8T2R cell, the 8T1R cell, the 7T1R cell, and the 7T2R cell. The results reveal that when comparing 6T2MC to 7T1R and 7T2R cells, 6T2MC has a shorter write delay (5.50%) and a shorter read latency (98.35%). When compared to 7T2R and 7T1R cells, the 6T2MC cell has significantly reduced power consumption (38.86%) and leakage power (23.80%). Power use, data read/write delay, and system noise margin are only few of the crucial cell metrics that have been vastly enhanced. The proposed design is greatly enhanced by the use of FinFET and memcapacitors due to the former's superior properties over MOSFET.

Recently designed integrated circuits (ICs) in Deep sub micron technology (DSM) have required less energy to run because of the rapid expansion of the semiconductor industry. As transistor technology continues to shrink in size, digital circuit performance has been steadily improving. However, the short channel effect (SCE) and the drain induced barrier lowering effects (DIBL) have emerged as major obstacles due to the miniaturization of electronic circuits. A 9T SRAM cell is proposed and compared to the other (N) T SRAM cells in this study by Sharma,

Nidhi (2016), which uses FinFET technology for SRAM cells of various topologies. The suggested circuit reduces the dynamic power consumption of a 10T SRAM by as much as 82.21% and the leakage power consumption by as much as 61.35% at 25°C and 45.13% at 110°C. For consistent comparisons, we run our simulations in HSPICE at 32nm with V DD =0.8V.

The key design considerations for embedded cache memory are speed, power consumption, noise tolerance, and reliability. It is difficult to design an SRAM cell that can function on low supply voltages because of variations in process, voltage, and temperature. The traditional 6T SRAM cell is unstable and prone to read/write errors at scaled technology nodes. Due to its lack of bit-interleaving design, it is also vulnerable to multibit soft error rate. A low-power, resilient single-bitline 9T SRAM is presented by Chandramauleshwar Roy (2021) using a 16 nm technology node in the subthreshold region. The effectiveness of the proposed cell is shown by comparison with other recently released SRAM cells, such as the single-ended NTV 9T (SENTV9T), the write and read enhanced 9T (WREN9T), and the conventional 6T (CONV6T). When compared to WREN9T/SENTV9T, the proposed cell exhibits 1.25/1.96% lower read current IREAD variability. The proposed cell has a 4.23-point improvement in noise over CONV6T thanks to its read decoupled operation.

In order to combat sophisticated process variation and provide support for ultra-low power operation, stationary random-access memory (SRAM) is undergoing a period of expansion. More than 80% of the area of modern microdevices is taken up by memories, and this trend is only projected to grow. Leakage current (Ileakage) is greater with lower collision strategies in metal oxide semiconductor field effect transistors (MOSFETs) because of these challenges. Due to its superior stability, the fin field effect transistor (FinFET) can be used as a viable alternative to CMOS in the 45 nm variant. The memory cells play a crucial role in the distributed computing system. The most popular memory is static random-access memory (SRAM), which is estimated to take up more than 60% of the total space of the chip. M. V. Nageswara Rao (2023) proposes a FinFET-based 16 nm-knot SRAM cell. The enhanced cell has reduced power leakage and reduced current leakage in addition to faster read access times. When comparing the proposed FinFET-based 10T SRAM to devices based on MOSEFET technology, the proposed device achieves 80.80% lower PDP in write mode and 50.65% lower PDP in read mode. SNM is up by 22.20 percentage points and Ileakage is down by 25.53 percentage points.

Power consumption and data processing speed of integrated circuits (ICs) are becoming increasingly important for many emerging applications of artificial intelligence (AI), including driverless vehicles and the Internet of Things (IoT). Modern SRAM architectures are able to provide both high throughput and high accuracy for AI processing. Unfortunately, in order to store sophisticated AI models, these SRAMs have to use a lot of energy and take up a lot of room. To circumvent the power and throughput issues in AI computation for autonomous vehicles, Kim Y (2021) presents ground-breaking ultra-low power and high-throughput 8T SRAMs by utilizing the electrical performance of CNFET and FinFET devices. Our proposed P-Latch N-Access (PLNA) 8T SRAM structure and single-ended (SE) 8T SRAM structure provide substantial enhancements in power consumption and throughput in comparison to the existing state-of-the-art 8T SRAM designs. When designing SRAM circuits with FinFETs or CNFETs, more tubes and fins means faster operation. However, the increased surface area and power requirements may result from the extensive use of tubes and fins. In order to maximize available space, the authors have reduced the number of tubes and fins without sacrificing the performance of the memory circuit. First and foremost, the stacking of devices in the reading part of our new SRAMs cell allows for better low-power operation, improved readability and writability, and a greater pull-up ratio without sacrificing read Static Noise Margin (SNM). Even greater delay and power performance is displayed by the suggested 8T SRAMs when a collaborative voltage sensor amplifier and independent read component are incorporated. Writing power consumption is reduced by 96% in the proposed PLNA 8T SRAM and by roughly 99% in the proposed SE 8T SRAM as compared to the current state-of-the-art 8T SRAM in the FinFET model, and by 98% in the CNFET model.

To comprehend the potential future performance of VLSI circuits, it is necessary to be able to predict variability tolerance. In this investigation, we use the cadence virtuoso software to analyze the effects of PVT fluctuations on a variety of FinFET circuits. 7 nm FinFET-based circuits' sensitivity to variations in voltage and temperature is studied. This method is based on the hypothesis that power dissipation and delay can be optimized by raising operating temperature and power input. FinFET

files at the 7 nm technology node are simulated using a wide range of domino logic by employing a multi-gate prediction model. The set-reset logic circuit and high-speed cascade circuit technique proposed here outperforms state-of-the-art methods such as the mirror-footed domino, high-speed clocked delay, and modified high-speed clocked delay in terms of power consumption and delay over a wide range of operating temperatures and power input levels. Monte Carlo simulation allows us to calculate the mean and standard deviation of performance for the set-reset logic circuit and high-speed cascade circuit that we propose. To mitigate the delay introduced by an increase in temperature and reduce the supply voltage from 0.7 V to 0.3 V, the suggested circuit is simulated using FinFET technology. When compared to standard practices, the proposed approach cuts power consumption by as much as possible. The proposed methods significantly decrease both the delay and footprint of the current system.

Microprocessors' cache memories are built around static random-access memory (SRAM) cells. Their efficiency is crucial because they are a part of the core processing unit. Because only 10–15% of a modern SoC's transistors are devoted to logic and the rest are used for cache memory, performance requirements continue to rise. In addition, AI-reliant implantable, portable, and wearable electronics necessitate an effective and trustworthy SRAM design for compute-in-memory (CIM). In modern technological nodes, reliability is of paramount importance for reaching performance benchmarks. In particular, the low supply voltages used by battery-powered applications pose a threat to the reliability of SRAM cells. The transistor's off-state current is rapidly catching up to its on-state counterpart in modern devices. However, design integrity can be compromised due to manufacturing differences that alter transistor design parameters. The integrity of the SRAM cell is further compromised by the handling of sensitive data, adverse environmental factors, and charge emission from IC packaging materials. FinFET-SRAMs, due to their aggressive scaling, are operating near the limit, where even a small deviation can result in a catastrophic failure. Gul W. (2022) organizes the problems with SRAM cell design into five groups and then provides a thorough examination of the most pressing ones. The mathematical foundations and workable solutions are explained for each class.

SRAM is a type of memory that can store information indefinitely without needing to be refreshed. When compared to DRAM (Dynamic Random Access Memory), which must have its stored data refreshed at regular intervals. Each bit of information in Static RAM is stored in a flip-flop circuit, while in Dynamic RAM it is stored in a capacitor. However, capacitors gradually lose their charge and must be recharged over time. As a result, SRAM outperforms DRAM and is more stable than DRAM even when not in use. In this study, Venkataiah C (2023) compared the write and read delays, PDP, and Static Noise Margin (SNM) of SRAM cells constructed with various field effect transistors. The CNT-based SRAM cell with optimal values for CNT density, CNT diameter, and CNTFET flat band voltage outperforms and outlasts competing device technologies in terms of performance and stability. The write and read latency of an optimized CNTFET SRAM cell are 85.8 and 94.3 percent better than those of a MOSFET based SRAM, respectively. The HSPICE tool has been used for all simulations, with a 32nm technology node.

3. PROPOSED METHOD

A. Fin-Fet 9T SRAM

Figure 3 depicts the purported 9T SRAM cell. For 9T SRAM cell design and simulation, the Sub-18 nm HP and low standby power FinFET PTM is used. This idea is an enhanced form of the 8T SRAM cell that was developed before [5]. The bit cell's structural stability in the near-threshold region is investigated, and its resistance to process, voltage, and temperature variations is fine-tuned. Asymmetric cross-connection of inverter pairs is proposed for the 9T SRAM bit cell. There are two FinFET transistors (M1-M2) in the left face inverter and four (M3-M4-M5-M6) on the right. An access transistor with a low Vt (LVT) transmission gate is used to boost the bit cell's write margin and write time. In addition, the dual threshold technique is used to simultaneously improve performance while reducing power consumption. Transistors M4, M5, M7, and M8 have two fins, as shown in Table 1, to boost driving strength, while Transistors M1, M2, M3, M6, and M9 have only one fin, as shown in Table 1. It is clear from Table 2 that the suggested bit cell makes effective use of both high and low threshold transistors to simultaneously achieve high performance and low power consumption.

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Table 1. SRAM cell transistor dimensions that have been reported

Bit- Cell Design	Access FinFET (No. of Fins)	Pull-up FinFET (No. of Fins)	Pull-down FinFET (No. of Fins)	Feedback Cutting FinFET (No. of Fins)	Read transistor (No. of Fins)
6T	M5=M6=1	M3=1, M4=1	M1=1, M2=1	–	–
7T	M4=1, M7=1	M3=1, M5=1	M1=1, M6=1	–	M2=1
8T	M7=2	M8=1, M1=1	M5=M4=1	M2=M6=2	M3=1
9T	M7=M8=2	M3=M1=1	M2=M6=1	M4=M5=2	M9=1

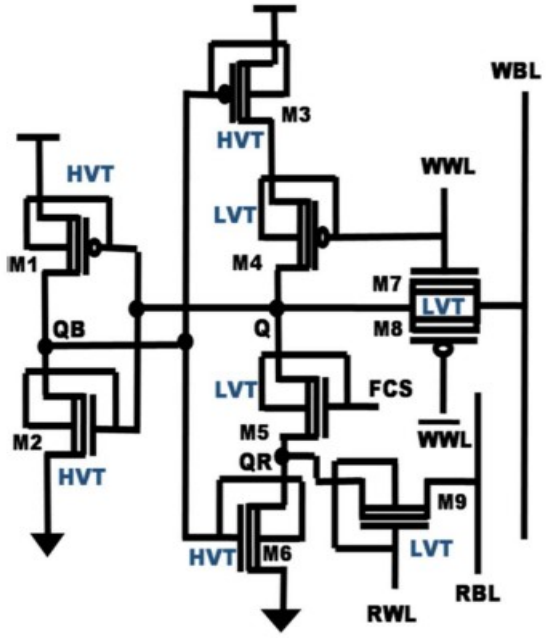

Figure 3: Proposed 9T SRAM cell architecture

B. Cell Functionality

As can be seen in Fig. 3, the proposed 9T SRAM cell employs an asymmetric cross-connected inverter pair to facilitate data storage at node Q. Each read and write operation makes use of a single read bit line (RBL) and a single write bit line (WBL). To facilitate reading, writing, and holding, the right inverter features two FinFET transistors (M4 and M5). The FCS, the write word line, and the read word line all function whether the state is "hold," "write," or "read." Table 3 provides a comprehensive summary of the control signals required for all modes of operation of the proposed FinFET based SRAM cell.

Table 2. Representation of both High Vt and Low Vt FinFETs in reported SRAM cells.

Bit-Cell Design	Access FinFET	Pull-up FinFET	Pull-down FinFET	Feedback Cutting FinFET	Read FinFET
6T	M5=M6=LVT	M3=LVT, M4=LVT	M1=HVT, M2=HVT	–	–
7T	M4=LVT, M7=LVT	M3=LVT, M5=LVT	M1=LVT, M6=HVT	–	M2=LVT
8T	M7=LVT	M8=HVT, M1=HVT	M5=HVT, M4=HVT	M2=LVT, M6=LVT	M3=LVT
9T	M7=LVT, M8=LVT	M3=HVT, M1=HVT	M2=HVT, M6=HVT	M4=LVT, M5=LVT	M9=LVT

C. Write Operation with Feedback Loop-Cutting

To enhance the write margin and write access time, a single ended bit-line design is used instead of an NMOS transistor. This configuration makes use of a low Vt transmission gate. When the write word line (WWL) is active and the feedback control signal (FCS) is at a low level, the voltage from the write bit line (WBL) is delivered through the transmission gate to the stored node Q, as illustrated in Fig. 7. The suggested approach uses FinFETs (M4 and M5) to revolutionize data writing in the sub-threshold operating domain by breaking the feedback closed loop topology of a cross-

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connected inverter pair (invL and invR). The writability of the proposed cell is much improved by switching out the NMOS access transistor for a transmission gate [28-30]. It has been demonstrated and researched that the cell's write characteristics are enhanced by the addition of a transmission gate. Assume that after one write cycle, node Q in the data storage system has the value 0. It then needs to switch to the high 1. The traditional 6T bit cell's write cycle activation is also when the pass transistor's strength is at its highest (VGS-VPASS= VWWL).

Table 3. Proposed 9-bit SRAM truth table.

	Hold	Write-1	Write-0	Read
WWL	'0'	'1'	'1'	'0'
WBL	'0'	'1'	'0'	'0'
RWL	'0'	'0'	'0'	'1'
RBL	'1'	'1'	'1'	'1'
FCS	'1'	'0'	'0'	'0'

As soon as the voltage at node Q = 0 rises, V(GS-PASS) falls. As a result, when VQ=VWWL-V(T-PASS), the pass transistor's strength drops and it enters a cutoff condition. One of the FinFETs maintains full conductivity in the write state after the pass transistor has been replaced by a transmission gate based on FinFET technology.

4. RESULTS

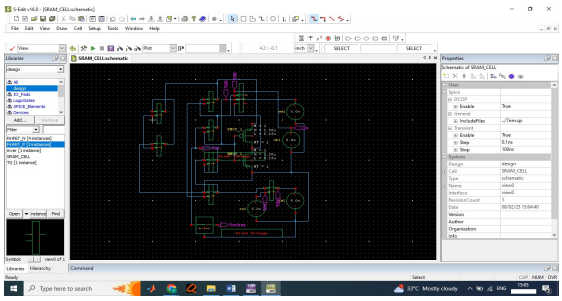

Figure 4: Proposed SRAM design

Above screenshot taken in Tanner EDA16.0 represents proposed FinFET based SRAM design using 9T SRAM with 7nm technology.

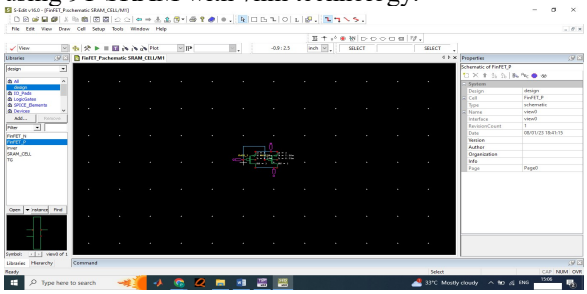

Figure 5: Proposed FinFET design

Above figure shows FinFET internal architecture with two gate PMOS

Figure 6: Storing '0'

Above result shows proposed 9T SRAM '0' storing graph.

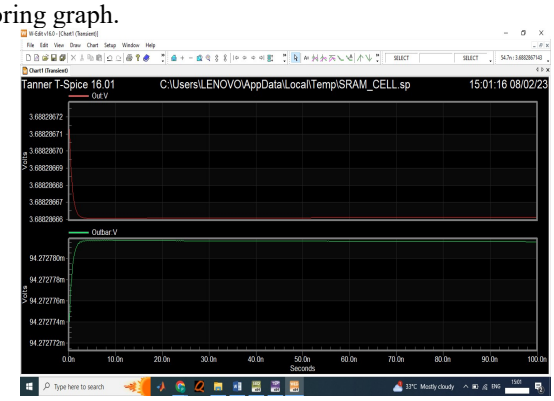

Figure 7: Storing '1'

Above result shows proposed 9T SRAM '1' storing graph.

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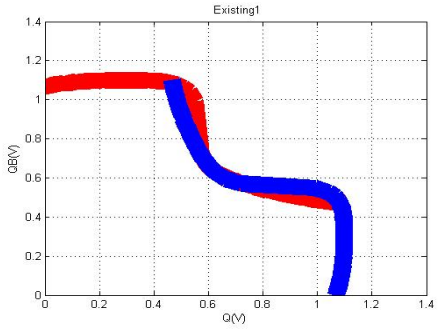

Figure 8: SNM for Existing method1

Above Graph represents existing SNM with unstable write read performance.

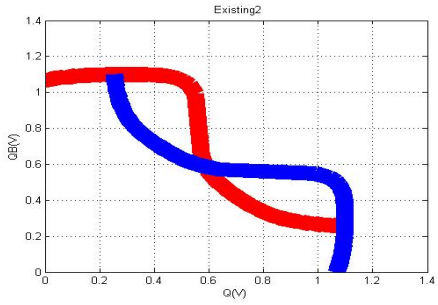

Figure 9: SNM for Existing method2

Above Graph represents second existing SNM with unstable write read performance.

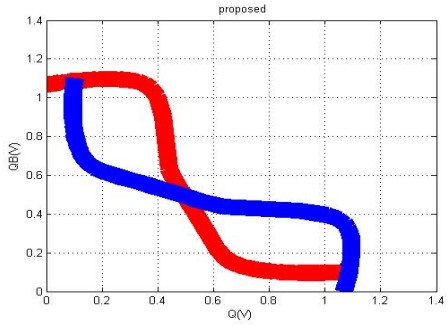

Figure 10: SNM for Proposed method

Above Graph represents proposed SNM with stable write read performance.

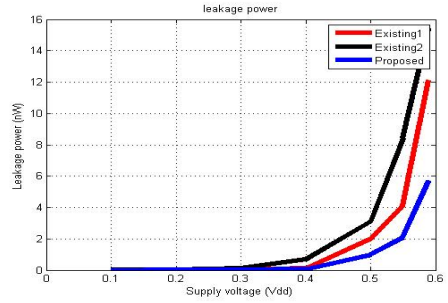

Figure 11: Leakage power comparison

Above Graph represents leakage power comparison of proposed and existing methods

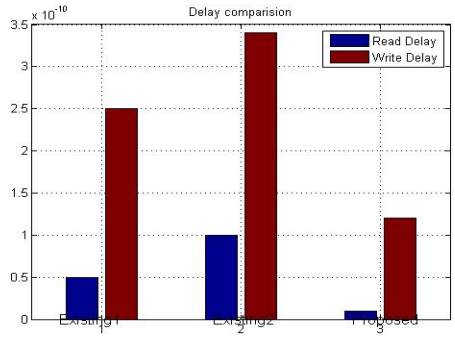

Figure 12: Latency comparison

Above Graph represents whole execution time delay comparison of proposed and existing methods.

5. CONCLUSION

The presented research demonstrates that FINFET is superior than CMOS SRAM cells in SRAM design due to its lower static power dissipation and latency. FinFETs have various benefits over bulk MOSFETs, including a simpler fabrication process (process flow) that is more akin to the traditional SOI CMOS process. FinFET, in comparison to other DG MOSFET topologies, offers a very high package density. Models of SRAM built with FinFET technology are offered to do away with SCEs. When compared to the standard MOSFET based SRAM cell, these simulations demonstrate a dramatic decrease in leakage current and power consumption. It is necessary to prioritise the intricacy and expense of their production.

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