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HIGH GAIN NARROW BAND SMALL SIGNAL HYBRID UNIT DARLINGTON PAIR AMPLIFIER

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ABSTRACT

Popularity of smart home gadgets gives rise to the demand for enhanced (wireless) RF power amplifiers. The global market of RF power amplifiers registered a CAGR of 3.2% between 2017 and 2021 and is expected to exhibit a growth of 15% from 2021 to 2032. The rising need of such RF amplifiers opens the path to a wide research in this field to fulfill the requirements. The Darlington pair amplifiers having high current gain still have the issue of poor response at higher frequencies, which can be removed by insertion of load at collector in the reference amplifier circuit to achieve higher voltage gain, power gain, bandwidth, slew rate and lower values of noise and harmonic distortion .A unique hybrid unit Darlington pair amplifier circuit with BJT-MOS is proposed in the present paper whose maximum voltage gain of 281.331, current gain of 33.698, bandwidth of 22.562 MHz, total harmonic distortion of $5.2*10^{-06}$ and slew rate of 106.389 V/m Sec and can operate on input signal in the range of 1mV – 10mV.The result shows that proposed amplifier has variety of applications may be used as pre amplifiers in VLF receivers, ultrasonic transmitters and, wireless communication, radio receivers, defense avionics, etc.

Keywords: *Darlington Amplifiers, MOSFET Amplifiers, Small–Signal Amplifiers, High Gain Amplifiers, High Frequency Amplifiers, Hybrid Configuration*

1. INTRODUCTION

There is a very wide array of amplifiers that functions across RF spectrum from a few MHz to the multi GHz range. Among all those amplifiers, the high gain RF power amplifiers, where the RF signal amplitude is minuscule and too low to be used directly , needs to be boosted so the overall SNR does not deteriorate as the signal passes through the rest of the circuit. The Darlington pair amplifiers which are high gain amplifiers are suitable candidate but with limitations of poor response problem at higher frequencies, limited voltage gain and power gain and smaller slew rate .It offers a little higher T.H.D .The objective of this work is to design a Darlington pair amplifier which is free from the problem of poor response at higher frequencies and also has high gain and lower T.H.D values. The modified hybrid Darlington pair proposed appears to be suitable to be used as high gain amplifiers in ULTRASONIC transmitters and receivers as shown in Fig.1.

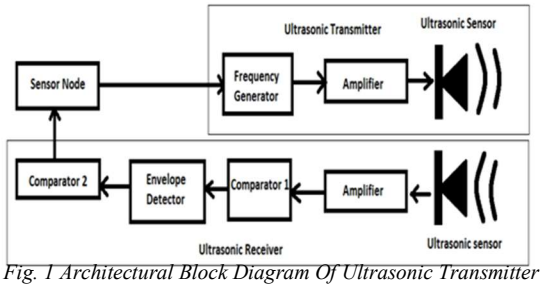

Fig. 1 Architectural Block Diagram Of Ultrasonic Transmitter And Receivers

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Moreover, variations in resistors R_A and R_E (Fig.3b) positioned at collector and emitter of BJT allows it to enter into a 700MHz frequency band. This range of frequency provides better network coverage due to low frequency and has the ability to penetrate buildings efficiently that lets the telephone companies offer better stable and faster connectivity in dense urban areas of Metro cities. Thus the proposed amplifier can be used as a drive amplifier in the wireless communication system .The block diagram of such wireless communication system with positions of proposed drive amplifiers is shown in Fig.2

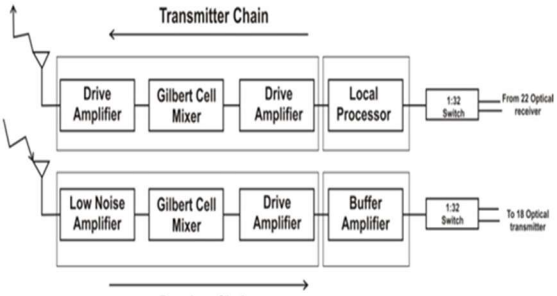

Fig. 2 Block Diagram Of Wireless Communication System

Since the proposed amplifier can work in the low frequency band it can cover distances up to 40 Kms which is far more than the high band, providing a benefit of lesser number of towers.

Darlington pairs are the ideal choice for the applications where high current gain and higher linearity are required **[1]**.Many small-signal amplifier circuits are proposed by researchers using Common Source MOSFETs in a Darlington pair configuration[**1,2**].Darlington configuration is a combination of two bipolar transistors with the emitter of one transistor is connected to the base of the other. The two collectors are associated together in such a way that the current amplified by the first transistor is again amplified by the second one. Present investigation includes hybrid topology in Darlington configuration which includes an NPN (BJT) at driver position and NMOS(MOSFET) [**10]** at follower position [**3,4**].The base of a Darlington transistor is sensitive enough to produce outputs for a few to tens of microamperes of input current from a switch or directly from TTL. But in a Darlington transistor since it is a combination of two transistors, it's base emitter voltage is twice than that of an individual transistor which comes in the range of 0.6V to 1.5V depending on the current driving through the transistor **[5-10]**.In the present circuit BJT is at the driving position because it has a low turn ON voltage whereas at the follower position MOSFET is used as it has very high input impedance due to the insulation layer and it consumes negligible energy in its operation as it has very low leakage current**[11]**. Also it has very high switching speed which reduces the slow response problem of Darlington pairs. BJT's are more commonly used in low current applications thus are beneficial as a driver in a small signal device whereas MOSFET's are ideal for high power applications which suits it's follower position **[5, 12-17].**

2. CIRCUIT DETAILS:

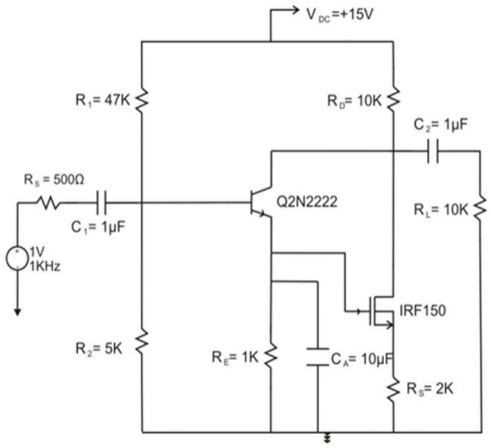

Fig.3 (A) Circuit Diagram For Reference Amplifier

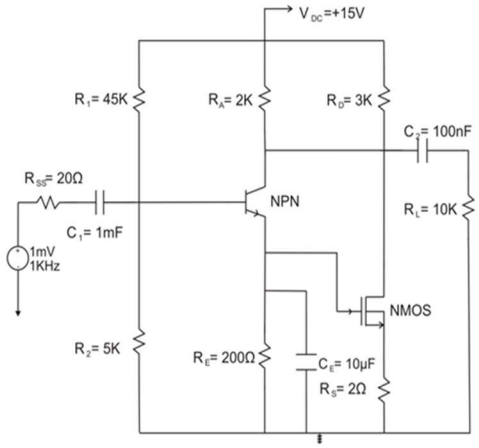

Fig.3 (B) Circuit Diagram For Proposed Amplifier

Present study is a comparison of the simulation of the hybrid unit of BJT and MOSFET in Darlington topology. The proposed amplifier is simulated in 180nm technology using Cadence

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Virtuoso and Spectre simulation. The circuit consists of an NPN (BJT) at driving position and MOSFET (nMOS) at follower position. BJT and MOSFET are attached to each other in Darlington topology with RC coupling and potential divider biasing. The required circuit diagram for reference and proposed amplifier are shown in Fig.3(a) and Fig.3(b) respectively. The additional resistance plays a vital role in amplifying the output as well as decreasing the amount of distortion in the circuit. Present investigation includes study of performance parameters with variation of various biasing elements, small-signal AC analysis, effect of temperature, determination of performing range for each parameter, and behavior of amplifiers under different conditions. The key merits of the proposed amplifiers are the elimination of the narrow bandwidth issue with reference amplifiers as well as the poor response issue with Darlington pair amplifiers at higher frequencies **[20]**. The components used in the reference and proposed amplifiers are listed below in Table-1.

Table-1 Component Details Of The Circuit:

Components	Reference Circuit	Proposed Circuit
Driving unit	Q2N2222	Npn
Follower unit	IRF150	nmos1
Rss (input sour resistance)	500	20Ω
R1 (biasing resistance)	47K	20K
R2 (biasing resistance)	5K	5K
R_A(additional resistance)	-	2K
R_E(emitter resistance)	1K	200Ω
R_D(drain resistance)	10K	3K
Rs (source resistance)	2K	2Ω
R_L(load resistance)	10K	10K
C1(coupling capacitor)	1µF	1µF
C2(coupling capacitor)	1µF	100nF
C_E(additional capacitance)	10µF	10u
V_{DC}(DC supply voltage)	15V	15V
AC source	1V-1KHz	1mv-1KHz

2.1 Circuital Parameter and Software Details:

In reference amplifier the BJT used is Q2N2222 which is a NPN and the MOSFET used is a power nMOS transistor IRF150 defined in P-Spice simulation software. Whereas the proposed amplifier uses nMOS transistors which are available at 180nm technology in Cadence Virtuoso and Spectre simulation **[3,4]** Table-3 shows the list of simulation parameters of used active devices in both the circuits.

Table-2 Simulation Parameters Of Bjt And Mosfet

Model Parameters	Reference Amplifier under P-Spice Simulation tool		Proposed Amplifier Under Cadence Virtuoso and Spectre Simulation	
	BJT	MOSFET	BJT	MOSFET
Model Name	Q2N2222	IRF150	Npn	nmos1
Cell Name	-	-	-	Nmos
Emitter Width	-	-	0.6	-
Area	-	-	0.36	-
Length(L)	-		-	180nm
Total Width(W)	-	2µm	-	2µm
Finger Width	-	0.3m	-	2µm
Threshold	-	-	-	800nm
S/D Metal Width(M)	-	-	-	400nm
Zero bias threshold voltage(VTO)	-	2.831	-	0.48
GAMMA (bulk threshold parameter)	-	0	-	0.666

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Kp (transconductance)	-	20.53E-06	-	0.490
PHI (surface potential)	-	0.6	-	0
IS(bulk p-n saturation current)	14.34E-15	1.94E-18	3.26E-16	NaN
CBD (bulk drain zero bias p-n capacitance)	-	3.229E-09	-	-
R_D (drain ohmic resistance)	-	1.031E-03	-	0
R_G (gate ohmic resistance)	-	13.89	-	-
R_{DS} (drain-source shunt resistance)	-	444.4E+03	-	-
CGSO (gate source overlap capacitance)	-	9.027E-09	-	370E-12
CGDO (gate drain overlap capacitance	-	1.67E-09	-	370E-12
BF (ideal maximum forward beta)	255.9	-	100	-
BR(ideal maximum reverse beta)	6.092	-	6	-
RC (collector ohmic resistance)	1	-	1	-
TF (ideal forward transit time)	411.10E-12	-	25E-12	-
TR (ideal reverse transit time)	46.91E-09	-	200E-12	-
CN (Base-Collector leakage emission coefficient)	2.42	-	2	-

3. OBSERVATIONS AND DISCUSSION

3.1. AC Analysis Of The Proposed Amplifier:

Performance parameters of the reference and proposed amplifiers at 180nm technology are recorded in Table-9 at room temperature with the help of Cadence virtuoso and Spectre simulation Fig.4 (a) and Fig.4 (b) show the frequency response curve for reference amplifier and proposed amplifier respectively.

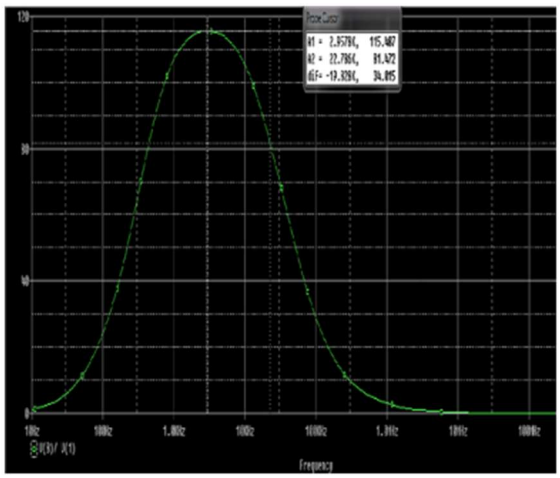

Fig. 4(A) Frequency Response Of Reference Amplifier

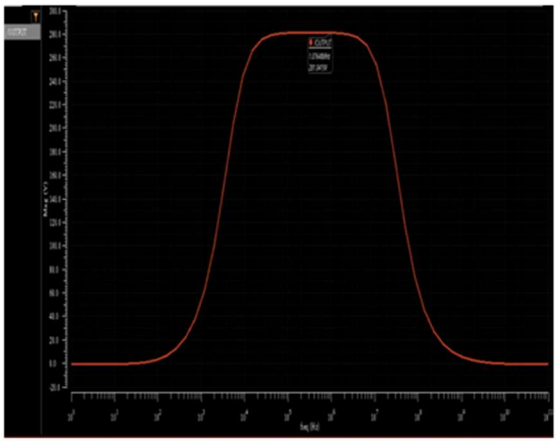

Fig. 4(B) Frequency Response Of Proposed Amplifier

On modifying the reference circuit simulation on P-Spice by an additional resistance R_A at the collector to V_{DC} and performing its simulation on Cadence virtuoso the power consumption and T.H.D of the proposed amplifier are significantly reduced.

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The proposed version is more acceptable as it has higher voltage gain, wider bandwidth, lower power consumption, low output referred noise at 1KHz frequency and greater stability than the reference amplifier It should also be noted that the observations taken for the proposed amplifier is recorded for 1V AC input signal source from which 1mV 1KHz signal is used for amplification purpose. Proposed amplifier emerges with high slew rate (rate of change of output voltage) which must be high in order to produce maximum undistorted output voltage swing **[21]**.

3.1.1. Mathematical Analysis of Hybrid Equivalent of Proposed Amplifier

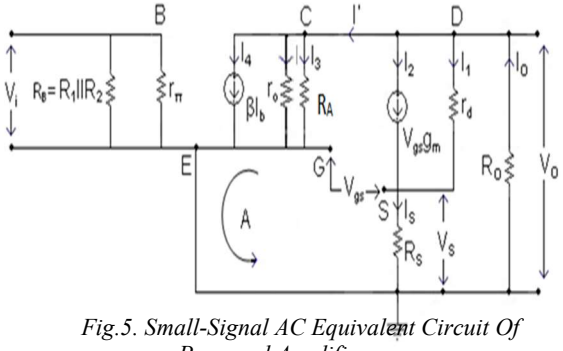

Fig.5. Small-Signal AC Equivalent Circuit Of Proposed Amplifier

$$V_{gs} + I_s R_s = 0$$

$$V_{gs} + (I_o - I')R_s = 0 \quad (1)$$

$$I' = I_3 + I_4$$

As node G at ground, therefore

$$R_C = r_o \| R_A$$

$$I' = -\frac{V_o}{Rc} + \beta I_b \quad (2)$$

Placing equation (2) in (1)

$$V_{gs} + \left[I_o - \left(-\frac{V_o}{Rc} + \beta I_b\right)\right] R_s =$$

$$V_{gs} + \frac{V_o R_s}{R_o} + \frac{V_o R_s}{Rc} - \beta I_b R_s = 0$$

$$V_o\left(\frac{R_s}{R_o} + \frac{R_s}{Rc}\right) = \beta I_b R_s - V_{gs}$$

$$V_{gs} = \beta I_b R_s - \frac{V_o R_s}{R_o} - \frac{V_o R_s}{Rc} \quad (3)$$

Now, applying KCL at node D s

$$I_o = I_1 + I_2 + I_3 + I_4$$

$$\frac{V_o}{R_o} = \frac{V_s - V_o}{r_d} + V_{gs} g_m + \left(-\frac{V_o}{Rc}\right) + \beta I_b$$

$$\frac{V_o}{R_o} + \frac{V_o}{Rc} = \frac{V_s}{r_d} - \frac{V_o}{r_d} + V_{gs} g_m + \beta I_b$$

$$\frac{V_o}{R_o} + \frac{V_o}{r_d} + \frac{V_o}{Rc} = \frac{-V_{gs}}{r_d} + V_{gs} g_m + \beta I_b$$

$$\frac{V_o}{R_o} + \frac{V_o}{r_d} + \frac{V_o}{Rc} = V_{gs}\left(g_m - \frac{1}{r_d}\right) + \beta I_b \quad (4)$$

Placing equation (3) in (4)

$$\frac{V_o}{R_o} + \frac{V_o}{r_d} + \frac{V_o}{Rc} = \left(\beta I_b R_s - \frac{V_o R_s}{R_o} - \frac{V_o R_s}{Rc}\right)\left(g_m - \frac{1}{r_d}\right) + \beta I_b$$

$$\frac{V_o}{R_o} + \frac{V_o}{r_d} + \frac{V_o}{Rc} = \beta I_b R_s \left(g_m - \frac{1}{r_d}\right) - V_o R_s \left(\frac{1}{R_o} + \frac{1}{Rc}\right)\left(g_m - \frac{1}{r_d}\right) + \beta I_b$$

$$\frac{V_o}{R_o} + \frac{V_o}{r_d} + \frac{V_o}{Rc} = \beta I_b \left[1 + R_s\left(g_m - \frac{1}{r_d}\right)\right] - V_o R_s \left(\frac{1}{R_o} + \frac{1}{Rc}\right)\left(g_m - \frac{1}{r_d}\right)$$

$$V_o\left[\frac{1}{R_o} + \frac{1}{r_d} + \frac{1}{Rc} + R_s\left(g_m - \frac{1}{r_d}\right)\left(\frac{1}{R_o} + \frac{1}{Rc}\right)\right] = \beta I_b \left[1 + R_s\left(g_m - \frac{1}{r_d}\right)\right]$$

$$V_o = \frac{\beta I_b \left[1 + R_s\left(g_m - \frac{1}{r_d}\right)\right]}{\left[\frac{1}{R_o} + \frac{1}{r_d} + \frac{1}{Rc} + R_s\left(g_m - \frac{1}{r_d}\right)\left(\frac{1}{R_o} + \frac{1}{Rc}\right)\right]} \quad (5)$$

Since $V_i = r_\pi I_b$ and $A_V = \frac{V_o}{V_i}$

Therefore, small-signal AC voltage gain of the proposed amplifier of Fig.3 will be

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$$A_V = \frac{\beta\left[1 + R_s\left(g_m - \frac{1}{r_d}\right)\right]}{r_\pi\left[\frac{1}{R_o} + \frac{1}{r_d} + \frac{1}{Rc} + R_s\left(g_m - \frac{1}{r_d}\right)\left(\frac{1}{R_o} + \frac{1}{Rc}\right)\right]} \quad (6)$$

The above expression shows that the

$A_v \alpha Rc$ ($R_C = r_o \| R_A$)

$A_v \alpha R_O$ ($Ro = R_L$)

This is further proved by the observations taken during the study of the proposed amplifier. It is found that the reference amplifier produces 3.5% T.H.D whereas proposed amplifier crops 5.296E-06% T.H.D. The proposed amplifier has extremely low value of T.H.D falling within the permissible limit of T.H.Ds for small-signal amplifiers **[19].**Presence of additional biasing resistance R_A in circuit configurations of respective amplifier put a significant impact on their performances which is shown in Table-6.

Table-3 Performance Parameters For Maximum And Minimum Values Of R_1 And R_2

Parameters	R_1		R_2	
	Max. (20k)	Min.(95k)	Max. (5k)	Min.(3k)
A_{VG}	281.331	8.816	281.331	93.507
A_{IG}	33.698	3.209	33.698	2.964
f_L	5.191 KHz	263.027 Hz	5.191 KHz	3.3113 KHz
f_H	22.567 MHz	33 3.827 MHz	22.567 MHz	116.554 MHz
Bandwidth	22.562 MHz	33 3.827 MHz	22.562 MHz	116.551 MHz

Table no. 3 shows that on decreasing the value of R_1 the values of current gain and voltage gain increases with narrowing of bandwidth by increasing the lower cut-off frequency whereas the value of high cut-off frequency decreases to its minimum value and vice-versa. Similarly, for minimum value of R_2 the current gain as well as the voltage gain gets reduced with widened bandwidth while on increasing the value of R_2 the current gain and voltage gain increases with increase in the value of lower cut-off frequency and reduced value of higher cut-off frequency which causes a significant change in the bandwidth. Thus we see that on varying R_1 from minimum to maximum the proposed amplifier can amplify signals from 5kHz to 333MHz that includes all the frequencies from VLF(very low frequency range) to VHF(very high frequency range).

Table-4 Performance Parameters For Maximum And Minimum Values Of Rs And R_d

Parameters	Rs		R_D	
	Max. (30k)	Min. (2Ω)	Max. (3k)	Min. (110Ω)
A_{VG}	303.107	281.331	281.331	20.84
A_{IG}	36.741	33.698	33.698	3.0413
f_L	5.104 KHz	5.191 KHz	5.191 KHz	6.066 KHz
f_H	30.199MHz	22.567 MHz	22.567 MHz	380.189 MHz
Bandwidth	30.194MHz	22.562 MHz	22.562 MHz	380.188 MHz

Table 4 shows that the proposed amplifier gives moderate value for current gain at minimum values of Rs with high voltage gain and moderate bandwidth that comes in HF region (high frequency) range. Whereas on increasing the value of R_S and R_D voltage gain and current gain increases to its maximum value. Similarly on increasing the value of Rs the value of F_L nearly remains unchanged whereas F_H increases slightly causing increased bandwidth while on increasing the value of R_D the value of F_L decreases slightly but the decrease in the value of F_H is significant which causes a significant decrease in bandwidth. Thus in terms of current gain and voltage gain R_s plays a significant role whereas in terms of bandwidth R_D plays the vitality. This proves that voltage gain of

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MOSFET based amplifiers is directly proportional to drain resistor.

Table-5 Performance Parameters for Maximum And Minimum Values Of R_{ss} And R_l

Parameters	R_{SS}		R_L	
	Min. (1Ω)	Max. (70k)	Min. (10Ω)	Max. (60k)
A_{VG}	301.387	1.143	3.230	303.097
A_{IG}	35.818	8.069	398.314	5.997
f_L	5.495 KHz	470.227 Hz	6.536 KHz	5.185 KHz
f_H	127.637 MHz	1.791 MHz	475.354 MHz	21.061 MHz
Bandwidth	127.632 MHz	1.791 MHz	475.353 MHz	21.056 MHz

Table 5 expresses that the value of voltage gain decreases with the increase in the value of source resistance and attains unity at 70K with compromised values of current gain and bandwidth. Thus keeping R_{SS} to its minimum value is beneficial in all terms to achieve optimum performance of the proposed amplifier.

On the other hand variation in R_L to its minimum value(10Ω) leads the voltage gain **[5,12,14]** to its minimum value and maximum value of current gain i.e 398.314, which is significantly high and makes this amplifier feasible to use in such devices which need high current gain . On increasing the load resistance to 60K the current gain drops to 5.997. Moreover the decrease of load resistance results in the widening of bandwidth up to 475MHz which comes in VHF range.

On discussing R_L we see that variation in R_L gives a wide range of A_{ig}, and B.W with an interesting feature. For maximum value of R_L the voltage gain increases to its peak value at the cost of reduced current gain and bandwidth. Whereas on decreasing the value of R_L to its minimum the value of current gain and bandwidth rises to its peak on the cost of considerably reduced voltage gain. This nature of the proposed amplifier is quite in accordance with the small signal Sziklai pair and Darlington pair amplifiers.

Thus the proposed amplifier can amplify signals from 5.185KHz (at R_L=60K) to 475.353MHz at (R_L=10Ω).Conclusively appropriate selection of the active elements pursues the amplifier in being capable of amplifying (super low frequency) signals which can penetrate seawater up to a depth of approximately 100 meters that allows its application in VLF receivers , SONARS, autonomous underwater vehicle for underwater communication as well as UHF(ultra-high frequency) signals which makes it suitable to be used for T.V broadcasting, cell phones , satellite communication services including GPS , personal RADIO services ,cordless phones , satellite phones and Bluetooth walkie-talkies **[22,23]**

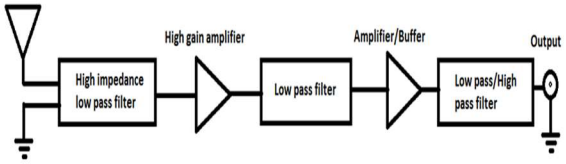

Fig.6 Block Diagram of VLF Reciever

Fig-6 shows the architecture block diagram of VLF receiver , where the proposed amplifier can be used at the position of high gain amplifier .These receivers are used by the geologists to measure the conductivity in the near surface of the earth.

Table-6 Performance Parameters For Maximum And Minimum Values Of R_A And R_e

Parameters	R_A		R_E	
	Max. (2k)	Min. (90Ω)	Max. (190Ω)	Min. (5k)
A_{VG}	281.331	18.46	295.246	4.227
A_{IG}	33.698	4.879	34.694	1.054
f_L	5.191 KHz	5.995 KHz	5.495 KHz	368.649 Hz
f_H	22.567MHz	410.518 MHz	18.197 MHz	
Bandwidth	22.562MHz	410.517 MHz	18.192MHz	798.109MHz

It is clear from Table 6 that at minimum value of R_A the voltage gain drops with increased bandwidth covering the entire range from 5KHz to

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410MHz making it entirely feasible for its use in preamplifier stages of long distance communications in military and defense avionics, electronic warfare, SONARs, Audio amplifiers, TV broadcasting **[22,23]**etc. Also we can see that on increasing the value of R_E the current gain decreases to unity with decrease in the voltage gain to its minimum value (4.227) with a drastic increase in bandwidth. On decreasing R_E to its minimum value the current gain is 34.694 with maximum voltage gain of 295.246. Thus current gain and voltage gain is directly proportional to R_A and inversely proportional to R_E. This is because the transistor being a current source, keeps the current constant, and so voltage across resistance R_A will go up with any increase in resistance which implies that the output voltage changes more providing larger voltage gain. Whereas the base emitter voltage does not change as much so the current change is less and therefore the gain is reduced. This happens because the emitter current change causes the emitter voltage to change in the same direction as the change in base voltage, partially counteracting the effect. On variation in R_A and R_E the amplifier amplifies signals from 5KHz to 798MHz which shows that the proposed amplifier is capable of amplifying signals from VLF(very low frequency range) to UHF(ultra high frequency range).Thus it's application widens to T.V broadcasting , wireless communication ,satellite phones, mobile communications such as GSM, CDMA and LTE services, Wi-Fi etc.

Fig-2 shows the block diagram of a wireless communication system in which proposed amplifiers can be used at the position of the drive amplifier. Bluetooth, Wi-Fi, radar, radio are some applications where electromagnetic signals broadcast from sending facilities to intermediate and end user devices.

When an additional capacitor C_E is removed, the voltage gain (A_v= -11.346) and current gain (A_I = 4.244) decreases with an increase in bandwidth. Moreover on increasing the value of C_E, voltage gain increases with decrease in current gain and narrowing the bandwidth **[1,2, 11]**. This happens due to the charging of capacitor, when it is about to be saturated, voltage across the capacitor increases initially and then becomes fixed whereas the current decreases.

Table-7 Variation Of Performance Parameters With Additional Capacitance C_E:

C_E	A_{VG}	A_{IG}	f_L	f_H	B.W (MHz)
1 nF	205.960	67.125	20.539 MHz	52.920MHz	32.381 MHz
10 nF	271.599	47.456	3.981 MHz	27.498 MHz	23.517 MHz
100 nF	279.938	48.584	458.897 KHz	23.333 MHz	22.875 MHz
1 µF	281.207	88.722	47.658 KHz	22.765MHz	22.717 MHz
10 µF	281.331	33.698	5.191 KHz	22.567MHz	22.562 MHz
100 µF	281.339	10.457	1.042 KHz	22.506 MHz	22.505 MHz

3.1.2. Variation Of Voltage Gain And Current Gain With Supply Voltage:

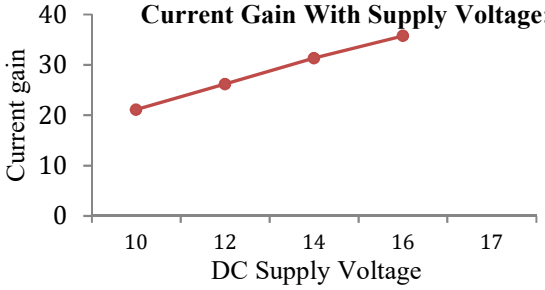

Fig 7(a)

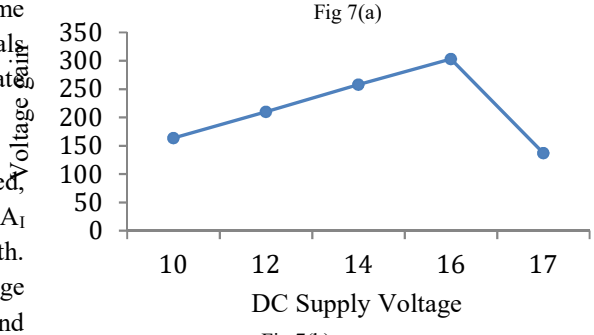

Fig 7(b)

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From fig.7(a) it is clear that the value of voltage gain increases with increase in supply voltage and attains maximum value of AVG =303.241at 16 Volt which is the critical voltage and decreases exponentially. The output waveform deteriorates further on increasing the supply voltage **[17].**Whereas on increasing the supply voltage the current gain increases to a maximum value of A_{IG} = 35.78 at 16 Volt as shown in fig 7(b).

3.2 Thermal Analysis:

Table-8 Variation Of Performance Parameters With Temperature:

TEMPERATURE	A_{VG}	A_{IG}	f_L (KHz)	f_H (MHz)	B. W (MHz)
-40	327.217	39.77	6.475	23.604	23.598
-30	316.537	38.738	6.208	23.519	23.513
-20	312.183	37.756	6.048	23.564	23.558
-10	305.153	36.823	5.955	23.350	23.345
0	298.413	35.932	5.495	23.280	23.275
10	291.912	35.077	5.495	23.098	23.093
20	285.623	34.250	5.235	23.034	23.029
27	281.331	33.698	5.191	22.567	22.562
30	279.495	33.457	5.136	22.624	22.619
40	273.578	32.696	5.064	22.107	22.102

From the table 8 we can observe that the proposed amplifier exhibits better results at low temperatures. We can see that the values of various performance parameters increase with the decrease in temperature. This is because MOSFET exhibits negative temperature coefficient at higher values of gate to source voltage. As the gate to source voltage increases the drain current decreases with increase in temperature. On increasing the temperature, the space between atoms increases due to thermal expansion of the energy states which the result of increased lattice vibration. Due to the lattice vibration the band gap decreases and collision rate increases between majorities charge carriers and ions in the semiconductor channel. As a result the mobility of charge carriers decreases due to which drain current of MOSFET and therefore the resultant voltage gain and current gain decreases with increase in temperature **[24]**.

4. RESULTS AND DISCUSSIONS:

Table-9 Performance Parameters Of The Reference And Proposed Amplifiers

Parameters	Reference Amplifier (under P-Spice simulation)	Proposed Amplifier (under Cadence Virtuoso and Spectre simulation)
Avg (voltage gain)	115.522	281.331
Aig (current gain)	35.242	33.698
F_L(lower cut-off frequency)	448.197Hz	5.191KHz
F_H(higher cut-off frequency)	22.794KHz	22.567MHz
Bandwidth	22.345KHz	22.562MHz
Vo(peak output voltage)	106.567Mv	53.385mV
Io (peak output current)	10.664 µA	28.133µA
Device Avg(device voltage gain)	-	281.331
Device Aig (device current gain)	-	38.046
T.H.D	3.5%	5.296E-06%
Power Consumption	-	165.0614mW
Input Noise	3.223nV/sq.Hz	23.1676nV/sq.Hz
Output Noise	0.3455µV/sq.Hz	5.5523pV/sq.Hz
Slew Rate	-	106.389 µV/m sec
Power Gain	4071.226	9480.292
Input Signal Voltage	1mVat 1KHz	1mV at 1KHz
Permissible range of input signal voltage	0.01-15mV	1mV-10mV

Table-9 shows that the qualitative features of the proposed as well as the reference amplifier. The inclusion of an additional resistance R_A and R_E to the reference amplifier enhances its performance which is exhibited by the data mentioned in table-5. The data reveals that *the proposed amplifier is better than the reference amplifier in terms of voltage gain as it rises from 115.22 to 281.331 which is more than the double of initial value, bandwidth which is 1000 times better than the reference amplifier , moderate power consumption, negligible distortion in micro range ,stability due to high slew rate i.e 106.389µV/m sec and extremely low input and output noise of nano and pico range respectively with a compromise in the value of*

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current gain. Also the peak current of proposed amplifier is nearly thrice the peak current for reference amplifier [1, 2, 11]. Thus, from all the observations we can conclude that the proposed amplifier is very promising in wireless communication system with higher values of gains, lower value of T.H.D and noise. It is also free from poor response problem at higher frequencies.

5. PRE LAYOUT AND POST LAYOUT SIMULATION:

The layout design of the proposed amplifier at 180nm technology is shown in Fig.8 which is designed using Layout XL Tool. The BJT and MOSFET used here are all integrated because the substrate is directly connected to the source **[24]**. The INPUT, OUTPUT, VDC and GND pins are fixed at the left, right, top and bottom of the layout respectively **[24]**.

The dimensions of layout are 7.975µm and 7.91µm respectively, with the Layout area equals 63.08225µm^2. DRC and LVS runs are done exhibiting no errors and give approximately similar results pre and post layout simulation with variation in permissible range [**25**].

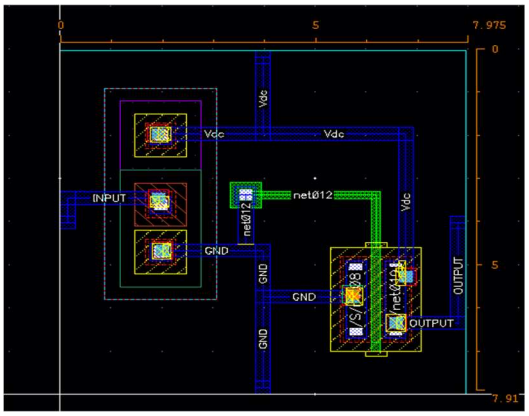

Fig.8 Layout of Proposed Amplifier

Now comparing the pre-layout and post layout results as follows:

Parameters	Pre-Layout	Post-Layout	% Variation
Voltage gain	281.331	281.207	0.05
Current gain	33.698	88.911	164.32
Bandwidth	22.562MHz	22.654MHz	0.3
Power Consumption	165.044mW	164.717mW	0.62
Slew Rate	16.199 µV/µsec	12.627 µV/µsec	22.04

6. CONCLUSIONS:

Present paper comprises of small signal amplifier using hybrid unit of BJT and MOSFET in Darlington pair and it's simulation is done and the results are compared. Proposed amplifier circuit has high values for current gain and voltage gain when simulated on Cadence Virtuoso and Spectre simulation with an added resistance when compared to the reference amplifier which was simulated on P-spice simulation software.

Whereas the band width of proposed amplifier is to be of high frequency (1MHz to 30MHz), also known as decimeter band as the wavelengths range from one meter to one tenth of a meter. Thus these amplifiers can be used in commercial and defense avionics, space and deep space, electronic warfare, naval applications, mobile internet, satellite communication and wireless communication. Also with an appropriate change in the biasing resistances, the proposed amplifier can perform as preamplifiers in VLF receivers , SONARS, autonomous underwater vehicle for underwater communication as well as UHF (ultra-high frequency) signals which makes it suitable to be used for T.V broadcasting, cell phones , satellite communication services including GPS , personal RADIO services ,cordless phones , satellite phones and Bluetooth walkie-talkies mobile communications such as GSM, CDMA and LTE services, Wi-Fi etc**[22,23]**. A problem that arises in the development of these amplifiers is that the gain of the amplifier reduces as it enters in the 700MHz frequency range. So, to overcome this problem the value of R_L can be raised so that the gain can be increased.

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