

IMPLEMENTING JERK FREE BLDC POSITION CONTROL USING SOC WITH FOURTH ORDER TRAJECTORY PLANNING

AJAY PAITHANE^{1*}, SAKSHI PAITHANE², SUNIL DAMBHARE³, MADHAV THIGALE⁴ AND MUKIL ALAGIRISAMY⁵

¹Associate Professor in E&TC Department of Dr. D. Y. Patil Institute of Engineering Management and Research, Pune.

²Associate Professor in E&TC Department of JSPM's Rajarshi Shahu College of Engineering, Tathawade, Pune.

³Professor in Mechanical Department of Dr. D. Y. Patil Institute of Engineering Management and Research, Pune.

⁴Assistant Professor in E&TC Department of Dr. D. Y. Patil Institute of Engineering Management and Research, Pune.

⁵Associate Professor, Faculty of Engineering, Lincoln University College, Malaysia.

E-mail: ajay.paithane@dypiemr.ac.in, sapaithane_entc@jspmrscoe.edu.in, sunil.dambhare@dypiemr.ac.in, madhav.thigale@dypiemr.ac.in, mukil.a@lincoln.edu.my

ABSTRACT

High Performance Motion Systems is essential for precise position of equipment used in the medical, automotive industries. Accomplishing the precise position with minimal time and vibration is a real challenge which makes design complex. Motion control system, typically requires three components- motor drive, electrical control hardware and control algorithm. Diligently determining each component of motion control is a crucial for high performance system and low development time. This paper demonstrates use of BLDC motor drive. The design and implementation of BLDC commutation and peripheral interfaces in programmable hardware logic in Zynq SoC processor as electrical control hardware. Fourth order trajectory Planning which improves the position accuracy and reduces vibration as a control algorithm can be used for high performance motion systems. The simulation result of FPGA control logic of BLDC commutation and peripheral interface demonstrate that processor can offload its task to FPGA. Test result for the hardware implementation affirms the accuracy and minimal vibration. Thus, Implementing BLDC motor as a Drive, Zynq SoC as control Hardware and fourth order algorithm as a control algorithm give high performance motion with ease of development time.

Keywords: *SoC, FPGA, Trajectory Planning, BLDC, Encoder, CAN*

1. INTRODUCTION

Precision position control is frequently required in high performance motion control systems like medical equipment, robots, industrial automation, instrumentation, computer hard disk, automotive and space technology [6,17]. Motion control system, typically requires three components- motor drive, control hardware and control algorithm. It is important to diligently select all the three components. There is different alternative for each component.

1. For actuator motor drive, there are different drive options like Brushed DC, Brushless DC (BLDC), Permanent Magnet Synchronous Machines and

Stepper motor. The choice of appropriate motor selection depends on the application needs [3,7].

2. For control Hardware, there are different options. Use ARM controller [26] or DSP processor [4,8] or microcontroller [1] or use the SoC [33] [27] or use the FPGA [34],[2],[29].

3. Similarly there are different alternative for control algorithm and control hardware like trapezoidal velocity profile, 3rd order s-curve model and 4th order s-curve model [17],[12],[20]. This paper presents the implementation of the precision position control using the unique combination of Brushless DC Motor (BLDC) as an actuator device, FPGA based SoC as has a hardware control mechanism and fourth order trajectory planning model as control algorithm. The BLDC has many advantages over the other motor

types. High dynamic performance, precise controllability, low audible noise, low RFI and high efficiency at optimal cost [1],[3],[13],[23],[27]. In order to accomplish precision motor positioning with minimum vibration and overshoot there are different control planning strategy [14],[20] but the fourth order trajectory planning is ideal to achieve a jerk free profile motion [17],[18]. The Fourth order trajectories need to solve tedious differential equation [17] or trigonometric equation [20],[22] in time bound manner to achieve optimal reliability and accuracy. This requires a hardware control which have superior timing performance. Therefore Zynq-7000 SoC is used as an control Hardware platform. Zynq-7000 SoC product integrates a feature-rich dual or single-core ARM Cortex-A9 MP-Core based processing system (PS) and Xilinx programmable logic (PL) in a single device. The ARM Cortex-A9 MP-Core is the heart of the PS which also includes on-chip memory, external memory interfaces, and a rich set of I/O peripherals. As Zynq-7000 SoC device contains the PS, the PL and I/O resources on the same device, it can easily use for the high-performance motor application The PS consisting of Cortex-A9 MP-Core can used as the computing systems that can implement communication channel, perform loops, timings, decisions and complex mathematic calculations. On other side, the PL can be programmed using a hardware description language (HDL) for accessing and controlling the timings of the peripheral devices. The inherent parallel architecture of PL help to precise control of the peripheral device timings.

2. METHOD

2.1 Principle of Operation of BLDC Motor Drive

In conventional brushed DC motors, the rotor coil current is delivered through carbon brushes. These brushes wear out over the lifetime thereby reducing the robustness [3], [28]. However, in Brushless DC motor (BLDC) as the name suggests, the motor current does not pass through brushes into the coils instead electronics commutation is used. In BLDC motor, the rotor is made up of permanent magnets poles and the coils are fixed which are placed in the stator. Hence no brushes are needed for passing the current in BLDC motors. The permanent magnet on the rotor varies from two to eight pole pairs [31]. The torque ripple requirement determines the number of poles and numbers of slots [11],[33]. Generally permanent magnet is made up of ferrite magnet but now days even rare earth alloy magnet is gaining popularity.

The Stator is made-up of stacked steel laminated plate with winding. Typically, there are six winding connected together in the star fashion [26]. Commutation sequence is needed to rotate the BLDC rotor. In each commutation sequence, one winding end of stator coil is connect to positive potential, another winding end of stator coil is connected to negative potential and last winding end of stator coil is disconnected [34]. Due to which a magnetic field is form by the stator current. Since the BLDC rotor is made up of permanent magnets poles, there is an interaction between magnetic field of stator and rotor. This interaction generates the torque [24]. The maximum torque is generated when orientation of magnetic fields is perpendicular to each other since the torque generated is function of angular difference in between magnetic field and current direction. In order to keep the rotor moving, magnetic field of stator winding should shift its position. The rotor moves to catch-up with stator field. BLDC requires six commutation steps to finish one electrical cycle. Please note that one electrical cycle may or may not be equal to one mechanical revolution. Therefore, winding coil current needs to updated for every 60 degrees of electrical cycle [26]. Reversing the applied phase voltage causes the motor to rotate in the reverse direction [34]

2.2 Fourth Order Trajectory Planning

The Motion control System aims to achieve desired velocity or position using respective feedback loops. But the main concerned of any precise motion control is to attain desired velocity or position in minimum amount of time without overshoot in actual velocity or position and at the same time keeping minimum system vibration [20]. The path planning algorithm always tries to attain desired velocity or position in minimal time, at acceptable overshoot and with minimum system vibration. To accomplish desired position, generally a simple trapezoidal velocity profile is preferred in which the motor drive starts with constant acceleration up-to maximum velocity. Then it continues with maximum velocity and the end it retard with constant de-acceleration. From the figure 2 we observe that step change in the acceleration causes infinite jerk [20]. Therefore, in trapezoidal velocity profile, the system motion exhibits overshoot and excessive vibration. Also, it requires longer time to reach final desired position. This results in potential threat to accomplish precise position. To overcome this problem, fourth Order trajectory planning is used. The fourth Order trajectory is based on constant derivative of jerk profile. The fourth order profile is constrained with

maximum allowable derivative of jerk. The time constants of the constant derivative jerk profile can be obtained from solving the equations of kinematics [11].

The derivative of jerk profile is the input to the controller. To obtain the necessary precise position, the derivative of jerk needs to be integrated four times.

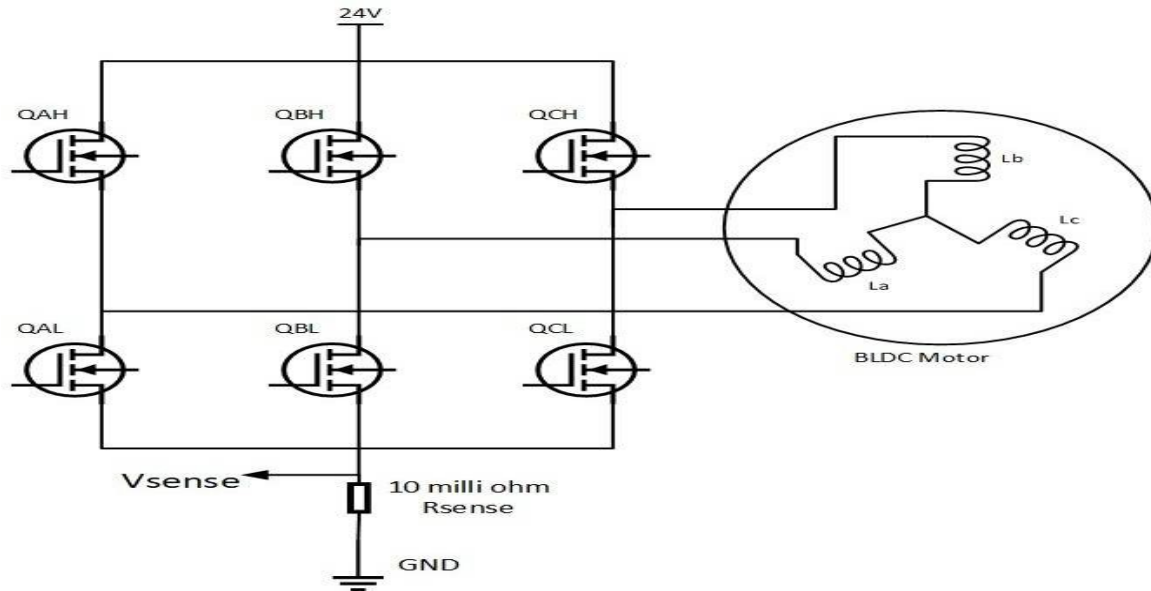


Figure 1. BLDC H-Bridge Configuration

Numerical methods of integration is used for performing integration [15]. Sampling rate of 1 millisecond was considered for all the numerical calculation. The sampling frequency is important and determines the stability and performance of the digital feedback controller [17]. For T to be the sampling time, the derivative of jerk profile is delayed with $2T$, jerk with $1.5T$, acceleration with T and finally velocity by T milliseconds. The derivative of jerk profile followed by integration blocks define the set point for the position control loop. In actual controller design, the derivative of jerk profile is set using lookup table, which is then followed by numerical integration with above-mentioned sampling rates.

2.3 Hardware Design

The figure 4 shows top-level architecture and implementation of precision control position. The input command to the motion control system is given by the CAN commands. For this a personal computer with USB to CAN adaptor is used. Using CAN command a desired velocity or position is set to motion control hardware. The hardware Board consist of SoC Board, BLDC driver, voltage to frequency converter, hall sensor interface, Quadrature increment encoder interface and SSI based absolute position encoder interface circuit. The output of motion control hardware board is connected to BLDC motor. For proper BLDC commutation hall sensor feedback is connected to

the Hardware. The BLDC motor is also assembled with the quadrature incremental encoder to measure the motor shafts speed and detect the motor direction. The BLDC motor's output shaft is connected to gearbox. The gearbox helps to reduces the drive speed and at the same time increases the output torque to drive the system load. The output of the Gearbox is also connected to absolute position encoder to measure the system load position. The absolute position encoder is multi-turn and can measure up to 8 turns. The current sense circuit is needed to implement the MOSFET driver protection logic. A resistive current sensing scheme is used to measuring electrical current on Hardware board. Low value series resistor is connected in series with the return ground path as shown in figure 1. The output current sense voltage is converted into frequency domain. A voltage to frequency converter(V/F) Integrated circuit. (IC) is used for this purpose.

2.4 SSI Position Encoder

Synchronous Serial Interface (SSI) is most commonly used serial interface standard for industrial rotary encoders application (*SSI Synchronous Serial Interface Master - Application Note*, n.d.).

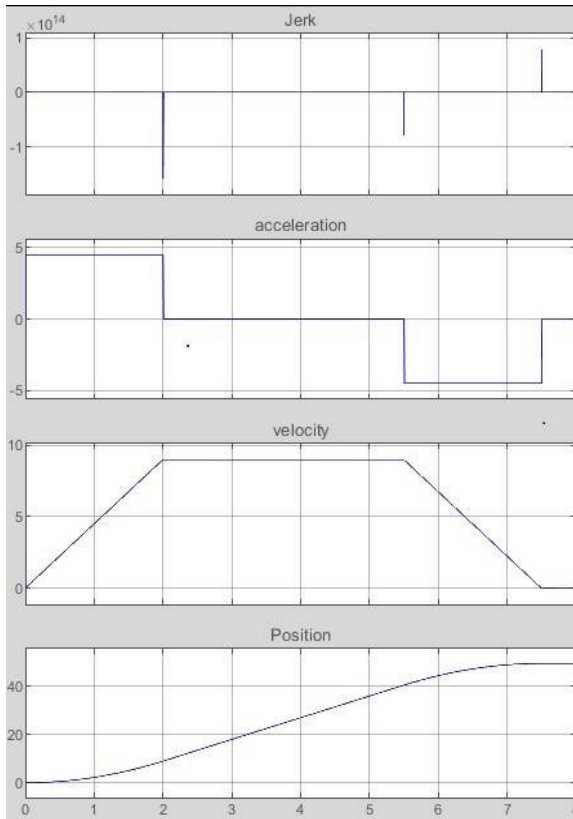


Figure 2. Trapezoidal Path Planning

Master which is SoC has point to point communication with a slave which is rotary position encoder (*SSI Encoders-Encoder Interface Protocols*). The sensor in the slave device continuously updates position data and writes to the output register. The slave device shifts out the output register data when master SoC sends a train of pulses. Thereby SOC can read the actual position of the system load and use it in the planning algorithm. The interface hardware is simple RS-422 transceiver which generate the differential clock from the master to slave and sense differential data received from slave to master. IC like MAX1486 transceiver from MAXIM can be used for RS-422 transceiver [14]. If galvanic isolation is needed, then an isolation can be provided that effectively breaks ground loops thus preventing unwanted current travelling between master and slave (*SSI Synchronous Serial Interface Master - Application Note*, n.d.).

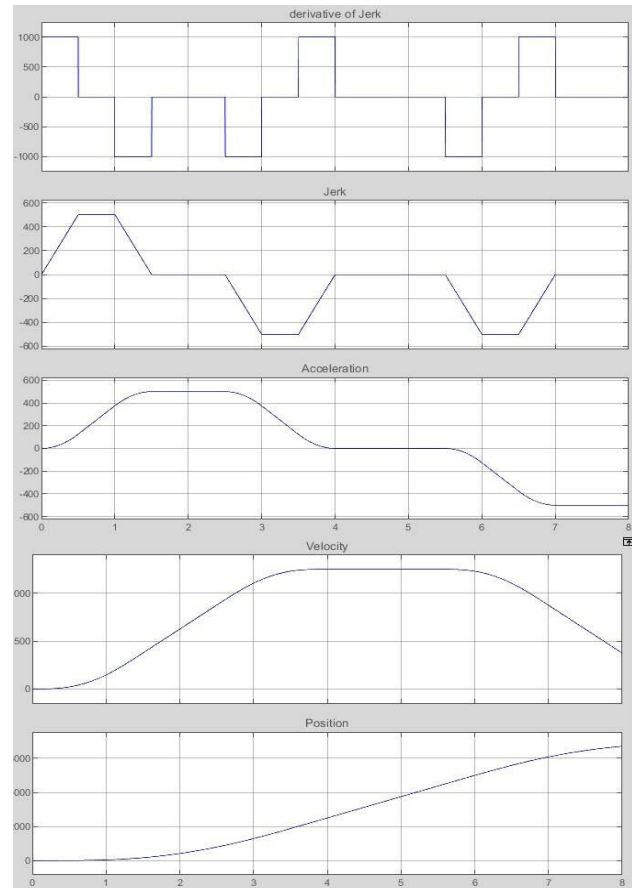


Figure 3. Fourth order Path Planning

is needed, then an isolation can be provided that effectively breaks ground loops thus preventing unwanted current travelling between master and slave (*SSI Synchronous Serial Interface Master - Application Note*, n.d.).

2.5 Quadrature Incremental Encoders

Incremental encoder is needed for the application where in the instantaneous velocity is required like medical industry, automobile, robotics. For measuring instantaneous velocity, encoder need to have high resolution, high accuracy, high noise immunity. The optical incremental encoders consist of circular slotted disc with large number of slots, that are distributed equally. The LED is used to pass the Light through the slots which activates two sensors. The two sensors help to produce two pulses train with phase shift of 90 degrees (quadrature) with each other. The direction of the rotation determines whether a given train pulses will lag or lead with the other. The

frequency of pulses train is proportional the angular velocity. The SOC detects phase angle between pulses to determine the direction of BLDC motor

and measure the frequency of the train pulse to calculate the instantaneous angular velocity.

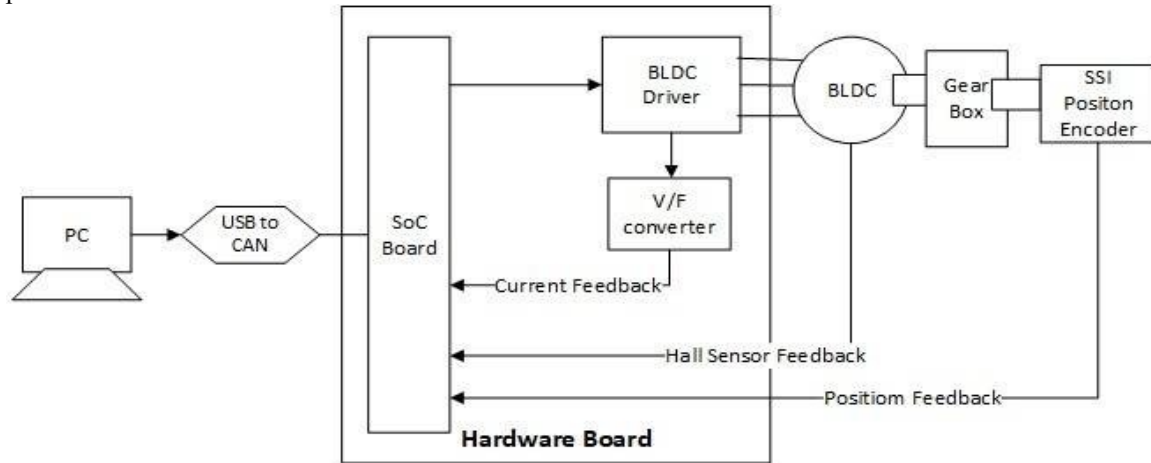


Figure 4. System Block Diagram

2.6 Gear Box

Gearbox is required to change the speed and torque so that converted mechanical energy can be used to drive the load. In precision position control application, the gearbox is used to reduce output rotational speed and to increase output torque. There is different type of gearbox - Helical gearbox, Coaxial helical inline, Bevel helical gearbox, Planetary gearbox, Worm reduction gearboxes. Harmonic drives are widely used wherein the applications requires high torque. It is superior to planetary gear on account of high reduction ratios, size, small weight, zero backlash and compactness [9].

2.7 BLDC Driver

The BLDC Driver IC used is TLE7184F. It controls six MOSFET connected in the bridge configuration. It helps to reduce the discrete components in typical BLDC applications and give sufficient flexibility for customization. This IC receives reset signal and 6 MOSFET control signal from the SoC. It also has Current sense Op-Amp which helps for current measurement. It also has protection mechanism for Short Circuit, Over Voltage, Under Voltage and over-temperature. Six N-channel MOSFETs are used to make three-phase bridge structure for BLDC motor. These MOSFETs are selected taking into consideration of low ON resistance, high drain to source breaks down

voltage, high surge current, Gate charge, Reverse Transfer Capacitance and fast reverse recovery time. The BLDC Motor Driver contains three phase inverter circuits as discussed in figure 1 to turn on the supply voltage on each motor phase according to the SoC signals. The SOC determines commutation pattern based on the direction and Hall Sensor Feedback signal. Also a SSI interface is implemented to read the position encoder on the Hardware board.

2.8 Voltage to Frequency Converter

The Voltage to Frequency (V/F) IC used in the design is AD7740. It used a charge- balance for the conversion. It requires minimal external Components

for implementation. The nominal applied input Range is from 0V to VREF. The SoC feeds the reference frequency to AD7740 and measures the output frequency of AD7740. The nominal input range from 0 V to VREF corresponds to an output frequency of 10% of CLKIN to 90% of CLKIN.

2.9 SoC Design

The FPGA based SoC is a heart of the position design which accepts the control command from the PC over CAN and execute the Fourth order planning algorithm. The processing logic(PL) or processor fabric does all the communication over CAN and RS232 terminal whereas the programmable logic(PL) also known as FPGA

fabric performs all the interface with the peripherals. Since peripheral logic is implemented in FPGA fabric, all interface logics executes

concurrently. This helps to improve the execute time for control system algorithm as the PLA to do only the high-level arithmetic calculation.

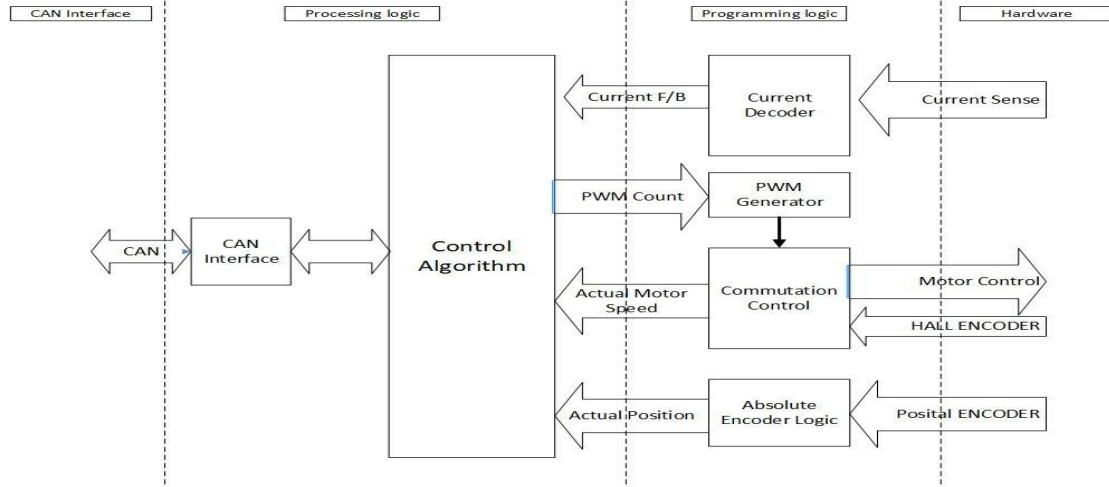


Figure 5. System Block Diagram

2.10 CAN Interface

CAN Controller inside the SOC is compatible to ISO 11898-1, CAN 2.0A, and CAN 2.0B standards. In our precision control application, the Standard (11-bit identifier) frames with Bit rates of 250Kb/s is implemented. The CAN specification is high immunity to electrical noise and has ability to self-diagnose and repair data errors. These features have made CAN very popular in medical, manufacturing and automation (*Introduction to the Controller Area Network (CAN)*). In normal mode, if there is any error or arbitration loss then the CAN protocol automatic performs re-transmission. This makes CAN protocol usage easy at the application layer. The computer program on the PC sends the

set position, set velocity or set PWM command over the CAN and receive the instantaneous position, velocity and applied PWM.

2.11 PWM Generation Logic

In power electronics, the pulse width modulation (PWM) is widely used to control power by controlling the power switch [16]. In this paper power switch is MOSFET as shown in the figure 1. The desired PWM output is generated by comparing the up-counter and reference count. The PWM signal is set high when up-counter's value is less than reference count indicated as Set PWM in figure 6 else the PWM signal is reset to low [10].

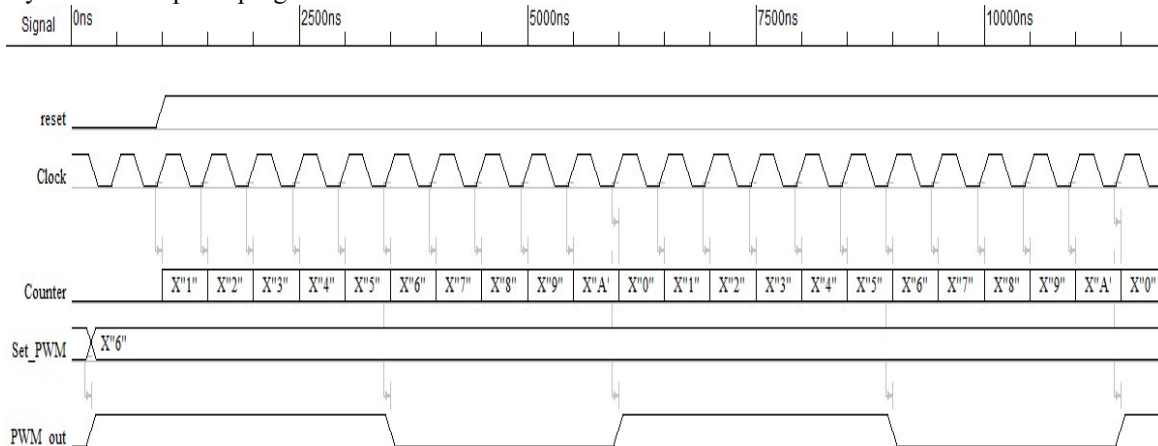


Figure 6. PWM Generation Logic

For changing the PWM duty cycle, we need to change reference count or Set PWM as shown in figure 6 and for changing the PWM frequency we need to change the terminal count of up-counter [25].

2.12 BLDC Commutation Logic

As discussed in earlier section 2.1, the BLDC motor required proper energizing coil sequence to rotate in one direction. Please check individual motor’s datasheet to find either it is clockwise or anticlockwise. The equation for each MOSFET enable is derived as (*toshiba.semicon-storage.com*, n.d.) QAH = A and (not B) QBH = B and (not C) QCH = C and (not A) QAL = (not A) and B QBL = (not B) and CQCL = (not C) and A. The commutation implementation is done using the stats or the look-up table as given below [17]

Table 1: The Commutation implementation

Hall A-	Hall B-	Hall C-	QA H	QB H	QC H	QA L	QB L	QC L	Coil A-	Coil B-	Coil C-
1	0	1	1	0	0	0	1	0	V+	V-	OFF
1	0	0	1	0	0	0	0	1	V+	OFF	V-
1	1	0	0	1	0	0	0	1	OFF	V+	V-
0	1	0	0	1	0	1	0	0	V-	V+	OFF
0	1	1	0	0	1	1	0	0	V-	OFF	V+
0	0	1	0	0	1	0	1	0	OFF	V-	V+

2.13 Current Decoder Logic using Frequency Counter

As discussed in earlier section, the current measurement is done using Voltage to Frequency converter IC. The sense resistor converts the current into voltage and output frequency of V2F IC corresponds to BLDC current is connected to current decoder block in figure 7. The frequency signal is then measured using the frequency counter block using the time interval method.

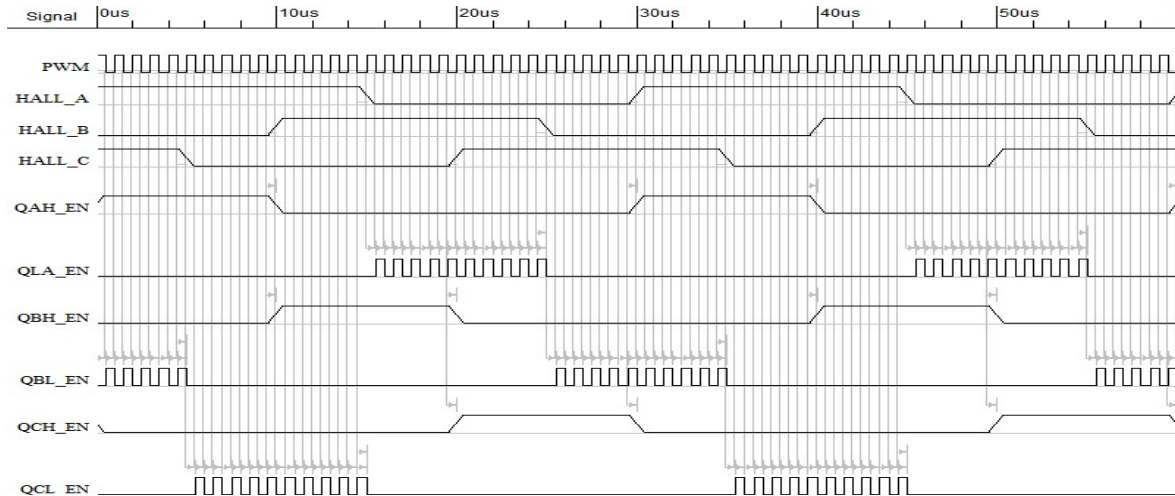


Figure 7. BLDC Commutation

In time interval method, the received input frequency pulses are counted for fixed time slot. The fixed time interval is called as the time base. For measurement of input pulse, a gate controlled for fixed interval. Input pulses passing through the

gate is connected to the counter. At the end of interval, output value of counter is latched for the measurement. The counter is reset after each measurement but the latched value is available all the time for SoC to read.

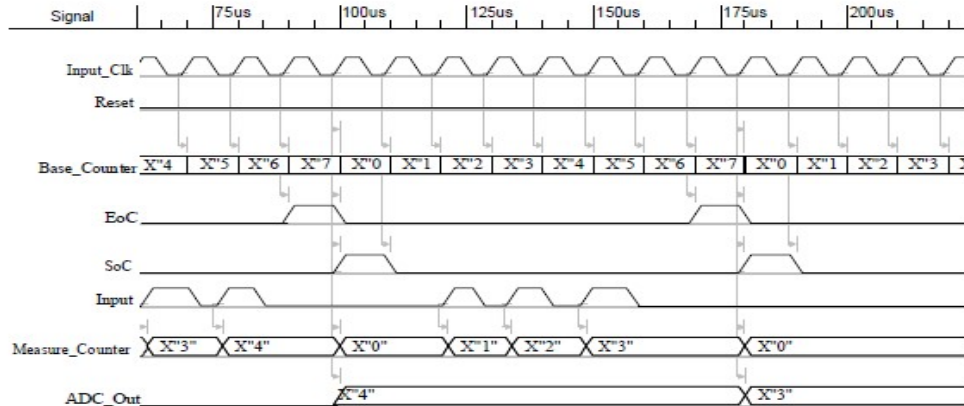


Figure 8. Current Decoder

2.14 Quadrature Encoder Logic

The quadrature encoder is connected to the BLDC motor shaft. The encoder generally has three outputs namely “Channel A”, “Channel B” and “Index”. The “Channel A” and “Channel B” are signals consist of a pulses train, which is 90-degree phase shift. The third signal is called Index which

give one pulse per motor shaft revolution. To determine the motor direction, the “Channel B” level is sensed at the rising edge of the “Channel A” signal. The level is high then it is Clockwise rotation and if level sampled is low then motor shaft is rotating in an anticlockwise direction. In this paper fixed-time methods is implemented that the counts pulse over a fixed time period [19].

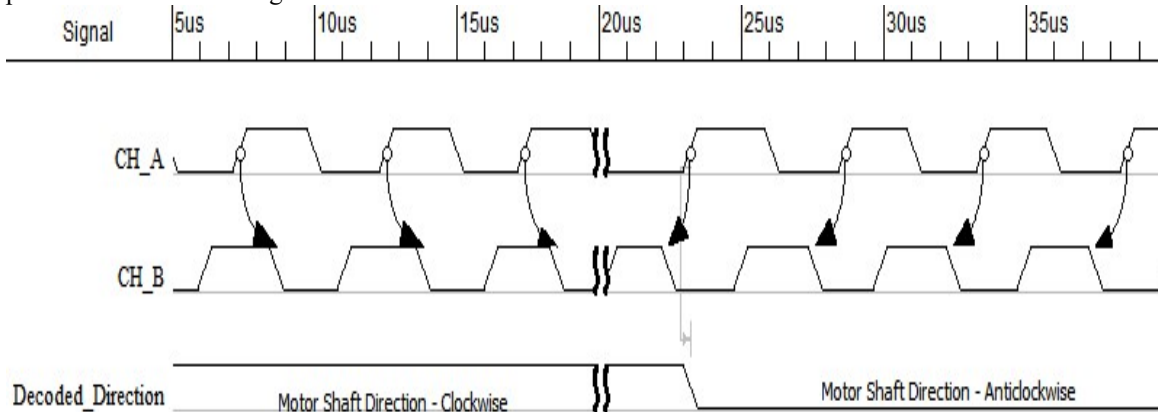


Figure 9. Quadrature Encoder Logic

The encoder used in this paper is 512 counts per revolution (CPR) and the gearbox used is 120:1 ratio. Therefore, the with respect to the angular position is as follows.

CPR of output Shaft = CPR of Motor Encoder x Gear Box Ratio. CPR of output Shaft = 512 x 120
 CPR of output Shaft = 61440. Pulse per degree rotation = 61440/360 = 170 count/degree. The motor velocity is calculated by measuring one encoder channel to using Frequency counter block.

2.15 SSI Absolute Interface Logic

The interface of slave SSI absolute encoder with master SoC is done by using only two signals namely SSI CLOCK and SSI DATA. The FPGA Logic generate 16 pulse train generated on SSI CLOCK signal and captures 16-bit data word from the encoder on SSI Data for reading a position data [31]. The FPGA logic implements a state machine to implement SSI interface. The initial state of SSI CLOCK is HIGH. For reading the SSI encoder, the state machine toggles the SSI CLOCK signal 16 times per read cycle. In response the SSI encoder drives the data signal at each rising edge of

the SSI CLOCK signal. The received data is captured at falling edge of the SSI CLOCK. No particular start or stop sequence is required for fetching the SSI encoder data. Next data transfers have account for the transfer pause so that SSI encoder can update the next position value. The state machine should take care of the maximum SSI CLOCK frequency and transfer pause period between two read as per the encoder's datasheet. The data fetched from the SSI encoder is registered which can be accessed programming logic. Angle Calculated from the Multi-turn Value is Number of Turns = 8. Measurement Range = 360 degrees x 8 turn = 2880-degree Number of Output Bit = 16. Maximum encoder value = 0xFFFF = 65535 Therefore Angle per Count = Measurement Range/Maximum encoder value Therefore Angle per Count = 2880/65535 = 0.0439 degree/count.

2.16 Control Algorithm

The fourth order trajectory is the reference point for the position control PID block. On other side the position control PID receives the actual position from SSI interface logic and accordingly it calculates the error and provide the reference velocity to velocity control PID. The Velocity control PID also receives the actual motor velocity from quadrature encoder using Quadrature encoder logic. Accordingly, the velocity control PID calculates the error and provide the desired PWM and direction of rotation which is fed to BLDC commutation logic.

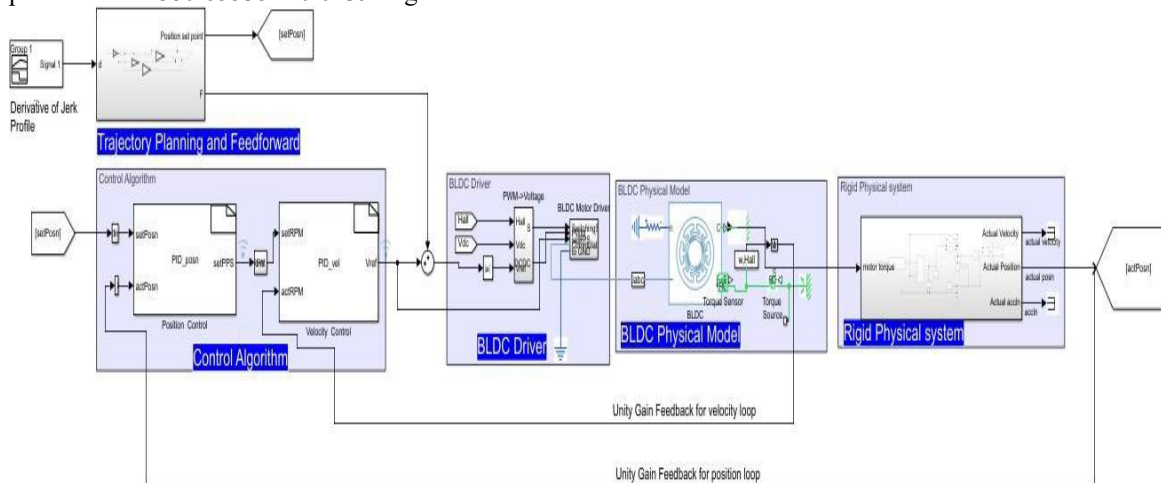


Figure 10. 4th Order Control Logic

3. RESULT:

3.1 Simulation and Implementation

The IO peripheral Block BLDC motor 2 is designed which consist of Current Decoder, Quadrature incremental speed detector, PWM generator, BLDC commutation logic and SSI absolute encoder logic. Following figure 11, 12, 13 shows the simulation result of PWM generation logic, SSI Interface logic and BLDC commutation logic simulation results respectively. The simulation shows that BLDC commutation and peripheral interface can be offloaded to FPGA fabric.



Figure 11. PWM Generation Simulation

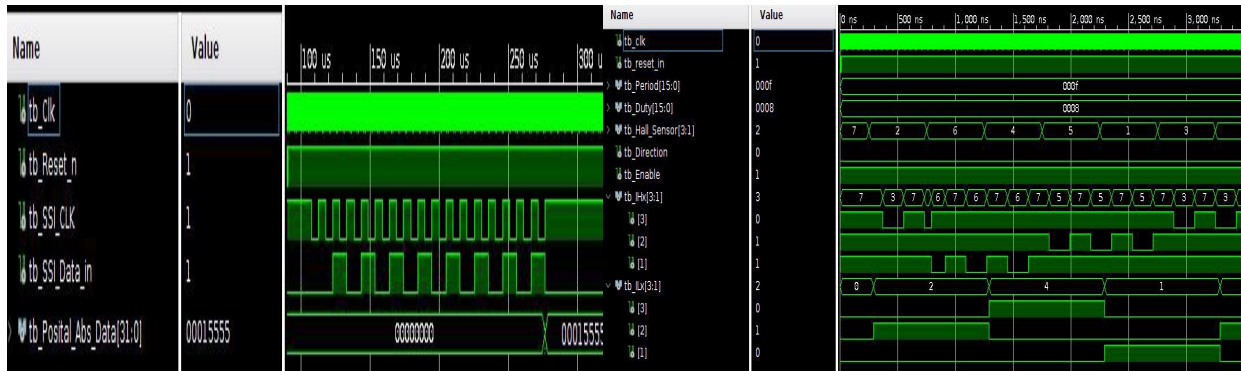


Figure 12. SSI Interface Simulation

Figure 13. BLDC Commutation logic

Each individual peripheral is mapped to a unique address. The "BLDC motor 2" RTL model implemented in Vivado 2017.4 is shown figure 14. SoC HDL design flow can in figure 14. "BLDC motor 2" is an IP block with AXI-Lite interface implemented on programmable logic. This AXI-Lite interface helps ARM processing system to exchange the data with "BLDC motor 2".

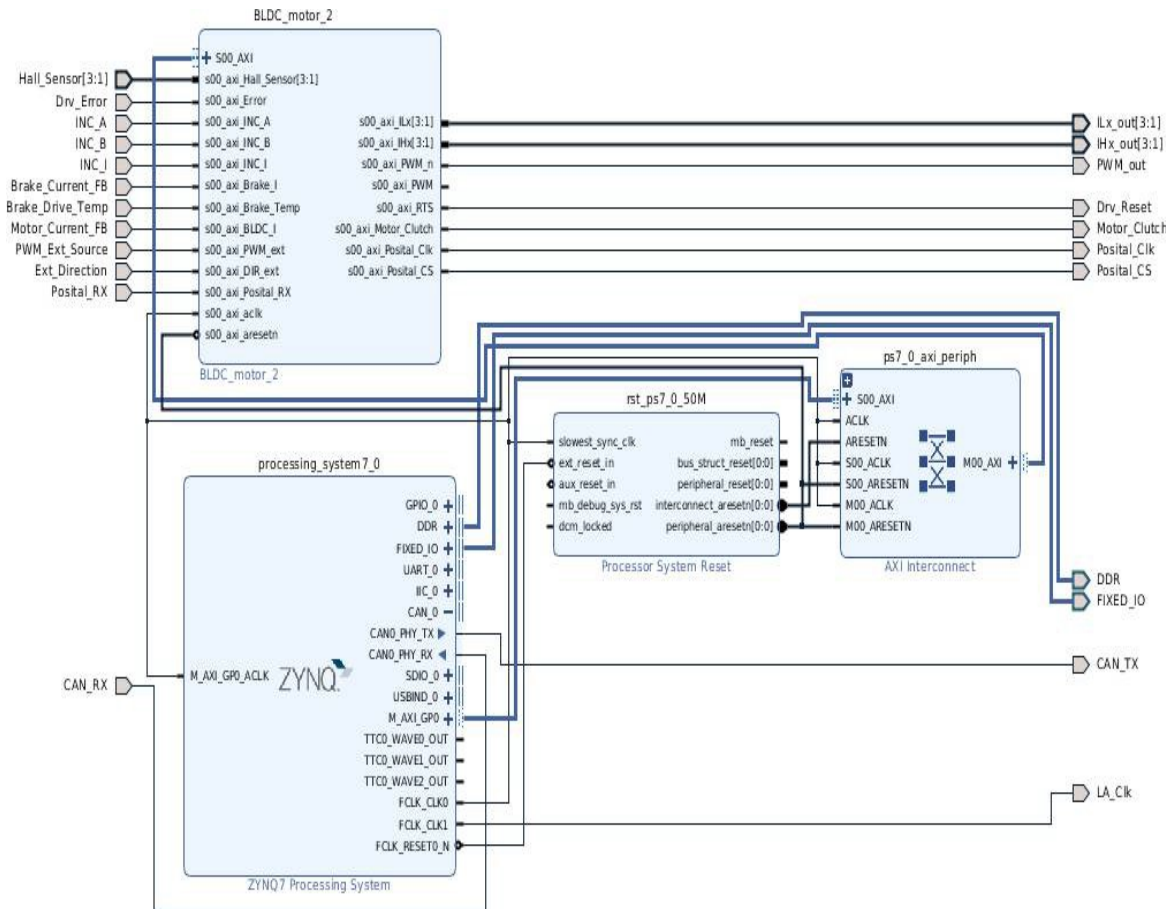


Figure 14. BLDC IP's RTL

4. DISCUSSION

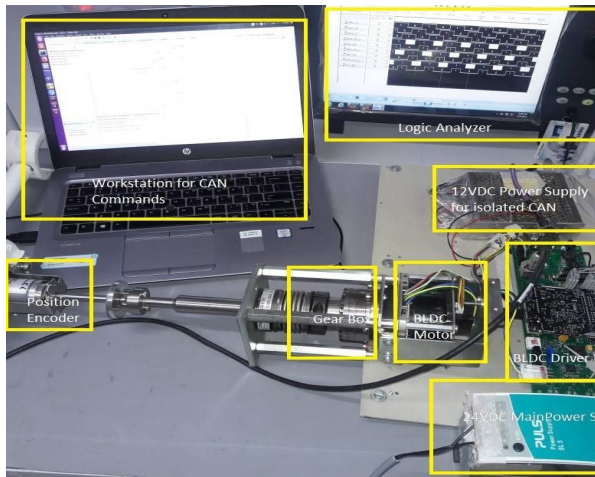


Figure 15. Test Bench Setup

Figure 15 shows the workbench experimental setup which consist of BLDC Driver Board, BLDC motor with quadrature encoder, Gear Box, position encoder, 24V DC main power supply, isolated CAN power, Workstation and Logic Analyzer. Using Xilinx’s SDK, the a 'C' language program was created, compiled and downloaded in the Zynq SoC. The workstation was loaded with the CAN analyser software to transmit the CAN command to the BLDC Driver Board. All the SoC’s peripheral device like 6 six BLDC IC driver signal lines, SSI absolute position encoder and quadrature interface signal are connected to the Logic analyser to observe the waveform. The Logic analyser waveform validated the correctness of the BLDC driver behaviour, position encoder and Quadrature encoder for the speed. The CAN command for the a given PWM was given from the Workstation and the waveform was capture to check if the BLDC Driver’s works correctly. The figure 16 shows the waveform capture on the Logic analyser.

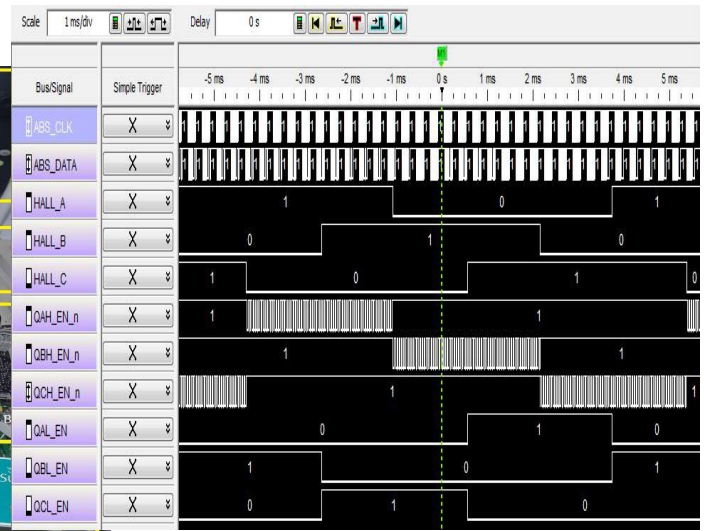


Figure 16. BLDC commutation pattern captured on Logic Analyzer

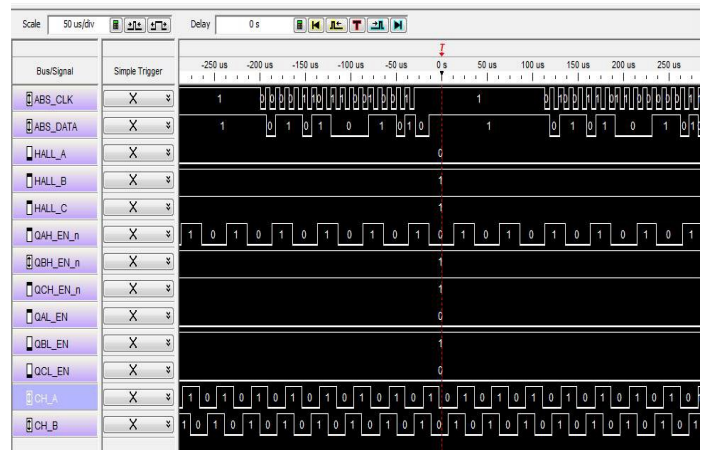


Figure 17. Encoders wave pattern captured on Logic Analyzer

5. CONCLUSION AND FUTURE SCOPE

After observing the control system behaviour control system implementation with fourth order trajectory planning, Zynq SoC and BLDC motor it is concluded that, the control system can accomplish the precise position without any jerk. The result demonstrates that the steady state error largely reduced. Thus, SoC based control system can quite useful in high performance application with high load applications. The model-based approach helps to reduces the cumbersome calculations and trial and errors in controller parameter tuning. Thereby reducing the development time.

REFERENCES:

- [1] Agarwal, Pooja and Arpita Bose. "Brushless Dc Motor Speed Control Using P1roportional-Integral And Fuzzy Controller." IOSR Journal of Electrical and Electronics Engineering 5 (2013), pp. 68-78.
- [2] Balaji, S. R., & Muniraj, C. (2015). Implementation of pi controller for 3 phase BLDC motor drive using FPGA. International Journal of Reconfigurable and Embedded Systems (IJRES) Vol. 4, No. 1, March 2015, pp. 42-54.
- [3] Derammelaere, S, Haemers, M, De Viaene, J, Verbelen, F., & Stockman, K. (2016). A quantitative comparison between bldc, pmsm, brushed dc and stepping motor technologies. In 2016 19th international conference on electrical machines and systems (ICEMS), pp. 1-5.
- [4] Dixon, J., Rodriguez, M., & Huerta, R. (2002). Position estimator and simplified current control strategy for brushless-dc motors, using dsp technology. In Ieee 2002 28th annual conference of the industrial electronics society. IECON 02, Vol. 1, pp. 590-596.
- [5] Ekekwe, N., Etienne-Cummings, R., & Kazanzides, P. (2007). Incremental encoder based position and velocity measurements vlsi chip with serial peripheral inter-face. In 2007 ieee international symposium on circuits and systems, pp. 3558- 3561.
- [6] Ellahi, Nabiya. (2021). Extended Kalman filter based Brushless DC motor for rotor position and speed control. 10.36227/techrxiv.17208848.
- [7] Febin & Jayan, Jestin & Krishna, Mohan & P, Prajof. (2021). DC-link current based position estimation and speed sensorless control of a BLDC motor used for electric vehicle applications. International Journal of Emerging Electric Power Systems. 22. 10.1515/ijeeps-2020-0235.
- [8] Gamazo-Real, Jose-Carlos & Martínez-Martínez, Víctor & Gomez-Gil, Jaime. (2022). ANN-based position and speed sensorless estimation for BLDC motors. Measurement. 188. 10.1016/j.measurement.2021.110602.
- [9] Ghorbel, F. H., Gandhi, P. S., & Alpeter, F. (2001). On the kinematic error in harmonic drive gears. Journal of Mechanical Design, 123 (1), pp. 90-97.
- [10] Gupta, G. S., Mukhopadhyay, S., & Tin, C. M. (2006). A project based approach to teach mixed-signal embedded microcontroller for dc motor control. In Third ieee international workshop on electronic design, test and applications delta'06), pp. 6-10.
- [11] Hanselman, D. C. (1997). Effect of skew, pole count and slot count on brushless motor radial force, cogging torque and back emf. IEE Proceedings- Electric Power Applications, 144 (5), pp. 325-330.
- [12] Hernandez, Isai & Rodriguez, Carlos & Linares Flores, Jesús. (2021). Rotor position estimation in a bldc motor at low speed using g-functions and extended state observers, pp. 1-6.
- [13] Jin, Hao & Liu, Gang & Li, Haitao & Zhang, Haifeng. (2021). Closed-loop Compensation Strategy of Commutation Error for Sensorless BLDC Motors with Non-ideal Asymmetric Back-EMFs. IEEE Transactions on Power Electronics, pp. 1-11.
- [14] Khosravipour, Amirhossein. (2020). Increasing the efficiency of brushless motors (BLDC) and examining optimization methods. 10.13140/RG.2.2.20567.50083.
- [15] Koinakov, G., Dunchev, L., & Furnadziev, V. (1984, 09). A method for real time numerical integration. Microprocessing and Microprogramming , pp. 79-83.
- [16] Koutroulis, E., Dollas, A., & Kalaitzakis, K. (2006). High-frequency pulse width modulation implementation using fpga and cpld ics. Journal of systems architecture, 52 (6), pp. 332-344.
- [17] Lambrechts, P., Boerlage, M., & Steinbuch, M. (2004). Trajectory planning and feedforward design for high performance motion systems. In Proceedings of the 2004 american control conference, Vol. 5, pp. 4637-4642.
- [18] Manoj. Kumar. (2020). Comparison of single loop and Cascade loop control of bldc motor drive. i-manager's Journal on Electrical Engineering. 13. 38. 10.26634/jee.13.3.16858.
- [19] Merry, R., van de Molengraft, R., & Steinbuch, M. (2007). Error modelling and improved position estimation for optical incremental encoders by means of time stamping. In 2007 american control conference pp. 3570-3575.
- [20] Nguyen, K. D., Ng, T.-C., & Chen, I.-M. (2008). On algorithms for planning s-curve motion profiles. International Journal of Advanced Robotic Systems, 5 (1), pp. 1-11.
- [21] Nov'ak, P. (2001). Ssi-interface and protocol for industrial sensors. In Xxvi asr 2001 seminar on instruments and control, pp. 370-373.

- [22] Papathanasopoulos, Dimitrios & Mitronikas, Epaminondas. (2019). Diagnosis of Defective Hall-effect Position Sensors in Brushless DC Motor Drives, pp.137-142.
- [23] Park, J. S., Gu, B.-G., Choi, J.-H., & Jung, I.-S. (2011). Development of bldc motor drive for automotive water pump systems. Journal of International Council on Electrical Engineering , 1 (4), pp. 395–399.
- [24] Park, S. J., Park, H. W., Lee, M. H., & Harashima, F. (2000). A new approach for minimum-torque-ripple maximum-efficiency control of bldc motor. IEEE Transactions on Industrial Electronics, 47 (1), pp. 109–114.
- [25] Pongswatd, S., Chaikla, A., Ukakimapurn, P., & Tirasesth, K. (2007). Digital tech- nique to generate variable and multiple pwm signals. In Second international conference on innovative computing, informatio and control (icicic 2007), pp. 457–467
- [26] Ramesh, M., Rao, G. S., Amarnath, J., Kamakshaiyah, S., & Jawaharlal, B. (2011). Speed torque characteristics of brushless dc motor in either direction on load using arm controller. In Isgt2011-india, pp. 217–222.
- [27] Reddy, B. P., & Murali, A. (2016). Soc fpga-based field oriented control of bldc motor using low resolution hall sensor. In Iecon 2016-42nd annual conference of the ieeec industrial electronics society, pp. 2941–2945.
- [28] Rodríguez-Molina, Alejandro & Villarreal-Cervantes, Miguel & Serrano- Perez, Omar & Solís-Romero, José & Silva-Ortigoza, Ramón. (2022). Optimal Tuning of the Speed Control for Brushless DC Motor Based on Chaotic Online Differential Evolution. Mathematics. 10. 1977. 10.3390/math10121977, application symposium, pp. 133-136.
- [29] Sankar, A. B., & Seyezhai, R. (2014). Simulation and implementation of sensed control of three-phase bldc motor using fpga. In 2014 international conference on science engineering and management research (icsemr), pp. 1–5.
- [30] Sathyan, A., Milivojevic, N., Lee, Y.-J., Krishnamurthy, M., & Emadi, A. (2009). An fpga-based novel digital pwm control scheme for bldc motor drives. IEEE transactions on Industrial Electronics, 56 (8), pp. 3040–3049.
- [31] Sen, Aryadip & Singh, Bhim. (2021). : Peak Current Detection Starting based Position Sensorless Control of BLDC Motor Drive for PV Array Fed Irrigation Pump. IEEE Transactions on Industry Applications. PP. 1-10.
- [32] Shrutika, C. & Matani, Sahil & Chaudhuri, Siddhartho & Gupta, Atul & Gupta, Shishir & Singh, Navdeep. (2021). Back-EMF estimation based sensor less control of Brushless DC motor, pp. 1-6.
- [33] Tashakori, A., Hassanudeen, M., & Ektesabi, M. (2015). Fpga based controller drive of bldc motor using digital pwm technique. In 2015 ieeec 11th international conference on power electronics and drive systems, pp. 658–662.
- [34] Yang, G., Ye, Z., Pan, Y., & Ma, Z. (2013). The implementation of s-curve acceleration and deceleration using fpga. TELKOMNIKA Indonesian Journal of Electrical Engineering, 11 (1), pp. 101-110.