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REDUCED COMPONENTS MULTILEVEL INVERTER TOPOLOGY

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ABSTRACT

This paper presented a new low-component-count multilevel inverter. The generalized structure of the proposed topology is formed via cascading, and it is found to improve output voltage level count. It is possible to use the developed structure of the proposed topology with either asymmetrical or symmetrical values of DC source voltages. Binary configuration is employed to choose the values of DC source voltages. Third harmonic injection sinusoidal pulse width modulation technique is adopted to create gating signals for the presented topology. Comparative analysis of the presented topology shows the best performance in DC sources. The switch count and low blocking voltage on the switches make this topology more cost effective compared to certain other topologies in the extant literature. Losses analysis for the presented topology was shown. MATLAB/SIMULINK is employed to carry out the simulation. The presented topology is validated using a prototype designed to create a 7-level output voltage.

Keywords: *Modeling Of Switching Pulses, POD Technique, Symmetrical And Asymmetrical Multilevel Inverter, Selection Of DC Sources.*

1. INTRODUCTION

Power converters from DC to AC are commonly known as inverters. Inverters find diverse application in driver control, power supplies, electric vehicles, HVDC transmission, and renewable energy systems [1], [2]. Huge demand of electric power and depletion of non-renewable resources paying way to the utilization of renewable energy resources such as wind, solar [3]. Traditional inverters create output voltage of square-wave shape with two levels, one in the positive level and another in the negative level. The THD, dv/dt and voltage burden on the switches are very high in two-level inverters. These problems can be overcome with multilevel inverters (MLI'S) in which output voltage waveform having more than three-level. Output voltage in the multilevel inverters can be synthesized from many input sources that produce staircase waves with minimum harmonic distortion, while high voltage can be generated using low rated power devices. Improved performance and cost effectiveness are the most attractive features of MLIs to researchers in the field.

The most popular MLI among the different classical MLIs [4] is the cascaded H-bridge (CHBMLI). It has fewer switching components and does not require flying capacitors (or) clamping diodes. CHBMLIs are used in several industrial sectors to control pumps, compressors, fans etc. MLIs have two configurations: symmetrical and asymmetrical [23]. Symmetrical MLIs have DC sources values of similar magnitude, while asymmetrical MLIs have DC sources values of dissimilar magnitudes. Greater output voltage levels can be achieved with fewer components when using asymmetrical MLI rather than symmetrical MLI.The topology presented in [5] posited MLI with fewer switches and sources and two algorithms to decide the DC source values. In [6] a topology was suggested with less switch count compared to traditional inverters , power losses and total peak inverse voltage (PIV) is less. In [7] a submultilevel inverter was presented, the series connection of submultilevel inverters produce the multilevel output voltage. Submultilevel inverter and series connection create only zero and positive levels of output voltage, an H-bridge used to create negative levels of output voltage. In [8], a topology with module connection was presented. Each module was made with two isolated DC sources, H and half bridges. A topology in [9] formed by semi half bridge cells connected in a crisscross manner to

the load to generate levels in the output voltage. The optimized structure is shown with reduced components. The switching pulses for the given topology was created by phase displaced pulse width modulation technique (PDPWM). A single DC source with a transformer [12] was used to develop the topology, which gives multilevel output with symmetrical and asymmetrical configurations. In [13], two T-connections were connected back to back by switches to provide a new structure that allows for more levels in output. In this structure different paths were created to DC sources to avoid H-bridge for polarity generation. The presented basic unit of MLI in [17] consisted of three DC sources and five unidirectional switches. By cascading basic units, levels in the output voltage could be boosted. A separate DC source with two switches is connected to create output voltage minimum level.

The present paper contributes to extant research in the following aspects:

1. With reduced switch count a new topology was presented.

2. Number of switches, sources, and the cost function are compared to the number of levels. It presents the best results compared to a few other presented topologies in the literature.

The structure of the paper is as follows: In section 2, a novel topology is presented, and cascading is shown to improve the levels in the output. In section 3, binary sequence algorithm is presented to decide the values of the DC voltage sources. Third harmonic injection technique with Phase Opposition and Disposition carrier signal is used to generate switching pulses, presented in section 4. In section 5, the voltage blocked by each switch is calculated to determine the switches rating. Section 6 is comparison between the presented topology and some conventional topologies in terms of switches, DC sources and blocking voltage. Section 7 details the calculation of conduction and switching losses. Section 8 delineates the simulation and hardware results. Finally, the section 9 presents the conclusion of this research.

2. PRESENTED TOPOLOGY

The presented topology as depicted in Fig.1 can create output voltage as shown in Table I. Basic unit consist of five unidirectional switches (S_1, S_2, S_3, S_4 and S_5), two DC voltage sources(V_{K1}, V_{K2}) and H-bridge is used for polarity generation, consist of four unidirectional switches (S_A, S_B, S_C and S_D). The H-bridge is not a part of basic unit. Switches in the topology are IGBT's with antiparallel diodes. In Table 1, the switching states of the presented topology, it create three output levels 0, VK1, VK2 and (VK1 + VK2). To generate zero level three redundant states are possible. The basic unit is able of creating only positive output voltage levels and the negative levels in output voltage i.e -VK1, -VK2 and - (VK1 + VK2) can be created using H-bridge. Switches of the H-bridge should withstand high voltage and they will be operating in the fundamental switching frequency. Make sure that switches S2, S3 and S5 should not turn on at same time instant to avoid short circuiting risk of V_{K1}. Similarly, switches S_1, S_3 and S_4 should not turn on at same time instant to avoid short circuiting risk of V_{K2}.

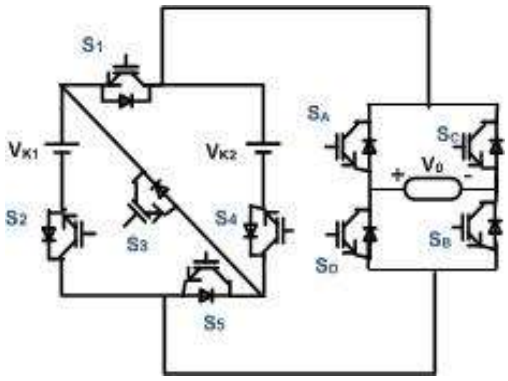

Fig.1 Structure of presented topology

For the presented topology, count of switches

$$N_{SW} = 5K + 4 \quad (1)$$

Count of DC sources

$$N_{DC} = 2K \quad (2)$$

Table 1. Switching states of 7-level output voltage with one basic unit and H-bridge.

Output Voltage (Vo)	+Vo/-Vo Switching States
0	S_5,S_3,S_1,S_A,S_B (or) S_A, S_B (or) S_C, S_D
+/- (VK1)	S_1,S_2,S_A,S_B / S_1,S_2,S_C,S_D
+/- (VK2)	S_4,S_5,S_A,S_B/ S_4,S_5,S_C,S_D
+/-(VK1+VK2)	S_2,S_3,S_4,S_A,S_B/ S_2,S_3,S_4, S_C,S_D

Fig.2 illustrates, basic units connection in cascaded fashion to improve levels count in the

output voltage. Table 2 shows the switching states for the presented topology with two basic units are cascaded.

Sum of the voltages across each basic topology gives output voltage of multilevel inverter.

$$V_{0(t)} = V_{1(t)} + V_{2(t)} + \cdots + V_{K(t} \quad (3)$$

where $V_{1(t)}$ is output voltage across first basic unit.$V_{2(t)}$ is output voltage across second basic unit. $V_K(t)$ is output voltage across p^{th} basic unit.

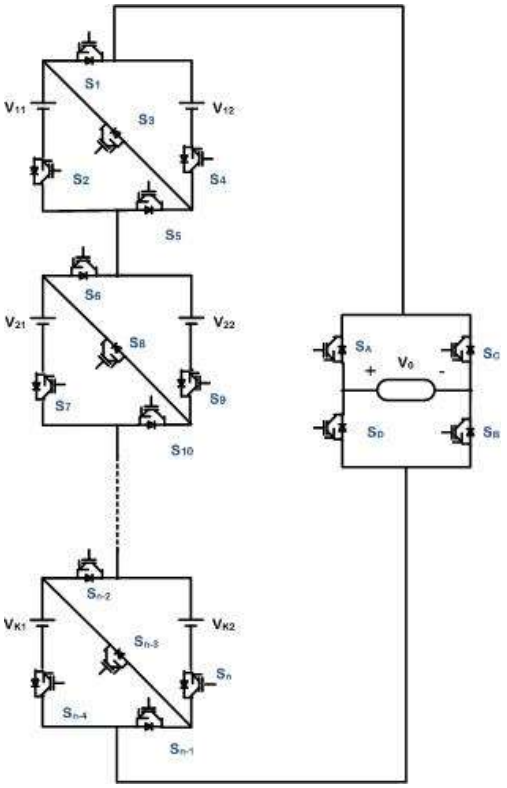

Fig.2 Cascaded presented topology

3. CHOOSING MAGNITUDE OF DC SOURCES

The DC voltage sources for a MLI's plays a major role in deciding levels in output voltage. For all topologies, the value of DC sources to reach the maximum levels in the output voltage may not be the same. Symmetrical and asymmetrical configuration are available in the literature [10-12], [14], [22], [24] to decide the DC sources voltage values. Output levels can be generated using either symmetric or asymmetric DC source configurations with the presented topology. The selection of DC source values in symmetrical configuration with unary sequence is determined as

$$V_{Ki} = V_{dc}\,; i = 1,2 \quad (4)$$

Output voltage maximum value for the presented topology with unary sequence is given as

$$V_{0max} = \sum_{i=1}^{p} V_{dci} = p \times V_{dc} \quad (5)$$

where 'p' is the DC source count. The levels count in the output voltage is given as

$$N_L = 2 \times \left(\frac{V_{0max}}{V_{dc}}\right) + 1 = (2 \times p) + 1 \quad (6)$$

The DC source values in asymmetrical configuration with binary sequence is given as

$$V_{Ki} = 2^{(m-1)} \times V_{dc}\,; i = 1,2 \quad m = 1,2,--p \quad (7)$$

Output voltage maximum value with binary sequence algorithm for the presented topology is given as

$$V_{0max} = \sum_{i=1}^{p} V_{dci} = (2^p - 1) \times V_{dc} \quad (8)$$

The levels count in the output voltage is given as

$$N_L = 2 \times \left(\frac{V_{0max}}{V_{dc}}\right) + 1 = 2^{(p+1)} - 1 \quad (9)$$

4. MODULATION TECHNIQUE

Switching pulses to an inverter can be created by comparing carrier signals with the reference signal. Many modulation schemes are available in the literature [13][15]. Third Harmonic Injected Modulation technique (THI) with Phase Opposition Disposition (POD) scheme was used to determine switching pulses to the inverters switches which is shown in Fig.3. The switching pulses are mathematically modelled for 7-level output in the presented topology [23] [25].

Table 2. 31-level output voltage switching states for the presented topology with two basic units and H-bridge.

Output voltage(Vo)	+Vo/-Vo Voltage switching states
0 V	$S_4,S_2,S_3,S_A,S_B,S_9,S_7,S_8$ (or) S_A,S_C(or)S_B,S_D
+/- 1V (VK1)	$S_{10},S_8,S_6,S_2,S_1,S_A,S_B$ / $S_{10},S_8,S_6,S_2,S_1,S_C,S_D$
+/- 2V(VK2)	$S_{10},S_8,S_6,S_5,S_4,S_A,S_B$/ $S_{10},S_8,S_6,S_5,S_4,S_C,S_D$
+/- 3V(VK1+VK2)	$S_{10},S_8,S_6,S_3,S_2,S_4,S_A,S_B$/ $S_{10},S_8,S_6,S_3,S_2,S_4,$ S_C,S_D
+/- 4V(VK3)	$S_{10},S_9,S_5,S_3,S_1,S_A,S_B$/$S_{10},S_9,S_5,S_3,S_1,S_C,S_D$
+/- 5V (VK1+VK3)	$S_{10},S_9,S_2,S_1,S_A,S_B$ / $S_{10},S_9,S_2,S_1,S_C,S_D$
+/- 6V (VK2+VK3)	$S_{10},S_9,S_5,S_4,S_A,S_B$ / $S_{10},S_9,S_5,S_4,S_C,S_D$
+/- 7V (VK1+VK2+VK3)	$S_{10},S_9,S_3,S_1,S_4,S_A,S_B$/ $S_{10},S_9,S_3,S_1,S_4,S_C,S_D$
+/- 8V (VK4)	$S_7,S_6,S_5,S_3,S_1,S_A,S_B$ / $S_7,S_6,S_5,S_3,S_1,S_C,S_D$
+/- 9V (VK1+VK4)	S_7,S_6,S_2,S_1,S_A,S_B / S_7,S_6,S_2,S_1,S_C,S_D
+/- 10V (VK2+VK4)	S_7,S_6,S_5,S_4,S_A,S_B / S_7,S_6,S_5,S_4,S_C,S_D
+/- 11V (VK1+VK2+VK4)	$S_7,S_6,S_3,S_2,S_4,S_A,S_B$ / $S_7,S_6,S_3,S_2,S_4,S_C,S_D$
+/- 12V (VK3+VK4)	$S_7,S_9,S_8,S_5,S_3,S_1,S_A,S_B$/ $S_7,S_9,S_8,S_5,S_3,S_1,$ S_C, S_D
+/- 13V (VK1+VK3+VK4)	$S_7,S_9,S_8,S_2,S_1,S_A,S_B$ / $S_7,S_9,S_8,S_2,S_1,S_C,S_D$
+/- 14V (VK2+VK3+VK4)	$S_7,S_9,S_8,S_5,S_4,S_A,S_B$ / $S_7,S_9,S_8,S_5,S_4,S_C,S_D$
+/- 15V (VK1+VK2+VK3+VK4)	$S_7,S_9,S_8,S_2,S_3,S_4,S_A,S_B$ / $S_7,S_9,S_8,S_2,S_3,S_4,$ S_C,S_D

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$$S_{1P} = a_1 - a_2 \quad (10)$$

$$S_{2p} = a_1 - a_2 + a_3 \quad (11)$$

$$S_{3p} = a_3 \quad (12)$$

$$S_{4p} = a_2 \quad (13)$$

$$S_{5P} = a_2 - a_3 \quad (14)$$

The suffix 'p' in (10) to (14) represents pulses generated during positive half cycle. Negative half cycle pulses are created in the same way using (15) to (19).

$$S_{1n} = a_{-1} - a_{-2} \quad (15)$$

$$S_{2n} = a_{-1} - a_{-2} + a_{-3} \quad (16)$$

$$S_{3n} = a_{-3} \quad (17)$$

$$S_{4n} = a_{-2} \quad (18)$$

$$S_{5n} = a_{-2} - a_{-3} \quad (19)$$

The switching pulse to be given to the particular switches is given by

$$S_1 = S_{1p} + S_{1n} \quad (20)$$

$$S_2 = S_{2p} + S_{2n} \quad (21)$$

$$S_3 = S_{3p} + S_{3n} \quad (22)$$

$$S_4 = S_{4p} + S_{4n} \quad (23)$$

$$S_5 = S_{5p} + S_{5n} \quad (24)$$

$$S_A = S_B = a_1 \quad (25)$$

$$S_C = S_{1D} = a_2 \quad (26)$$

In general, the mathematical modelling for switching pulses for 'N' level inverter is given as

$$S_{1p} = a_1 - \sum_{n=1}^{K} (a_{2(2n-1)} - a_{4n}) \quad (27)$$

$$S_{2p} = \sum_{n=1}^{K} (a_{2n-1} - a_{2n}) \quad (28)$$

$$S_{3p} = \sum_{n=1}^{K} (a_{4n-1} - a_{4n+1}) \quad (29)$$

$$S_{4p} = \sum_{n=1}^{K} (a_{4n-2} - a_{4n}) \quad (30)$$

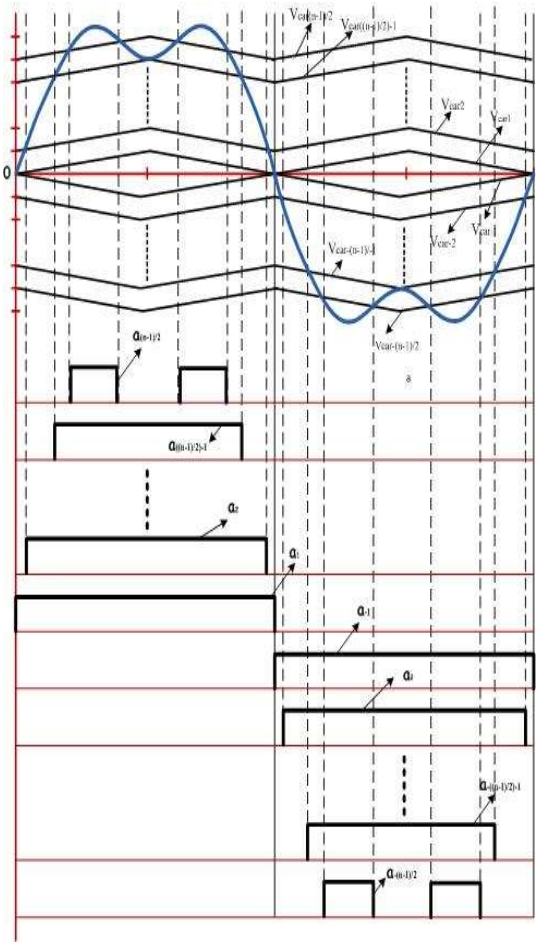

Fig 3. Gating pulses generation by comparing reference and carrier signal

$$S_{5p} = \sum_{n=1}^{K} (a_{2n} - a_{2n+1}) \quad (31)$$

$$S_{6p} = a_1 - \sum_{n=1}^{K} \left(a_{4(2n-1)} - a_{8n}\right) \quad (32)$$

$$S_{7p} = \sum_{n=1}^{K} \left(a_{8(2n-1)} - a_{16n}\right) \quad (33)$$

$$S_{8p} = a_1 - \sum_{n=1}^{K} \left(a_{4(4n-3)} - a_{4(4n-1)}\right) \quad (34)$$

$$S_{9p} = \sum_{n=1}^{K} \left(a_{4(2n-1)} - a_{8n}\right) \quad (35)$$

$$S_{10p} = a_1 - \sum_{n=1}^{K} \left(a_{8(2n-1)} - a_{16n}\right) \quad (36)$$

$$S_A = S_B = a_1 \quad (37)$$

Positive pulses for the switches can be generated using (28) to (36). The negative pulses for the switches can be obtained by

$$S_{1n} = S_{1p} \times a_{-1} \quad (38)$$

$$S_C = S_D = a_{-1} \quad (39)$$

The condition considered to derive the negative pulses from the positive pulses is given by

$$a_m \times a_{-1} = a_{-m} \quad (40)$$

Combination of positive pulses and negative pulses gives the complete gate pulses for the switches

$$S_1 = S_{1p} + S_{1n} \quad (41)$$

The complete gate pulse for the switch S_1 is given by (41). Equations similar to (41) can be derived for the remaining switches.

5. BLOCKING VOLTAGE ON THE SWITCHES

The MLI switches were chosen based on their blocking voltages and ON state currents, which have an impact on the inverter cost. The ON state current is determined by the load, and the topology has no bearing on it. The blocking voltage, on the other hand, is entirely determined by the inverter's construction and topology. The goal of the research is to create topologies with the lowest overall blocking voltage possible. Blocked voltage maximum value on the switch is the main parameter in determining the cost of the switch. If the total blocking voltage on the switch is decreased, the inverter's overall costs will also decrease [16], [20], [21]. Therefore to calculate this index, blocking voltage on each switches is necessary. Considering Fig.1, and the binary sequence algorithm to determine DC sources, the voltage blocked by the each switch is given as

$$VS_1 = \frac{V_{11}}{2} \quad (42)$$

$$VS_2 = VS_4 = VS_5 = V_{11} \quad (43)$$

$$VS_3 = VS_{12} \quad (44)$$

$$VS_A = VS_B = VS_C = V_{SD} = V_{11} + V_{12} \quad (45)$$

For the presented topology, the complete blocking voltage by all the switches is given by

$$V_{block} = VS_1 + VS_2 + VS_3 + VS_4 + VS_5 + VS_A + VS_B + VS_C + VS_D \quad (46)$$

6. PROPOSED TOPOLOGY COMPARISON WITH FEW EXISTING TOPOLOGIES.

The major goal of designed cascaded inverters is to achieve maximum level counts in the output voltage while employing fewer components. By decreasing the count of various components like switches, gate drivers and DC sources leads to lower cost, smaller size and simple control. Table 3

shows the relations used to draw comparisons between the proposed topology and some existing MLI topologies. The graphs for the number of switches, number of sources and cost function are plotted in terms of the number of levels based on these derived relations. The DC voltage source values in this study are chosen using a binary algorithm

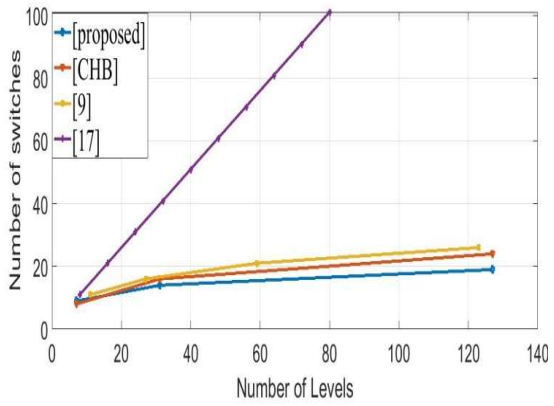

Fig 4. Comparison of switches against levels

Fig.4 illustrate , the variation of switches with levels . The presented topology showed good advantage with reduced switches than the considered topologies. In the presented topology all the switches are unidirectional.

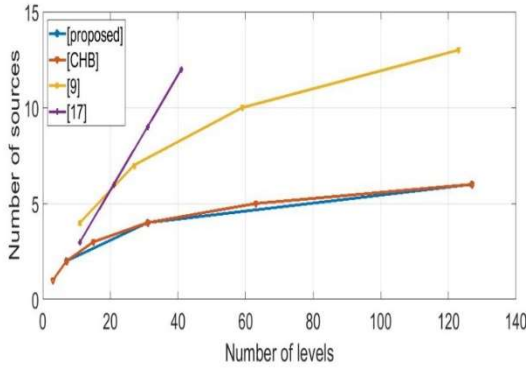

Fig 5. Comparison of switches against sources.

As shown in Fig. 5, presented topology requires less sources with less switches than the considered topologies , but the number of sources for the particular levels is same for the presented topology and cascaded H-bridge. Each basic unit of the presented topology requires two sources. The decrease of count in DC sources and switches decreases the volume and cost of the inverter.

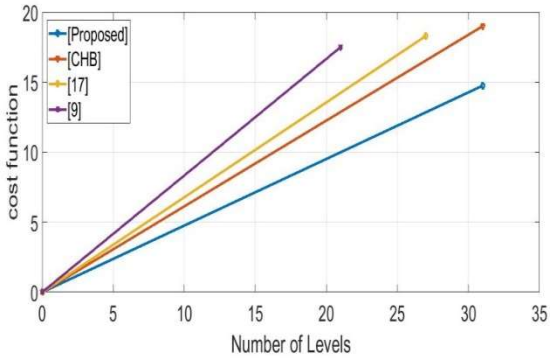

Fig 6. Comparison of cost function against levels.

The cost function plays major role in deciding the overall cost of the topology. The cost function is defined in [18], [19] and expressed as shown in (47):

$$CF = N_{IGBT} + \alpha V_{block}^{pu} = N_{IGBT's} + \alpha \left(\frac{V_{Block}}{V_{max}}\right) \quad (47)$$

The 'α' in (47) is an important variable quantity calculated as the weight factor of blocked voltage versus number of IGBTs [18], [19], [20]. In general, the magnitude of blocked voltage will be essential if 'α' is more than one, while the number of IGBTs and their respective prices will be important if 'α' is less than one.

The cost function against the number of levels, as depicted in Fig. 6, for α = 0.5 and k=1 shows that the presented topology is more cost effective than the other considered topologies. 'α' is choosen as 0.5 to give priority to the number of IGBTs in determining the cost function. According to the aforementioned comparisons, the presented architecture requires fewer switches and fewer DC sources, resulting in a lower cost function and less installation area to create certain levels of output voltage.

7. LOSSES CALCULATION

The sum of power losses in semiconductor devices accounts for the total losses in an MLI. Losses in a semiconductor device occur due to conduction and switching. The current flow through the switch during the 'on' state creates conduction loss. A switch in the proposed topology contains IGBT and diode. So, loss in IGBT ($P_{cond,IGBT}$) and anti-parallel diode($P_{cond,D}$) gives the total

conduction losses in switch. Generally, it can be obtained as follows [18-19]:

$$P_{cond,IGBT} = \left[V_{ON,IGBT} + R_{ON,IGBT}\, i^{\beta}(t)\right] i(t) \quad (48)$$

$$P_{cond,D} = \left[V_{ON,D} + R_{ON,D}\, i(t)\right] i(t) \quad (49)$$

The voltage drops of an IGBT and a diode in 'on' states are represented by $V_{ON,\ IGBT}$ and $V_{ON,D}$, respectively. The on-state resistance of IGBT and diode are represented by $R_{ON,IGBT}$ and $R_{ON,D}$ respectively. β is a constant of an IGBT, and, in general, it is considered close to 0.5.

The proposed inverter's average conduction loss is calculated as

$$P_C = \frac{1}{\pi}\int_0^{\pi} \left(N_{IGBT}(t) \times P_{cond,IGBT}(t) + N_D(t) \times P_{cond,D}(t)\right) d(\omega t) \quad (50)$$

$N_{IGBT}(t)$ and $N_D(t)$ are the 'on' state IGBT's number and diodes number in the current path.

During switching period turn-on and turn-off, switching losses can be obtained. linear approximation is used to calculate switching losses. During turn on period, turn off period of the switch, energy loss can be obtained as

$$E_{ON} = \int_0^{T_{ON}} V(t) i\,(t)$$

$$= \int_0^{T_{ON}} \left[\left(\frac{Vt_S}{T_{ON}}\right)\left(-\frac{I(T-T_{ON})}{T_{ON}}\right)\right] d(t)$$

$$= \frac{V_{IGBT}.I.T_{ON}}{6} \quad (51)$$

$$E_{OFF} = \int_0^{T_{OFF}} V(t) i(t)$$

$$= \int_0^{T_{OFF}} \left[\left(\frac{Vt_S}{T_{OFF}}\right)\left(-\frac{I(T-T_{OFF})}{T_{OFF}}\right)\right] d(t)$$

$$= \frac{V_{IGBT}.I.T_{OFF}}{6} \quad (52)$$

Where E_{ON} and E_{OFF} are the switch's on and off period energy loss. Cross over interval times of switches are T_{ON} and T_{OFF}. Before and after turn on voltage across the switch is V_{IGBT}. Current flow through switch before and after turn on is I.

Switching power loss can be calculated as follows, if there are N_{ON} number of turn-on's and N_{OFF} number of turn-off's of switches during fundamental cycle T:

$$P_{SW} = (N_{ON}E_{ON} + N_{OFF}E_{OFF}) \quad (53)$$

In an MLI, the total loss can be obtained as

$$P_{Loss} = P_{cond,IGBT} + P_{Cond,D} + P_{SW} \quad (54)$$

Inverter efficiency can be calculated as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (55)$$

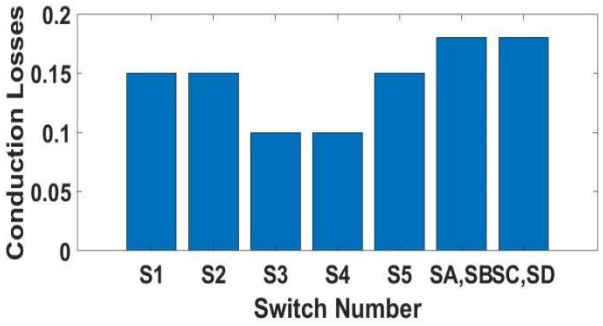

Fig 7. Conduction losses for proposed topology

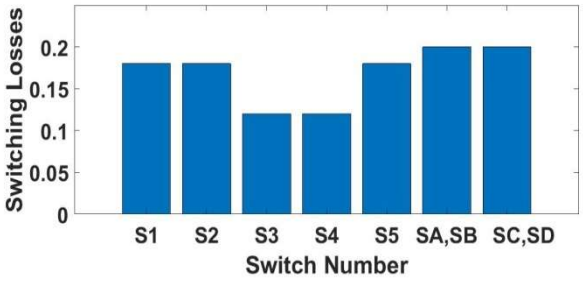

Fig 8. Switching losses for the proposed topology.

8. RESULTS

Results are confirmed in MATLAB/SIMULINK environment and experimentally validated. Simulation and hardware settings for Fig. 1 are as follows: L=55 mH, R=40 ohms.

SIMULATION RESULTS

When one basic unit is configured in a symmetrical uninary manner, as illustrated in Fig. 1 of proposed system, 5-levels occur in the output voltage, with each level as 100 Volt. Output voltage maximum amplitude is V = 200 Volts. Among 5-level output voltage as shown in Fig.9, positive half cycle has two levels, negative half cycle has two levels and one level at zero reference. With each level as 100 Volt.

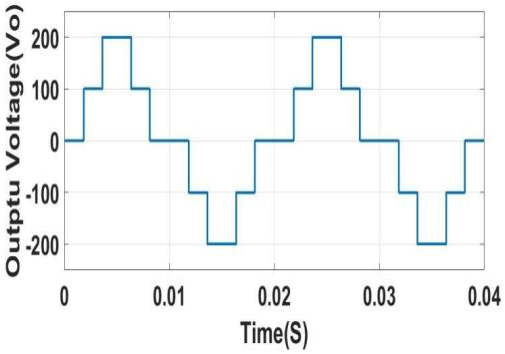

Fig 9. 5-level output voltage for symmetrical configuration.

A Binary sequence algorithm is utilised to find DC sources with Asymmetrical configuration. The DC source values in simulation are V1=100V, V2=200V. The output voltage has a peak amplitude of 300V. Among the 7-level output voltage as shown in Fig.10, positive half cycle has three levels, negative half cycle has three levels and one level at zero reference. with each level as 100 Volt.

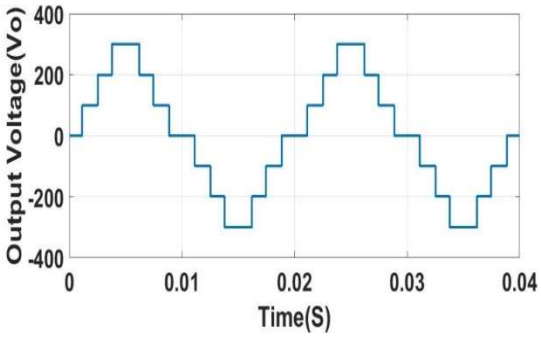

Fig. 10 7-level output for symmetrical configuration.

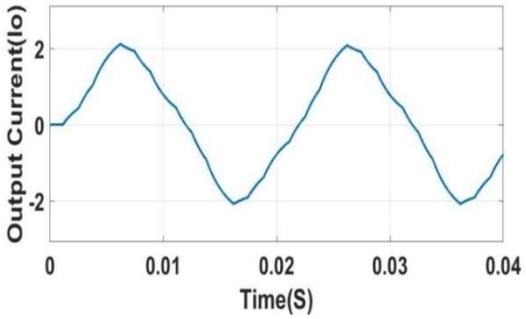

Fig 11. Output current of proposed topology.

Fig. 11 illustrates the output current. It is almost sinusoidal in nature due to the low pass filter behaviour of RL load. The phase delay in the output current is due to inductance in the load.

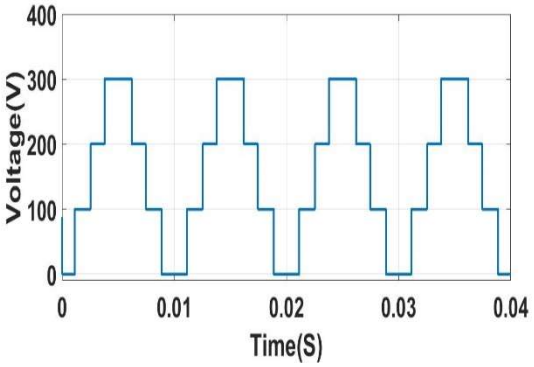

Fig 12. Output across basic unit of proposed topology.

Figure.12 depicts the output voltage level generation portion of the presented topology's basic unit. In the presented topology, the H-bridge is used to create polarities in the output with positive and negative cycles.

Fig.13 and Fig.14 depicts output voltage levels for modulation index of m=0.89 and m=0.7. In the case of m=0.7 the number of levels were decreased to 5-levels, even though the topology having the same parameters to the modulation index of m=0.89 .

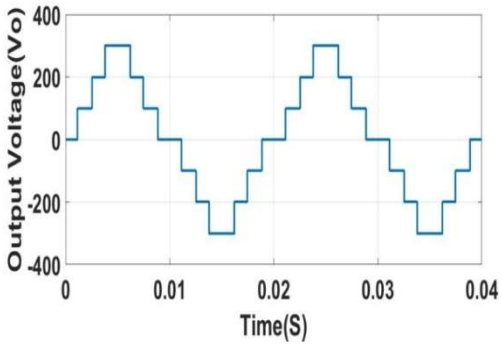

Fig 13. 7-level voltage output for modulation index 0.89.

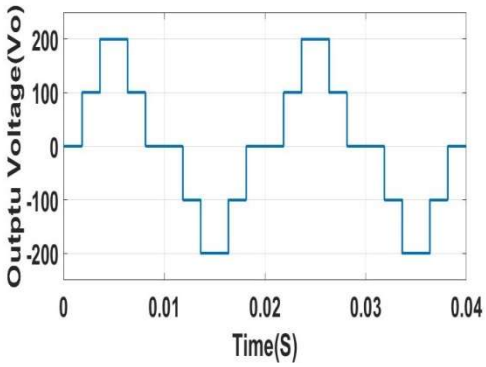

Fig 14. 5-level output voltage for modulation index 0.7.

When cascading two basic units as illustrated in Fig.2, the output voltage levels are depicted in Fig.15. The DC voltage source values in the simulation are V1=10, V2=20V, V3=40V and V4=80V. Output voltage has a peak amplitude of 150V. Among 15-levels output voltage as shown in Fig.13, positive half cycle has seven levels, negative half cycle has 7-levels and one level at zero reference.

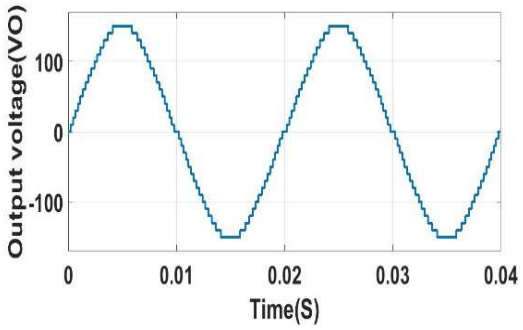

Fig 15. 31-level output voltage for two basic unit cascaded

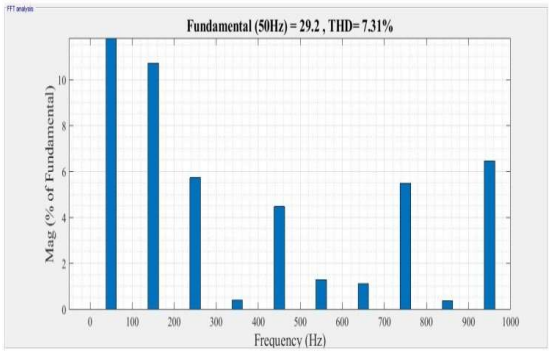

Fig 16. Output voltage THD spectrum

Fig. 16, shows harmonic spectrum of output voltage for the proposed topology under asymmetrical case (7-level) with one basic unit (n=1).

Experimental results

The experimental configuration of the proposed system to create output voltage of 7-level is shown in Fig. 17. It was created based on Fig. 1. The magnitude of DC source values are Vdc1=10 and Vdc2=20. The experimental setup consist of IGBT switches for basic unit and H-bridge. The IGBTs used in the basic circuit and H-bridge prototypes include (FGA25N120), a gate drive circuit (TLB250) and an FPGA processor make up the experimental configuration. To generate switching pulses for the IGBTs, the SPARTAN 6 XILINX FPGA processor is used.

Fig 17. Experimental setup of proposed 7-level inverter

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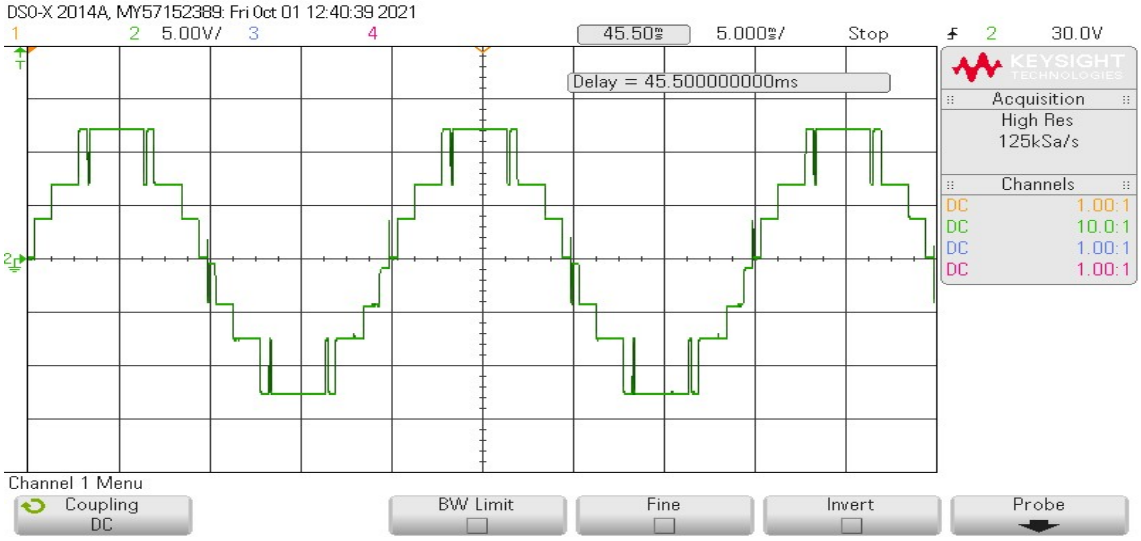

Fig 18. 7-Level Inverter Hardware Output Voltage With One Basic Unit And H-Bridge.

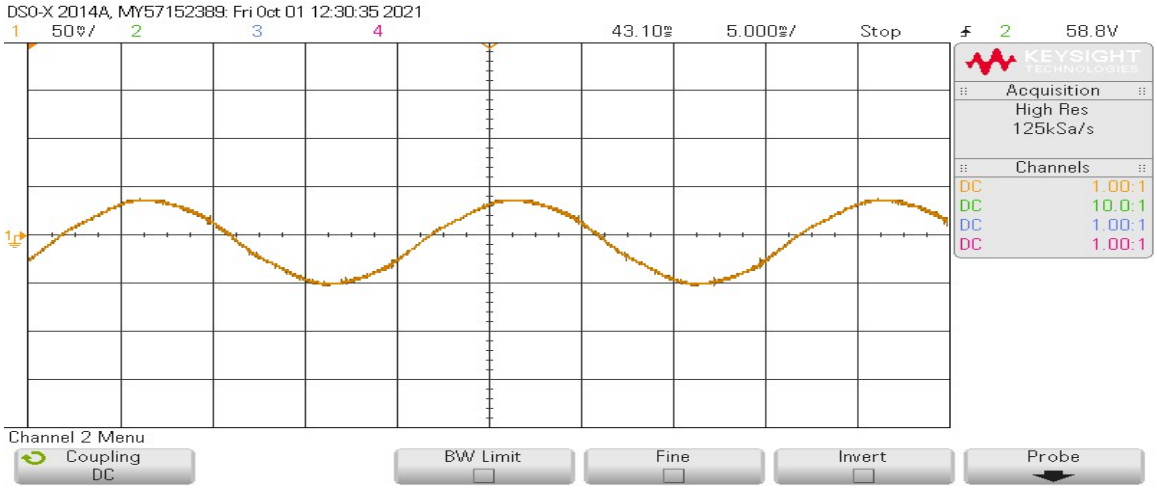

Fig 19. 7-Level Inverter Hardware Output Current With One Basic Unit And H-Bridge.

Fig. 18 shows the experimental results of hardware setup with a 7-level output voltage; the positive and negative halves have three levels each and one level is at zero. The current waveform of a 7-level inverter is shown in Fig. 19. The current waveform lags behind voltage waveform because of the inductive component in load.

9. CONCLUSION

The paper presented a new topology in which the basic unit generated levels only in the positive half cycle. The H-bridge was added to the presented topology to generate all voltage levels (i.e. positive and negative) in the output voltage. Symmetrical values for the DC sources with unary sequence and one basic unit resulted in 5- levels output voltage. Asymmetrical DC sources with the binary algorithm was considered in selecting the DC sources. The single basic unit in the presented topology produced 7-level output voltage. It can be extended to 'N' number of levels by cascading the basic units. The proposed topology presented the best result compared with some selected topology in terms of switches versus levels, switches versus DC sources and cost function versus switches. The topology was validated using a prototype model with one basic unit, and the DC voltage source values were selected using binary algorithm to generate seven levels in the output voltage.

Table 3. Comparison of some existing MLIs

	Proposed topology	Cascaded H-bridge	[9]	[17]
N_{Levels}	$2^{(2n+1)}-1$ 'n' basic units number.	2^n-1 'n' basic units number	$10n+1$ 'n' basic units number	$2^{(n+3)}-5$ 'n' basic units number
$N_{Switches}$	$\frac{5}{2}\left(log_2^{\frac{N_{Level}+1}{2}}\right)-1$	$4log_2^{(N_{Level}+1)}$	$\frac{8}{10}(N_{Level}-1)$	$5\left(log_2^{N_{Level}+5}\right)-9$
$N_{Sources}$	$\left(log_2^{N_{Level}+1}\right)-1$	$\left(log_2^{N_{Level}+1}\right)$	$\frac{3}{10}log_2^{N_{Level}-1}$	$3\left(log_2^{N_{Level}+5}\right)-8$
V_{0max}	$\left(\frac{(N_{Level}-1)}{2}\right)V_{dc}$	$\left(\frac{(N_{Level}-1)}{2}\right)V_{dc}$	$\left(\frac{(N_{Level}-1)}{2}\right)V_{dc}$	$\left(\frac{(N_{Level}-1)}{2}\right)V_{dc}$
$DC_{Sources}$	Symmetrical (1:1) Asymmetrical (1:2)	Symmetrical (1:1) Asymmetrical (1:2)	Symmetrical (1:1) Asymmetrical (1:2)	Symmetrical (1:1) Asymmetrical (1:2)

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