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PV FED MODIFIED MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCH COUNT

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ABSTRACT

Inverter plays very important role in many areas of Renewable Sources of Energy (RSE). One of the major developments in using RSE is solar power. This article introduces the power converter topology and consists of a power interface and various levels of MIT (Multilevel Inverter Topology). A modified version of the Cascade H-Bridge Multilevel Inverter (CH-MLI) has been introduced to improve power quality, power loss and topology complexity and cost. The input voltage is set to the rated voltage by the power converter and transferred to the DC bus. The MIT converts the DC bus voltage to AC and is supplied to an AC load. For such inverters, the ideal number of levels and switching frequency are explored, and five-level architecture is chosen based on the trade-offs. To suppress harmonics, this inverter uses a level shifted in phase disposition pulse width modulation technique, which was chosen after extensive testing of other advanced disposition pulse width modulation techniques. To lower the harmonics even more, the use of filters was studied, and an LC filter has been used, which yielded satisfactory results. The entire system is simulated with MATLAB / SIMULINK. The proposed inverter is compared to CH-MLI in terms of DC sources, number of switches, diodes, driver circuit and dv/dt stress.

Keywords: *Multilevel Inverter Topology (MIT), Modulation Techniques, Duty Cycle, Total Harmonic Distortion(THD), Maximum Power Point Tracking (MPPT).*

1. INTRODUCTION

One of the eco- and environmental friendly technique of power-generation using RSE is solar photovoltaic system (PVS) of power-generation. In recent years, lot of changes, challenges, and developments have been taken in the area of PVS technology. When compared to the conventional method of thermal power-generation with coal, PVS technology is proven such that it is an affordable source of power[1] – [2]. The major requirements in the PVS are PV cells. Apart from PV cells the system may also consists of a DC-DC converter to get the rated DC voltage, an inverter which converters DC to AC, design of a filter if necessary and the generated AC power is to be interfaced to a grid [3]. Generated power which is interfacing to grid should be free from harmonics. A major challenge that is the selection of inverter which has to produce a harmonic free AC power-generation. A two-level inverter is the basic inverter having many disadvantages such as, they introduce lot of harmonics in the voltage and current, selection of input voltage is double than that of the output voltage, higher switching losses and frequency. A two-level inverter can be preferred for low power applications [4].

To reduce the disadvantages of a two level inverter, several MITs are introduced. MITs are best suitable for high & medium power industrial applications [4] – [5]. The conventional MITs are [6], Diode clamping (DCM), Flying Capacitor (FLC) & Cascaded H-B (CHB-MLI) [7] – [9].

MITs consists of power semiconductor devices (PSDs) are of controlled devices, need to drive the gates. These PSDs can be controlled by using different modulation techniques depending upon the type of MIT chosen [10]. To drive the gates various modulation techniques applied for MITs are multicarrier pulse width modulation(PWM),

selective harmonic elimination, space vector PWM etc. [11] – [13].

Multicarrier PWM is simple with reduced control circuit complexity, level-shifted & phase-shifted multicarrier PWM can be applied [14]. Further different techniques to selection of carrier are phase - disposition (PD), phase – opposition - disposition (POD), alternate – phase – opposition - disposition (APOD) and phase-shifted carrier [15] – [18]. After implementing MIT with a proper modulation, still there exists lower order harmonics at the output of the inverter which are the result of high-switching frequency [19]. Thus a filter is required to further reduce the harmonics. A filter is designed such that it should have a low cut-off frequency & high attenuation at high switching frequency.

This study built on previous research by determining the optimal number of levels (using a 6-switch 5-level reduced switch topology), evaluating several PWM switching techniques and selecting the best one, and then evaluating different filters to use in the resulting system to further reduce output THD.

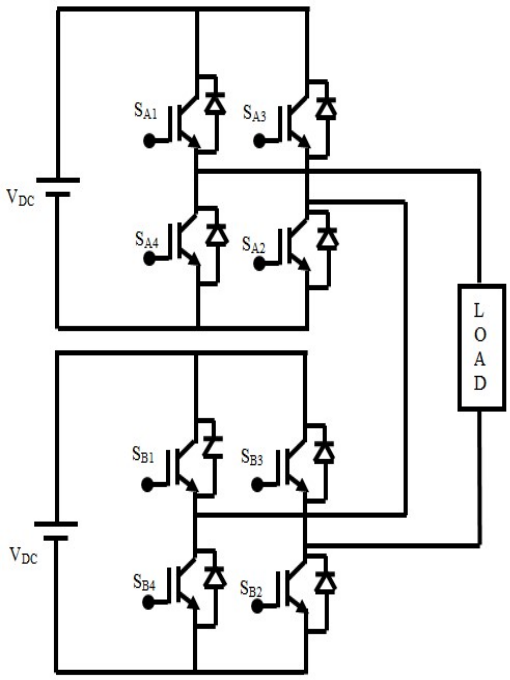
In this work a new topology of MIT is introduced with reduced number of PSDs and is fed from a PVS. An advanced phased array pulse width modulation technology is used to drive MIT. A proper LC filter with high attenuation and low cut-off frequency is designed to further reduce the harmonics at the output AC terminal of inverter. To track the maximum power of PVS incremental conductance algorithm is implemented. The entire system is implemented in MATLAB/SIMULINK and the results obtained with the proposed system are compared with the conventional MIT fed from PVS. Simulation results of the proposed MIT fed PVS provides the best results compared to the conventional MIT fed PVS in terms of reduced number of PSDs, harmonics and switching losses.

The rest of this paper is structured out as follows: The theoretical foundation of multilevel inverters, the PWM switching mechanism employed, and the reasons for adopting PWM instead of conventional switching sequences and filters are presented in Section II. In section III, the suggested MIT with integrated PVS is given. The simulation investigations on the proposed MIT using various switching techniques are presented in Section IV. Finally, in section V, the conclusions are drawn.

2. STRUCTURE AND OPERATING MODES OF PROPOSED MULTILEVEL INVERTR TOPOLOGY

Basic 5-level CHB-MLI is shown in Figure 1(a) whereas modified structure proposed in this paper is in Figure 1(b). To produce five voltage levels at the AC terminal of CHB-MLI, it require eight number of PSDs, whereas modified MIT requires six number of PSDs. Different modes of operation of modified MIT is shown in Figure 2. Five-levels of AC terminal voltage that is given by CHB-MLI is $+V_{DC}$, $-V_{DC}$, $+2V_{DC}$, $-2V_{DC}$ and 0V. $+V_{DC}$ and $-V_{DC}$ are obtained by turning on two main PSDs and one body diode. Similarly to obtain $+2V_{DC}$ and $-2V_{DC}$ three PSDs will turn on.

When compared to CHB-MLI, in the modified MIT only three PSDs turns, so that using this topology conduction and switching losses can be reduced. To get $+V_{DC}$ and $-V_{DC}$ one body diode conducts, which results in reduction of efficiency & quality of the signal.



(a)

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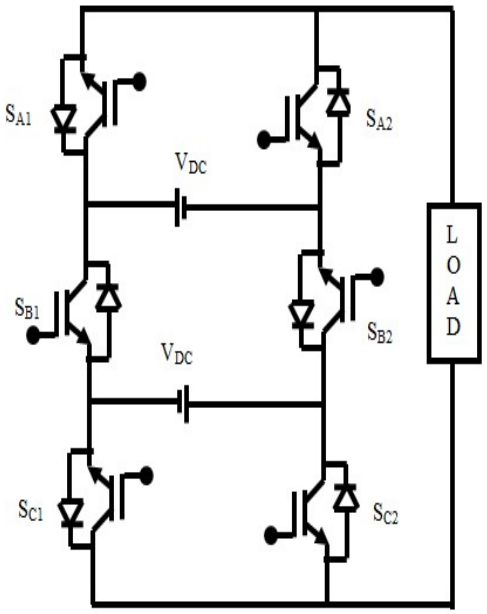


(b)

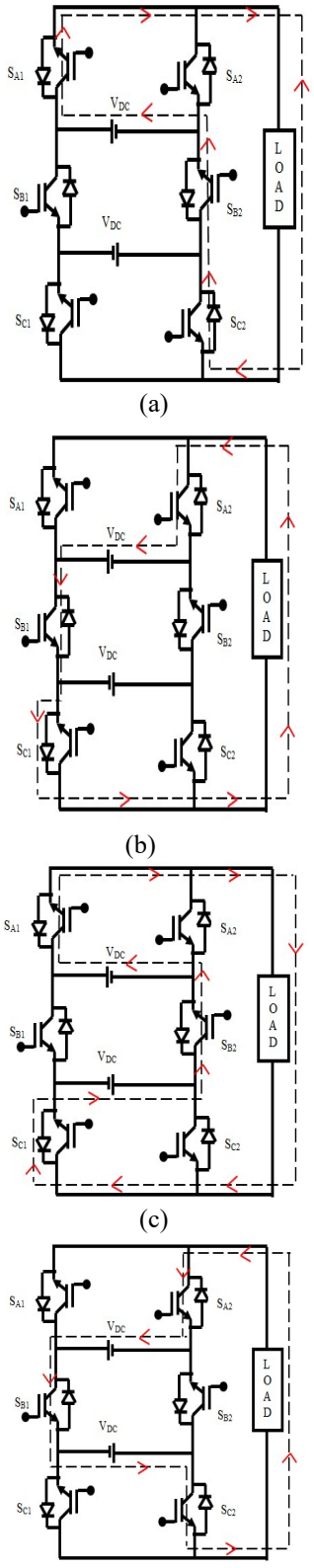
Figure 1: (a) 5-level CHB-MLI (b) Modified MIT

The switching sequence of modifies MIT is represented in Table 1 and operating modes are shown in figure 2.

Table 1: Switching Sequence

S_{A1}	S_{A2}	S_{B1}	S_{B2}	S_{C1}	S_{C2}	V_0
0	0	0	0	0	0	0
1	0	0	1	0	0	$+V_{DC}$
1	0	0	1	1	0	$+2V_{DC}$
0	1	1	0	0	0	$-V_{DC}$
0	1	1	0	0	1	$-2V_{DC}$

AC terminal voltage can be obtained by switching sequence, with witching frequency of 50 Hz. However this method of triggering the PSDs will introduce lot of harmonics. Instead of using this method of triggering, PWM techniques are preferable to a better sine wave. One of the best PWM technique that can be applied to CHB type MLIs is multicarrier PWM. In multicarrier PWM a sinusoidal reference wave is compared with a high-frequency triangular carrier and pulses are generated accordingly. This technique can be applied in two different ways: level shifted PWM (LSPWM), phase shifted PWM (PSPWM).



(a) (b) (c) (d)

Figure 2: Modes of operation of modified MIT

(a) $+V_{DC}$ (b) $-V_{DC}$ (c) $+2V_{DC}$ (d) $-2V_{DC}$

Carriers are implemented in LSPWM in different ways as PD, POD and APOD. In PSPWM technique number of carriers are selected with phase shift between the carriers and phase shift is calculated as

$$\theta = \frac{180^0}{m} \quad (1)$$

Where m: number of H-Bridges.

Figure 3 shows the modulation scheme for 5-level inverter. Here two carriers are required with high-frequency and is compared to sinusoidal reference, to generate pulses shown in Figure 4.

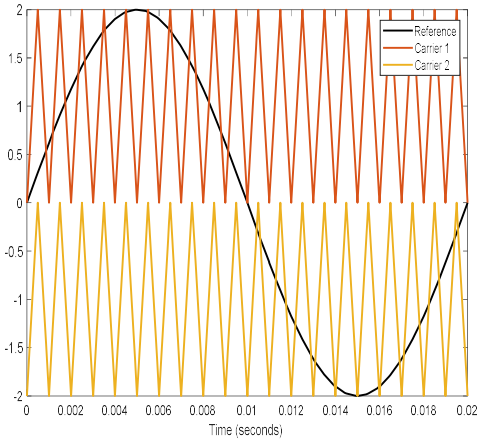
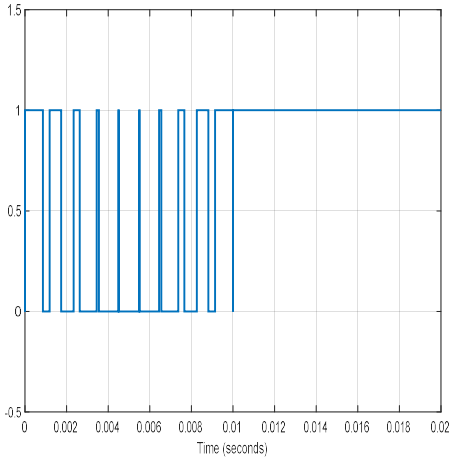
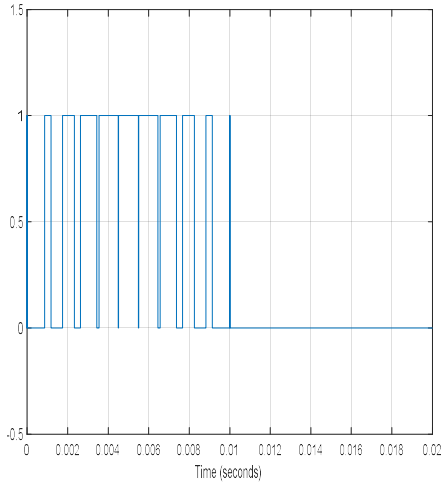
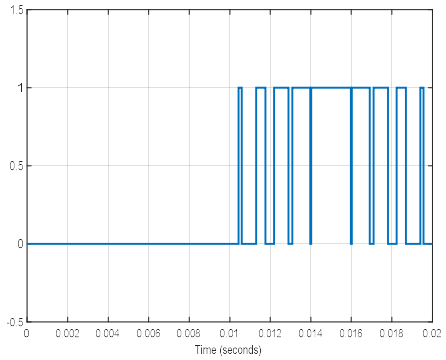


Figure 3: PDPWM technique







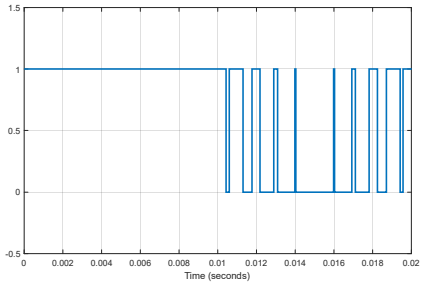


Figure 4: Pulse generation using PDPWM

3. PV FED MODIFIED MULTILEVEL INVERTER TOPOLOGY

The proposed PVS fed MIT through battery for one module is shown in figure 5, and battery is charged from PV cell through Boost converter. To track the maximum power from PV, Maximum Power Point Tracking technique is implemented. Many algorithms are available in the literature, each and every algorithm has its own merits and demerits. In this work, MPPT algorithm used is incremental conductance.

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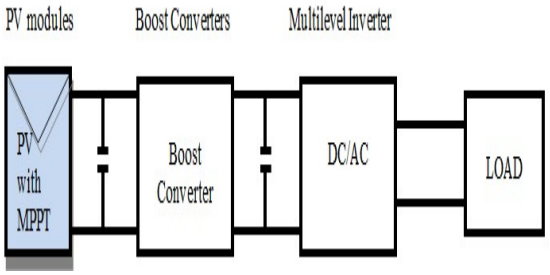

Figure 5: PV fed Multilevel Inverter for one module

3.1 Electrical Model of PV

Figure 6 shows the equivalent electrical circuit of ideal PV cell in single diode model. The equivalent circuit consists of anti-parallel diode with current source and series, parallel resistance. The basic current response of ideal PV is given by

$$I = I(p) - I_D$$

$$I_D = I(p)\left[e^{\left(\frac{qv}{akT}\right)} - 1\right]$$

Where
I(p) – Saturation current
a – Quality factor of the diode
q – Charge of an electron
k – Boltzmann's constant
T – Junction Temperature
kT/q – Thermal voltage

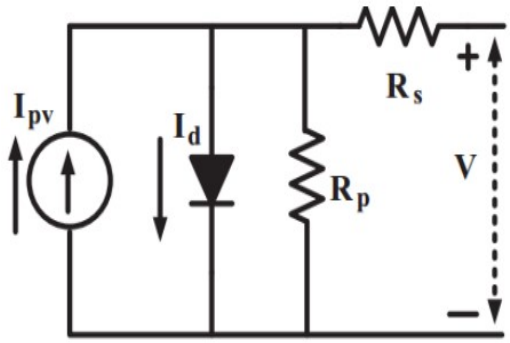

Figure 6: PV Single diode model

Response of single diode model of PV is not sufficient to generate I – V characteristics of PV array. PV array is formed by grouping of PV cells in series or parallel manner. The cells of solar connected in series provide higher output voltage whereas in parallel connection provides higher current. I-V characteristic depends on series resistance, parallel resistance, temperature and irradiation. Figure 7 show I-V and P-V curves of 213.15 W photovoltaic panels respectively. Table 2 presents the different parameter values of 213.15 W PV panel.

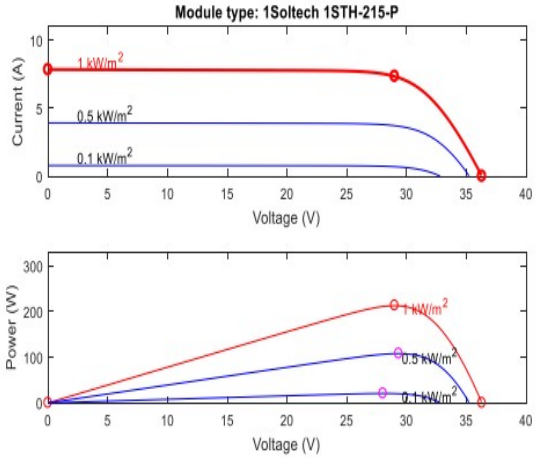

Figure 7 : I-V curve and P-V curve of 213.15 W photovoltaic panels

Table 2 : PV Parameters

Parameters	Values
Short circuit current (Isc)	7.84A
Open circuit voltage (Voc)	36.3V
Maximum power point voltage (Vmp)	29V
Maximum power point current (Imp)	7.35A
Maximum power (Pmp)	213.15W

3.2 Boost Converter

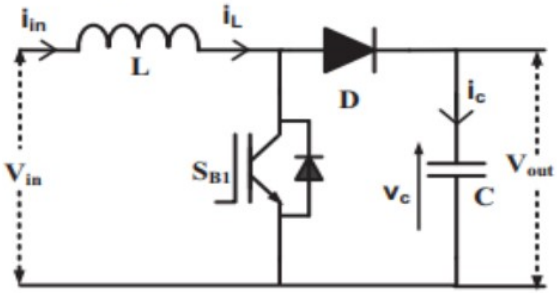

Figure 8 : Boost Converter

A boost converter is used to boost-up the DC voltage provided by PV cell and its operation is controlled by MPPT. Figure 8 shows the circuit diagram of boost converter. When the switch S_{B1} is closed for time duration t_1, the inductor current rises and the energy is stored in the inductor. If the switch S_{B1} is opened for time duration t_2, the energy stored in the inductor is transferred to the load via the diode D_1 and the inductor current falls. The waveform of the inductor current is shown in Figure 9.

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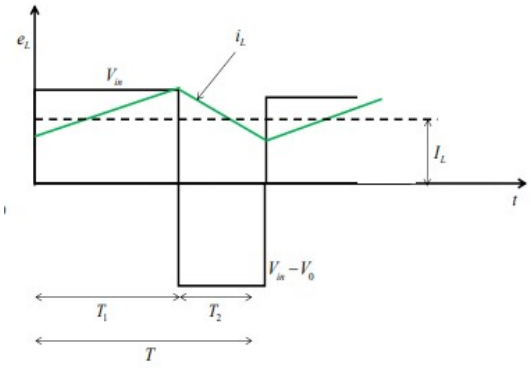

Figure 9 : Inductor current

The switch used in the Boost Converter operates at very high switching frequency to generate maximum power and the duty cycle for the switch is generated from MPPT algorithm. The values of Inductor (L) and Capacitor (C) to be chosen such that

$$L = \frac{V_{in}\delta}{f\Delta i_L} \text{ and } C = \frac{V_o\delta}{R\Delta V_c f}$$ where Δi_L is the peak-peak ripple current, ΔV_c is the peak-peak ripple voltage of the capacitor and δ is the duty cycle.

3.3 Incremental Conductance Algorithm

The advantages of incremental conductance algorithm is: it has higher-accuracy and its flow diagram is given in Figure 10.

The duty cycle of the converter is tuned automatically. The output voltage and current of the PV at time p are V(p) and I(p), respectively. ΔV and ΔI are the difference in voltage and current for time p-1 and p. ΔV and ΔI decides the duty cycle. The step size or duty cycle is unchanged if $\frac{\Delta I}{\Delta V} = -\frac{I}{V}$ or ΔI = 0, else it may increase or decrease depending on the ratio between ΔI and ΔV.

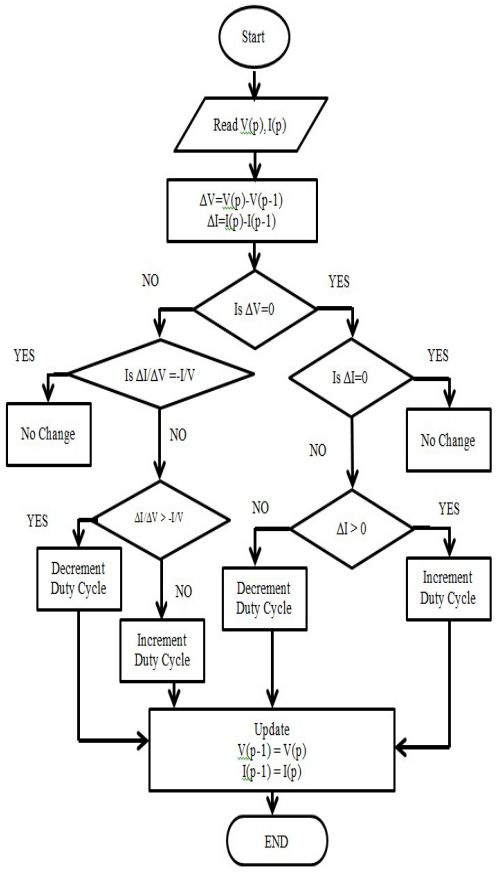

Figure 10: Flow diagram of MPPT algorithm

4. SIMULATION RESULTS

Simulink model of PV fed boost converter is shown in Figure 11. PV module considered in MATLAB is 1 Soltech 1STH-215-P, the maximum open circuit voltage is 36.3V and short-circuit current is 7.84A for one module of PV. Here two number of series-connected modules per string and one parallel string is selected, so the maximum open circuit voltage of PV is 72.6V. Each module of PV is exposed to 25^0C and specified irradiances are [1000 500 100]. The PVS is tuned using incremental and Conductance algorithm, which controls the operation of boost converter to step-up the output of PV. Here the maximum output of PV obtained is 72.57V and the output of boost convert is 104.6V are shown in Figures 12 and 13 respectively.

Input DC of MIT is connected from the output of boost converter is Shown in Figure 14. MIT is operated at different switching frequencies with and without using filter circuit. To control the output of MIT PD-LSPWM is chosen.

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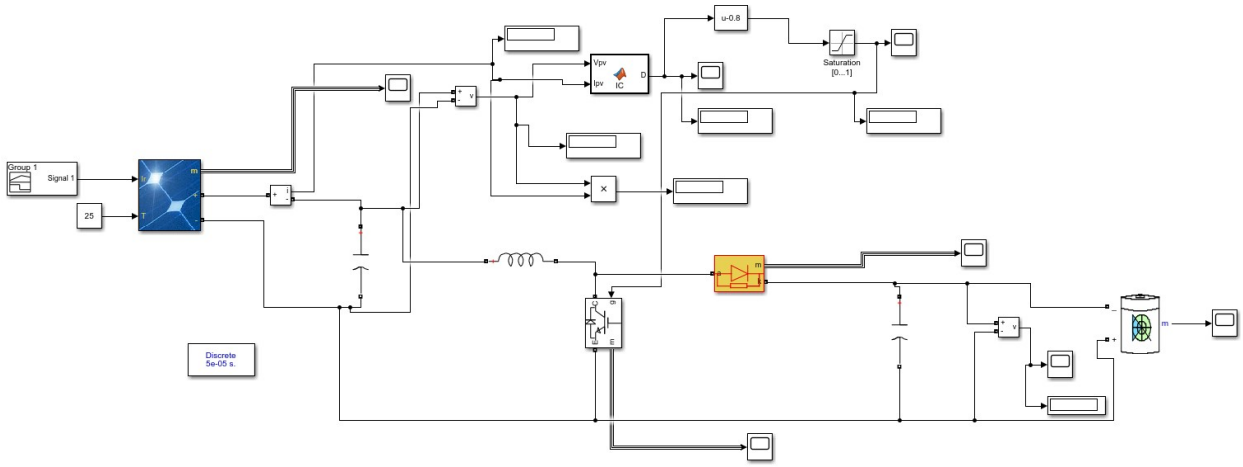

Figure 11: Simulink model of PV fed boost-converter

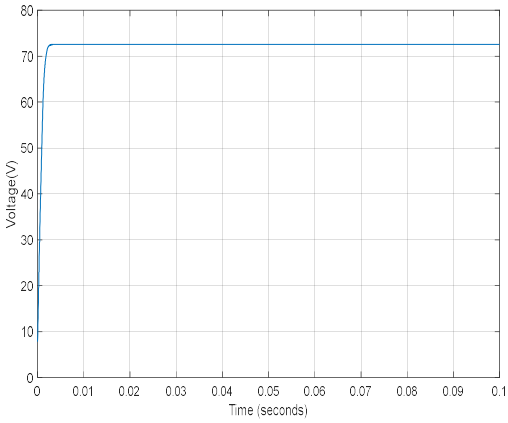

Figure 12 : PV terminal Voltage

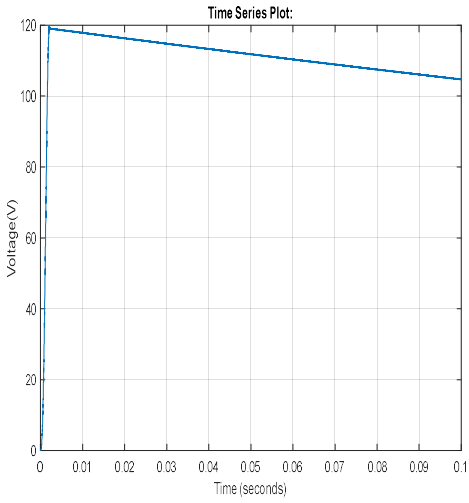

Figure 13 : DC voltage of Boost converter

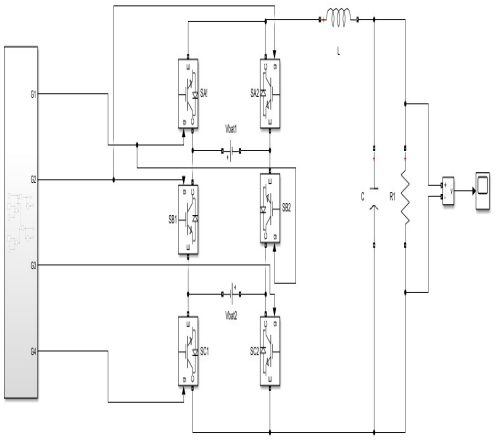

Figure 14 : Simulink Model of Modified MIT

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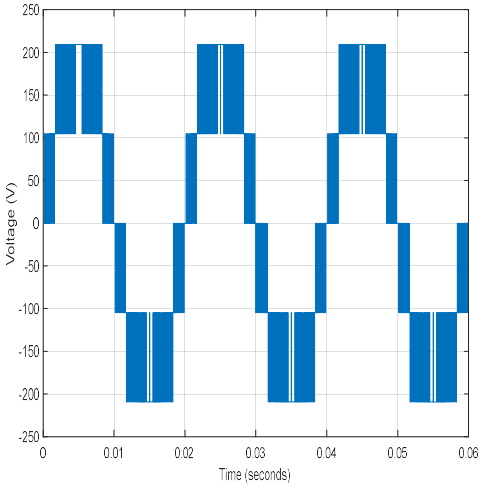

Figure 15(a): Proposed MIT 5-level voltage without filter

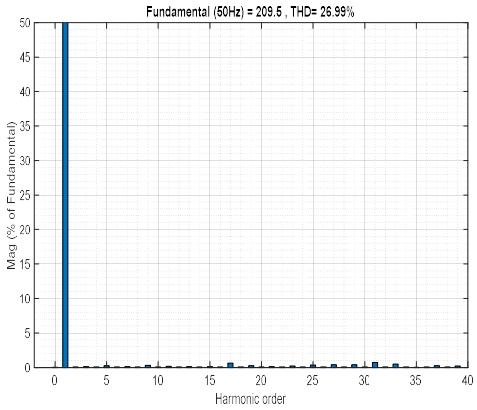

Figure 15 (b) : THD of proposed MIT without filter

The inverter output voltage and THD with and without filter is shown in Figure 14 and 15 respectively.

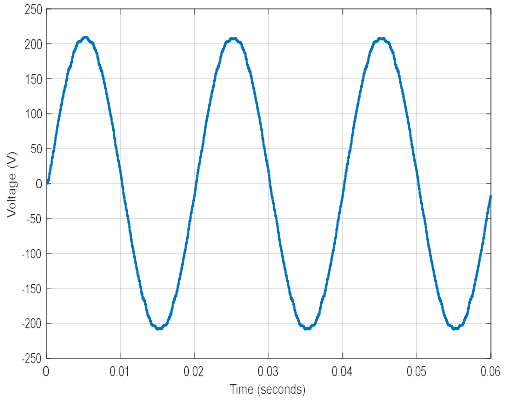

Figure 16 (a): Proposed MIT 5-level voltage with filter

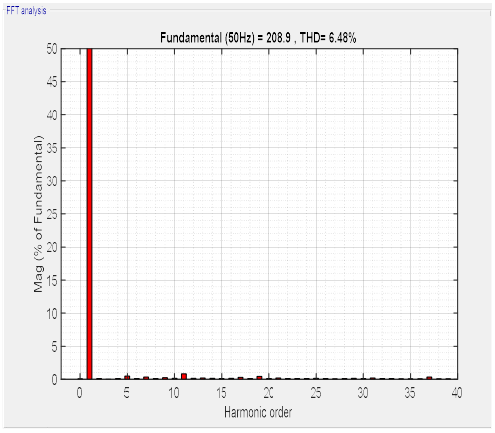

Figure 16 (b) THD of proposed MIT with filter

Similarly PVS based CHB-MLI is simulated, the output voltage and THD with and without filter is shown in Figure 17 & 18. From this it is observed that the MIT gives less THD than CHB-MLI. The comparison of two converters for five level inverter is shown in Table 3. By observing the comparison between two converters proposed MIT uses less number of switching devices with reduced THD.

Combining all of the THD values acquired from the simulations and comparing them for two cases: PWM unfiltered and PWM filtered for inverters. Because high-level inverters increase circuit complexity and cost, level seven is the recommended cutoff for multilevel inverter application.

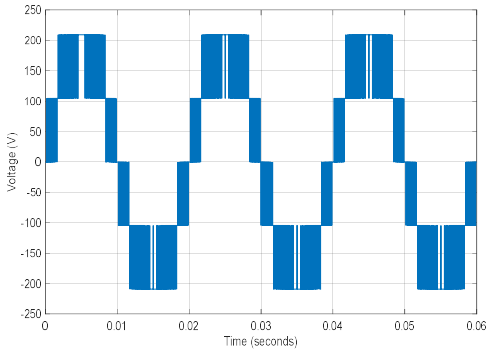

Figure 17(a): PVS based CHB-MLI 5-level voltage without filter

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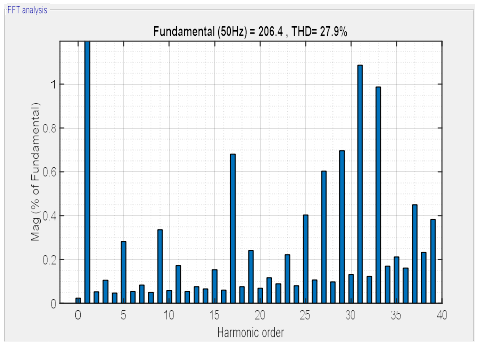

Figure 17(b): THD of PVS based CHB-MLI without filter

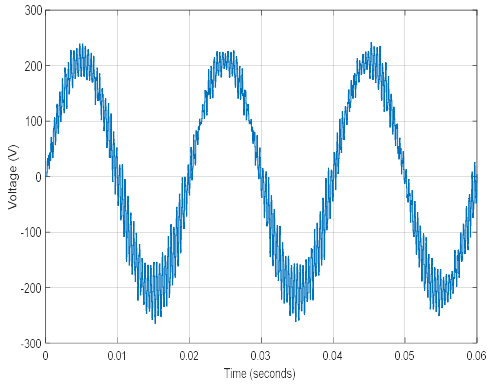

Figure 18(a): PVS based CHB-MLI 5-level voltage with filter

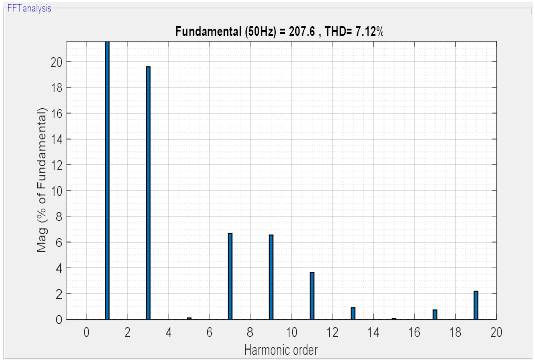

Figure 18(b): THD of PVS based CHB-MLI without filter

Table 3 : Comparison of CHB-MLI and proposed MIT

PARAMETERS	CHB-MLI	MIT
No. of DC sources	2	2
No. of PSDs	8	6
No. of body diodes	8	6
Gate drivers	8	6
Inverter output voltage with filter	207.6	208.9
THD without filer	27.9%	26.99%
THD with filter	7.12%	6.48%

An LC filter is designed such that, by choosing proper selection of resonant frequency based on switching frequency.

Filter resonance frequency is calculated using eq (2) and (3)

$$f_{res} = \frac{f_{res}(\min) + f_{res}(\max)}{2} \quad (2)$$

$$10 f_m \le f_{res} \le \frac{f_{switch}}{2} \quad (3)$$

f_{res} : resonance frequency

f_m : fundamental frequency

f_{switch} :switching frequency

L and C values can be calculated using eq (4)

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (4)$$

The value of C is chosen as 4µF, so that L value can be determined for resonance frequency. Table 4 provides the filter values for different switching frequencies.

Table 4 : Filter values for different switching frequencies

S. No.	f_{switch}	f_{res} (min)	f_{res} (max)	F_{res}	C – filter	L – filter
1	1000	500	500	500	4µF	2.53mH
2	1500	500	750	625	4µF	1.62mH
3	2000	500	1000	750	4µF	1.125mH
4	2500	500	1250	875	4µF	0.827mH
5	3000	500	1500	1000	4µF	0.633mH
6	3500	500	1750	1125	4µF	0.5mH
7	4000	500	2000	1250	4µF	0.405mH
8	4500	500	2250	1375	4µF	0.335mH
9	5000	500	2500	1500	4µF	0.28mH
10	5500	500	2750	1625	4µF	0.24mH
11	6000	500	3000	1750	4µF	0.206mH
12	6500	500	3250	1875	4µF	0.18mH

5. CONCLUSION

A 1-φ modified 5-level MIT with six switches is presented in this paper. The cost, complexity, area need, and losses have all reduced as a result of the switch reduction, while efficiency has enhanced. The MIT has been chosen over other designs because of

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its unique benefits. The advantages of MIT have been explored, including the optimal number of levels in the MIT and the optimal switching frequency. In this investigation, the best performing system was a 5-level MIT with a switching frequency of 3kHz. This performance, however, was achieved using unfiltered outputs. An LC filter was employed in this work to drastically minimize THD in the output. Proposed MIT is controlled using PD-LSPWM which is used for CHB-MLI also. Simulated results prove that for the same PWM technique. Proposed MIT gives best results as compared to CHB-MLI. Further this work can be carried out for higher levels and validate the simulated results with experimental setup.

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