ISSN: 1992-8645

www.jatit.org



POLAR CODE PERFORMANCE ANALYSIS FOR HIGH-SPEED WIRELESS DATA COMMUNICATION SYSTEM

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ABSTRACT

Polar code is the first channel code proven to reach Shannon capacity and is proposed for use in high-speed data communication system. However, the use of independent Polar code with a finite number of bits shows poor performance compared to earlier codes, namely Turbo and Tail-biting Convolutional codes. In this study, the Polar code is equipped with the Cyclic Redundancy Check (CRC-11) code and the Succesive Cancellation List (SCL) decoder according to the recommendations in the 5G System Specifications. The code performance is analyzed for a limited number of bits, using BLER and E_s/N_0 as performance parameters. The number of bits of information encoded in this study were 32 and 64 bits, while the number of bits in the codeword were 432, 864, and 1728 bits, so that the code performance for short blocks of information and codewords can be observed. The list sizes on the decoder are 1, 2, and 4. The simulation results show that the simulated code allows communication to take place with the value of Es / N0 in the range -11.5 dB to -1.8 dB to achieve Block Error Rate (BLER) 10⁻². This shows that a Polar code equipped with a CRC code and an SCL decoder has a good performance for a limited number of bits.

Keywords: 5G, CRC, SCL decoder, Polar Code

1. INTRODUCTION

The demand for reliable and high-speed wireless communication device interconnection has prompted the development of high-speed wireless data communication systems, the most prominent of which is the 5th generation wireless communication system or better known as the 5G communication system. The 5G communication system has the potential to realize data transmission speeds of up to 20 Gbps for downlink and 10 Gbps for uplink. A special feature of the 5G communication system that differs from its predecessors is the new channel coding pair for the data channel and the control channel [1]. In the data channel, the Linear Density Parity Check (LDPC) code is used which replaces the Turbo code in the 4G communication system. In the control channel, Polar code is used which replaces the Tail Biting Convolutional Code (TBCC) which was previously used in 4G communication systems [2]. Polar code is the first channel code that is proven to be able to achieve Shannon capacity for discrete binary input channels with a simple decoder [3], [4]. However, when used independently, Polar code with a finite number of bits shows poor performance compared to its predecessor codes [5]. Therefore, additional code is required to be used in conjunction with the Successive Cancellation (SC) decoder to improve its performance [6], [7], [8], [9]. A type of SC decoder that is commonly used is Successive Cancellation List (SCL), where the decoder yields a list of possible codewords as an output [10], [11], [12], [13]. An additional code commonly used with SCL decoders for Polar codes is the Cyclic Redundancy Check (CRC) code [9].

Research [14] has discussed about combining CRC with Polar code, with the focus of research on designing Polar coding with CRC code interleaved into it. The study did not specifically address the performance of Polar codes for a finite number of bits. Research [15] analyzed the best CRC codes to use with Polar codes. The code performance measure used is the minimum distance, and the consideration of the number of bits is not included in the discussion in this study.

Journal of Theoretical and Applied Information Technology

 $\frac{15^{\text{th}} \text{ April 2022. Vol.100. No 7}}{@ 2022 \text{ Little Lion Scientific}}$

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ISSN: 1992-8645
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The performance of Polar Codes when applied to infinite numbers of information bits are wellknown, however its performance for a finite number of information bits have not been particularly studied in recent researches. Therefore in this paper we propose the analysis of Polar code performance for the Physical Uplink Control Channel (PUCCH) on a 5G system with a limited number of bits. The number of bits of information A used is limited to 32 bits and 64 bits, and the number of bits in the encoding codeword is limited to 432, 864, and 1728 bits. The number of bits of information A in the selected uplink channel refers to the limit of 12 bits to 1706 bits, while the number of bits in the codeword E refers to the limit of 8192 bits [16]. The SCL used has a L list size of 1, 2 and 4 while the CRC used is CRC-11.

This paper is structured as follows. The second part of the paper will discuss channel polarization as the basis of Polar coding, as well as the structure of Polar coding. The CRC code will be revisited in the third section. The system model is given in the fourth section. The fourth section discusses the simulation results and conclusions are given in the last section.

2. CHANNEL POLARIZATION AND POLAR CODE STRUCTURE

A number of N independent communication channels can be combined with the channel polarization method, and then separated again in the decoding process. Channels that are processed in this way will experience separation, where some channels will have a capacity close to 1, while some other channels will have a capacity close to 0 [17]. Channels with a capacity close to 1 will be used for data transmission, while a channel with a capacity close to 0 will not be used because it is a pure noise channel. This polarized channel condition is the basis of coding using Polar Code [17].

Polar code is a linear block code with length $N = 2^n$ which is formed with a generator matrix with the following basic form [18]:

$$F = \begin{bmatrix} 1 & 0\\ 1 & 1 \end{bmatrix} \tag{1}$$

For example, for n = 3, then $N = 2^3$ and can be formed by multiplying the Kronecker product of the generator matrix in Eq. (1), in the following manner:

$$\mathbf{F}^{\otimes_{3}} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \otimes \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \otimes \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \otimes \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

$$(2)$$

Polar encoding is done by multiplying the input bits by the generator matrix. For example, when a generator matrix is used as in Equation (2), or it can be expressed as:

$$\mathbf{c} = \mathbf{G} \cdot \mathbf{u} = \left(\mathbf{F}^{\otimes n}\right) \cdot \mathbf{u} \tag{3}$$

where c is the codeword or result of encoding, u is the input bit matrix and $G = F^{\otimes n}$ is the generator matrix [19]. The resulting Polar codeword can be expressed by (N, K, F) where N is the length of the codeword in bits, K is the number of bits of information encoded per codeword, and F is a set of N-K integers called frozen bits and has a value of 0 [19]. The Polar code on the uplink channel of the 5G system is used to encode the Uplink Control Information (UCI) on the Physical Uplink Control Channel (PUCCH) and the Physical Uplink Shared Channel (PUSCH)[20].

Polar code decoding is done using Successive Cancellation (SC), where every bit that arrives at the receiver will be decoded sequentially using the information obtained from the channel as well as the hard decision of the previously received code [20]. SC has poor performance for short code, so it is less applicable to real applications. The development of SC is the Successive Cancellation List (SCL) where a set of SC decoders work in parallel to manage several candidate codewords that arrive at the receiver simultaneously [21]. The number of candidate codewords managed by the decoder at the same time is expressed as a list size or L. SCL improves decoding performance for codes of practical length, especially when combined with other channel encodings such as Cyclic Redundancy Check (CRC).

The decoder in SCL decodes the bits sequentially, one bit by one bit. In spite of this, L decoding paths are considered simultaneously at each decoding stage. The SCL decoder uses two decoding paths for each information bit u_i , considering both $u_i = 0$ and $u_i = 1$ options. From all the possible paths calculated, all but L most likely paths will be removed from consideration. Once the decoding process is done, the most likely among the

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E-ISSN: 1817-3195

L decoding path is selected as the decoder output [12].

3. CRC CODE

CRC code is a family of linear codes, which has a parameter of k bits to be encoded, n encoding bits, and (n-k) parity bits [9], [14]. Additionally, there is also a parameter P, which is a predetermined divisor, which can completely divide the resulting CRC codeword. If the information to be encoded is D, the CRC codeword can be expressed as:

$$T = 2^{n-k}D + (n-k) \tag{4}$$

CRC code can be expressed in polynomial form. If the information to be encoded in polynomial form is D(x) and the predetermined divisor is P(x), then

$$\frac{x^{n-k}D(x)}{P(x)} = Q(x) + \frac{R(x)}{P(x)}$$
(5)

where Q(x) is the result of the division and R(x)/P(x) is the remainder of the division. Thus the codeword in polynomial form is

$$T(x) = x^{n-k} D(x) + R(x)$$
 (6)

From Eq. (4), it is apparent that the information symbols form a part of the codeword, therefore the CRC codewords are systematic. The CRC decoder will check for errors by calculating whether or not the received codewords are divisible a generator polynomial g(x), which has the following form:

$$g(x) = g_i x^{n-k} + g_{i-1} x^{n-k-1} + \ldots + g_1 x + g_0$$
(7)

There are several types of CRC codes that have become international standards, including CRC-12 and CRC-16. The CRC-12 code has P(x) with the highest power of 12, and CRC-16 has P(x) with the highest power of 16. The CRC code used in this study is CRC-11, which generator is given by

$$g(x) = x^{11} + x^{10} + x^9 + x^5 + x^1 \tag{8}$$

The total number of bits after adding the CRC code and Polar code to the information bits was varied as many as 432, 864, and 1728 bits.

4. METHODS

The research was carried out by making simulations based on the system model given in Figure 1, and referring to [16]. A sequence of A bits of information will be formed into a polar codeword of T bits. The results of the coding will be reencoded using Polar code so as to form a new codeword with a length of N bits. Given that N must be 2n while the number of bits T does not need to meet 2n as long as T < N, then a rate matching process is needed, where the number of bits from the Polar encoding is adjusted to the required code rate. The minimum code rate for 5G communication is 1/8[20]. In this study, the A/E rate as given in Table 1. The data is transmitted by OPSK modulation on the AWGN channel. On the receiving side, demodulation, rate recovery, and decoding processes are carried out for Polar code and CRC code, respectively.

The performance analysis is based on E_s/N_0 (dB) versus the Block Error Rate (BLER) that is obtained for a particular E_s/N_0 level. Commonly, the addition of bits meant to give the information bits better protection against error, will cause the decrease of E_s/N_0 needed to reach a certain BLER.

The parameters used in the simulation are given in Table 1.

| Table 1. Simulation Farameters | |
|--------------------------------|---------------------------------------|
| Numbers of information | 32, 64 |
| bits, A | |
| Numbers of bits in the | 432, 864, 1728 |
| codeword, E | |
| A/E rate | 32/432; 32/864; 32/1728 |
| | 64/432; 64/864; 64/1728 |
| | |
| CRC-11 code generator | $x^{11} + x^{10} + x^{9} + x^5 + x^1$ |
| I :-+ -: I | 1.2.4 |
| List size, L | 1, 2, 4 |
| | |

Table 1. Simulation Parameters

The number of bits of information A selected corresponds to the available options for the 5G parameter, namely 12 bits A 1706 bits. The 5G specification states that there are three options for CRC codes that can be used on 5G systems, namely CRC-6, CRC-11, and CRC-24. The CRC-11 code was chosen in this study because it is recommended for use in PUCCH with A > 20 bits.



Figure 1. System model

5. RESULTS AND DISCUSSION

The simulation results for the number of data A= 32 bits and the number of bits after encoding E =432 bits are given in Fig. 2. Simulations are carried out for list sizes L = 1, 2, and 4. From the simulation results, it can be seen that the best performance will be obtained when L = 4 is used, where $BLER = 10^{-2}$ can be achieved with E_s/N_0 less than -5 dB. A smaller list size will have an impact on the larger $E_{\rm s}/N_0$ values needed to achieve a certain BLER performance. The larger the size of the list used, the more codewords the decoder considers, so the more likely it is that the decoder picks the right codeword and does not contain errors. At L = 4 there are 4 possible codewords considered by the decoder. The four possibilities will first be checked using a CRC decoder. Codewords that are successfully decoded

with the CRC decoder will be selected for further processing with the Polar decoder. If L = 1, the decoder only considers one possible codeword in the receiver. If the codeword contains errors, the decoding process is not successful. This causes the BLER performance for L = 1 to be worse than when L = 2 and L = 4.

Fig. 3 shows the simulation results when A = 32and E = 864 bits. The system performance when E= 864 bits will be better than when E = 432. In this simulation, the BLER = 10^{-2} is reached at E_s/N_0 less than -8 dB, smaller than what is needed to achieve the same BLER when E is 432 bits. The lower E_s/N_0 required to reach the BLER = 10^{-2} benchmark indicates that the number of errors is getting smaller as more protection bits are used when E = 864 bits.



Figure 2. Simulation Result For A = 32 bits and E = 432 bits



Figure 3. Simulation Results For A = 32 bits, and E = 864 bits

Fig. 4 shows the simulation results when E = 1728 bits is used. It is apparent that the system performance for both L = 1, 2 and 4 will be better than when E = 864 bits are used, which is indicated by the smaller E_s/N_0 values needed to reach the BLER = 10^{-2} benchmark. When L = 1, to reach BLER = 10^{-2} , the E_s/N_0 required approaches -10.1 dB, as opposed to -11.1 dB and -11.8 dB required when L = 2 and 4, consecutively. For all L values used in the simulation, the E_s/N_0 required to reach BLER = 10^{-2} are less than that needed when E = 864 bits (Fig. 3). This is because the use of more protective bits (i.e., E = 1728 bits instead of 864 bits) will improve the system performance.

The simulation results for A = 64 bits, with list size L = 1, 2, 4 and the number of bits after encoding E = 432, 864 and 1728 respectively are given in Figures 5, 6 and 7. In Fig. 5, simulation shows that for A = 32, the use of list size L = 1 will necessitates E_s/N_0 value of -1.875 dB to reach BLER = 10^{-2} . When L = 2, the E_s/N_0 required is -2.625 dB, and when L = 4, the E_s/N_0 needed is -3.25 dB.

Fig. 6 shows that when A= 64, for L = 1, the E_s/N_0 value of -4.875 dB to reach BLER = 10^{-2} . When L = 2, the E_s/N_0 required is -6 dB, and when L = 4, the E_s/N_0 needed is -6.49 dB.

In Fig. 7, it is shown that for L = 1, the E_s/N_0 value of around -8 dB to reach BLER = 10^{-2} . When L = 2, the E_s/N_0 required is -9.2 dB, and when L = 4, the E_s/N_0 needed is -9.7 dB.

Consistently, the simulation results when A = 64bit indicates that the performance is better with the higher the value of L and the number of bits after encoding E.

It is worth noting that when compared to the use of data bits A = 32 bits, the simulation results for A = 64 bits will show poorer performance. For example, with A = 64 bits and E = 432 bits shown in Figure 5, E_s/N_0 is required in the range of -3.25 dB to -1.875 dB to achieve BLER 10⁻². To achieve the same BLER of 10^{-2} , if A = 32 bits and E = 432 bits, the range of E_s/N_0 required is -5.4 dB to -4.1 dB. This is also seen in Fig. 6, where the E_s/N_0 level required is in the range of -5.1 dB to -4.9 dB to achieve BLER = 10^{-2} when A = 64 bits and E = 864bits. The same BLER can be achieved at E_s/N_0 range of -8.5 dB to -7.3 dB when A = 32 bits and E = 864bits. Fig.7 shows that to achieve $BLER = 10^{-2}$ when A = 64 bits and E = 1728 bits, the E_s/N_0 needed is in the range of -9.7 dB to -8 dB, which is larger than E_s/N_0 required when A = 32 bits and E = 1728 bits. The decrease in code performance when the A value increases, as indicated by the increase in E_s/N_0 required to reach a certain BLER, is caused by a tradeoff between E_s/N_0 and the A/E code rate. The smaller the A/E ratio, the smaller the E_s/N_0 required to reach a certain BLER.

The simulation results show that to achieve BLER 10⁻², the E_s/N_0 required for both A = 32 bits and 64 bits, for all simulated L values, always has a negative value or the signal power is below the noise power. This shows that the Polar code equipped with the CRC code and Polar decoder has a very good BLER performance that allows communication to occur even though the noise power exceeds the signal power.

ISSN: 1992-8645

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Figure 4. Simulation Result For A = 32 bits, and E = 1728 bits

 E_s/N_0 [dB]



Figure 5. Simulation Result For A = 64 bits, and E = 432 bits



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Fig. 6. Simulation Result For A = 64 bits, dan E = 864 bits



Figure 7. Simulation Result For A = 64 bits, dan E = 1728 bits

<u>15th April 2022. Vol.100. No 7</u> © 2022 Little Lion Scientific

ISSN: 1992-8645

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6. CONCLUSION

This study discusses the analysis of Polar code performance for a limited number of bits of information and codewords. The Polar code is equipped with a CRC code and an SCL decoder, where the CRC code used is CRC-11 and the SCL decoder has a list size of L = 1, 2, and 4. The code performance is analyzed using simulation, which generates 32- and 64-bit random binary information, and the number of bits in the codeword is 432, 864 and 1728 bits. The simulated BLER value of 10⁻² can be achieved with E_s/N_0 which is negative, which indicates that the Polar code with CRC code and SCL decoder allows communication even though the noise power exceeds the signal power. Simulations show that the system performance will improve when the list size L is increased, for all A and Evalues. Simulation results consistently show that the best system performance will be obtained at a small A/E rate.

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