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VOLTAGE SAG MITIGATION WITH PRE-SAG BASED DYNAMIC VOLTAGE RESTORER METHOD

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ABSTRACT

Quality control issues that can cause complex stack hardware to fail operation resulting in voltage drop occurring. A short circuit to the ground in the conveyance control frame is the cause of the failure. To overcome this failure, the elective arrangement of the stack safeguard against the voltage registers with electronic control based on a device that provides a three-phase voltage source can be controlled, namely a dynamic voltage restorer (DVR). This research focuses on pre-sag based of DVR execution with a discovery framework placed on the input side of the control supply. The DVR incorporates the voltage difference between the annoying droop and pre-fault state. The effect of a two-phase short circuit to ground fault with four different transformer winding arrangements was carried out using Matlab/Simulink. The simulation results show that various distribution transformer arrangements will produce various voltage drop effects. Phase shift and maintain stack voltage between 0.9-1.1 pu of real voltage to compensate for voltage-sag.

Keywords: *Voltage Sag, DVR, Injection Transformer, Pre-Sag, Two-phase fault*

1. INTRODUCTION

The voltage sag performance causes the load equipment to not operate, which will result in considerable losses for consumers of electrical energy. Most of the issues that occur on the grid, transmission and distribution aspect are voltage sags. Sources of droopy is troublesome to find, as they occur within or outside the facility. For example, a voltage drop in an exceedingly householding device indicates that a voltage drop is a smaller amount possible to wreck the equipment. However, equipment performance degrades, but the duration is usually short enough for the type of voltage drop most residential customers experience. Therefore, this issue is a serious concern especially for critical and sensitive loads in power quality processes. In addition, the impact on the malfunction of voltage sensitive control equipment, working in industries that stop operating during the product process.

Several studies have shown that, power system has disturbances, load variations, transformer energy and large induction motor launches occur in the power system [1]. To solve this problem, dynamic voltage restorer (DVR) equipment is used. Low cost, small and fast response done by DVR to reduce voltage drop [2]. The DVR is a circuit connected to a solid-state device whose voltage is injected into the system to control the load-side voltage. The point of common coupling (PCC) in the distribution system installed among supply and feeder [3].

The compensatory forced on the DVR is pre-sag compensation, phase compensation both phase angle and magnitude, and energy optimization approach. The pre-sag approach continuously detects the supply voltage and any disturbance in the forced of voltage. Therefore, adjusting of the voltage difference between the sag on the PCC and the pre-fault condition is required. Moreover, the load voltage is returned to the condition before the disturbance [4].

Several studies of power system fault on voltage sag mitigation have been conducted, such as as three phase to ground, phase to phase and two phase to ground, single phase to ground, has been created in transmission line model for generation of different types of voltage sag using Matlab/Simulink [1].

The functions, configurations, elements, operating modes, voltage injection approaches, and closed loop control of the DVR produce voltage has been investigated by [2]. In other hand, the configuration of DVR has been proposed by [3 by developed of d-q-0 regulator to mitigate of sags and swells voltage during single line to ground and three phase faults.

The Interline Dynamic Voltage Restorer (IDVR) correspond of several DVRs has been proposed by [4] to compensates voltage sag in feeder at other DVRs which is replenish the energy in the common DC link stoutly [4]. The compensation voltages in DVR based on dq0 algorithm is argued in order to fitted control limitations and reduced compensation, a voltage control has been proposed by [5]. Moreover, to addressing harmonics, the fuzzy controller-based DVR has been proposed by [6]. Whereas, A simple and practical approach has been proposed by [7] by calculating RMS voltage over one cycle and one- half cycle deployed on the magnitude variation and phase-angle jump for each phase are examined and analyzed.

An approach for compensation of voltage sag using dynamic sag corrector and DVR has been proposed by [8]. Adaptive proposition based Improved Linear Tracer Sinusoidal (TIALS) is used for extraction of basic reference load voltage immediately and precisely in order to mitigate power quality problem and, modeled using RT- LAB and MATLAB/ SIMULINK has been proposed by [9]. The control approach based on dq0 conception is set up veritably effective for associating and clearing any power quality disturbance has been proposed by [10] in distribution system. Moreover, [11] has been propose control voltage sag which are mitigates phase jumped in the load voltage by perfecting the whole sag compensation time.

The voltage compensation has been mitigated by [12] to control algorithm abc-dq0 scheme which has excellent capabilities, while reference vector generating has been used to enhance voltage restoration using discrete PWM pulse generator which proposed by [14].

To improved DVR performance a quasi-impedance of source inverter with several variable control has been discussed by [15]. Those analytical and proposed methods is not enough to addressing problem of transformer voltage sag. To mitigate those problem, root cause of problem which caused by two-phase short circuit to the ground by varies of transformer winding are investigated.

Most of the disturbances in utility systems are single line to ground faults (SLGF). Three-phase errors can be more severe, but are much less common. Across the system, the average urban customer may see 1 or 2 breakdowns a year whereas the same customer may experience more than 20 voltage drop events a year depending on how many circuits are fed from the substation. Therefore, voltage sag mitigation needs to be completed.

2. PROPOSED SYSTEM METHODOLOGY

A duration of voltage sag ranging from halfway cycle up to one minute by depreciation of RMS of 1 to 9 pu. [16]. It has two main parameters namely magnitude and time duration. Research model should be suitable to describe the circumstance of sag in voltage source and also its load voltage mitigation.

The investigation model was designed in several pathway. The first step was determining fault model of voltage slack in the form of short circuit two- phase to ground of distribution line. Another step was determining discovery and control approach to attain the error signal. The third step was determining DVR model installed on a network series to induce injection voltage. The coming step was determining the investigation model.

The voltage sag was determined by the cause of the short circuit to ground into four types based on variation of configuration transformer connection in the distribution system. These types of faults in this investigation were shown in Table 1.

Table 1: Fault Types.

Short circuit to ground	Transformer Configuration
Two phase A, B to ground	Yg/Yg Connection
Two phase A, B to ground	Yg/Δ Connection
Two phase A, B to ground	Δ/Δ Connection
Two phase A, B to ground	Δ/Yg Connection

The fault model which reflects to voltage disturbance has shown in Figure 1. The fault block is placed on the line 3 phase of 20 kV before the transformer of 20 kV 380V. While the Sag discovery is placed on bus A.

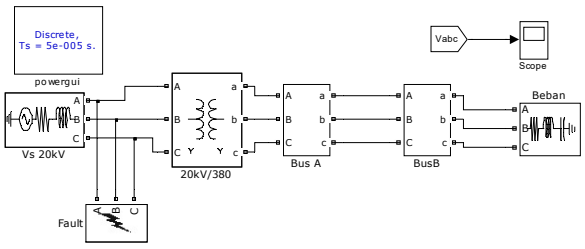

Figure 1: Fault Model Voltage Sag

According to IEEE P1564, a 70% drop in a 230-V system means the voltage drops to 161 V. So, with that 70% drop all that's left is 30% of the voltage. To obtaining the sag is to use an RMS voltage, several methods is proposed such as (i) From Fault to Trip; (ii) Reducing the Number of Faults; (iii) Reducing the Fault-Clearing Time; (iv)

Changing the Power System. moreover, several voltage sag devices are used to reduce sag, which are: Device Voltage Restorer (DVR), Uniform Power Quality Conditioner, Uninterruptable Power Supply, Motor-Generator Sets, Ferro resonant, Constant Voltage Transformers, Static transfer switch.

Only the DVR could compensate for the voltage drop due to sag very well. To protect sensitive loads from supply side interference; it can also act as a series active filter, isolating the source from the harmonics generated by the load the DVR is connected series. Whenever voltage drop is occurred, a DVR compensate high fluctuations in sag drop accompanied by frequent flicker at utility systems.

2.1. Dynamic Voltage Restorer (DVR)

The DVR unit comprises of 5 basic elements, namely detection and control unit, DC energy storage, voltage source inverter (VSI), injection transformer and filters [5] shown in Figure 2. A DC energy storage unit is used to provide the energy required to increase the injection voltage.

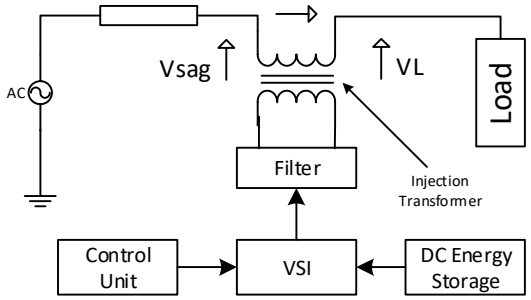

Figure 2: Basic Configuration of DVR [2]

Figure 2 shows the basic configuration of the DVR, when the source voltage (Vs) is lowered, the DVR injects the VDVR series voltage through the injection transformer so that the magnitude of the VL sensitive load voltage can be maintained to its nominal value. The injected voltage is expressed in Eq. (1).

$$V_L = V_{sag} + V_{DVR} \quad (1)$$

The VSI unit is used to convert the DC voltage into a sinusoidal AC voltage (injection voltage). While the main task of the filter is to maintain the compatibility of the voltage content generated by the VSI below the permissible level.

2.2. Abc To Dq Transformation

The metamorphosis abc to dq is made from the Clarke and Park transformation matrices. The three-phase system is converted from time area elements in the direct abc frame of reference, quadrature, and zero in the rotation of the reference frame. The transformation is used to rotate the frame of reference of a three-phase AC waveform similar to a DC signal. The dq transformation is often used to simplify the analysis of three-phase synchronous machines or to calculate the control of three-phase inverters.

The Clarke transform or abc to $\boldsymbol{\alpha\beta}0$ transformed is a space vector transformation of time-based signals from natural three- phase coordinate system V_{abc} into a stationary two-phase reference frame of $V\boldsymbol{\alpha\beta}0$. The 0- element is zero for balanced three-phase systems. The transformation matrices shown in Eq. (2).

$$\begin{bmatrix} V_0 \\ V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2)$$

The Park transform converts a vector in a stationary reference frame of $\boldsymbol{\alpha\beta}$ to a reference frame dq. The transformation matrix is shown in Eq. (3). This equation takes a two-phase quadrature voltage along a stationary frame and converts it into a two-phase synchronous frame.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} cos\,\theta & sin\,\theta \\ -sin\,\theta & cos\,\theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (3)$$

The inverse transformation dq0 to abc converts the time domain, quadrature, and zero components into components of a three-phase system in the abc frame of reference.

Eq. (4) defines the inverse transformation of the park matrix from the time domain, quadrature (dq) into a two-phase stationary frame of reference.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (4)$$

Eq. (5) defines the inverse transformation of the Clarke matrix from a two-phase reference frame to a three-phase system in an abc reference frame.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (5)$$

2.3. Phase Lock Loop (PLL)

The task of the PLL is to maintain the coherence between the frequency of the input signal and the frequency of the output signal respectively through phase comparison. The PLL Block Diagram shown in Figure 3 consists of three basic elements, such as: a phase detector, a loop filter, and a voltage-controlled oscillator (VCO).

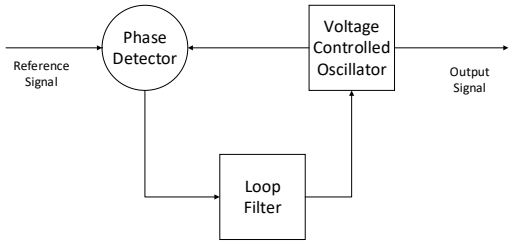

Figure 3: PLL basic diagram block

The VCO signal phase and the frequency of the incoming reference signal is compared. The resulting error voltage then generated. It's corresponding to the phase difference between the two signals. The error signals of the phase detector pass through the loop filter. After going through the loop filter the error signal is applied. Finally, the PLL block is used to generating a unit-in-phase sinusoidal waveform as the main voltage [3,5].

2.4. Pre-Sag Compensation Method

The DVR based on the Pre-Sag method tracks the supply voltage continuously and detects any disturbance, then injects the voltage difference between the sag and the ideal pre-fault condition. In this way, the load voltage is returned to the same angle and phase magnitude as the nominal pre-sag voltage. Therefore, it is highly recommended for non-linear loads that are sensitive to phase angle jumps [2].

However, higher rated energy storage devices and voltage injection transformers are required. Non-linear loads require large voltage and phase angle compensation as shown in Figure 4.

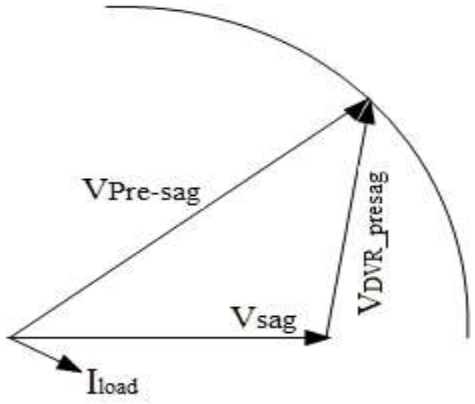

Figure 4: One Phase Vector Diagram

The magnitude of the voltage injection is the difference between the ideal pre-fault and sag conditions as shown in Figure 4. The DVR voltage injection is given in Eq. (6).

$$\overrightarrow{V_{DVR}} = \overrightarrow{V_{Pre-sag}} - \overrightarrow{V_{Sag}} \quad (6)$$

2.5. The Control Scheme

The proposed DVR control scheme from abc to dq0 transformation is used. The ratio of the rated voltage (Vs) and the reference voltage (Vref) is proposed. Voltage sag detection is placed on bus A after the distribution transformer is shown in Figure 5.

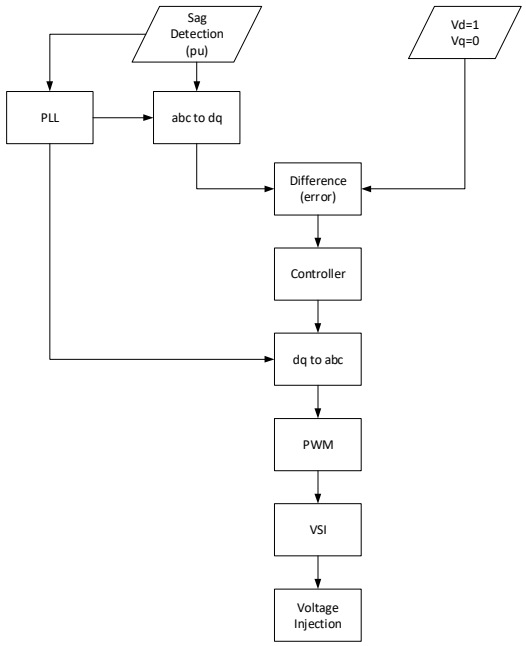

Figure 5: The Control Scheme of Voltage Sag

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The detection of the occurrence of a voltage drops, measured the compensation voltage, generate a PWM inverter trigger pulse, correct errors in series voltage injection, and stop the trigger pulse when the event has passed are the tasks of DVR controller [5, 10]. The transformation method provides information about the magnitude (d) and the phase shift (q) from the beginning of time to the end of the voltage drop. Quantity is expressed as an instantaneous space vector.

An error signal has been detected whenever supplied is dropped by 90% of rated. In addition, the error signal is transformed into a three-phase abc form. The fault signal is used as a control signal which produces a commutation sequence pattern for the VSI power switch using Pulse Width Modulation (PWM). Voltage is controlled by modulation. The modulated signal is required as a gate-insulated bipolar transistor (IGBT) trigger to provide an injection voltage to the charge drop voltage that occurs through the injection transformer.

2.6. Research System Model

The proposed model of this research is designed using Matlab/Simulink which fault detection is placed on Bus B voltage source after the 20kV/380V step-down transformer which is described in Figure 6. Two-phase short circuit a and b to ground is used as a fault model. The step-down transformer is distinguished by its three-phase winding connection. There are four types of primary and secondary transformer connection models, namely Y/Δ, Y/Y, Δ/Δ, and Δ/Y. This research model will be used to determine the difference in the sagging stress characteristics and their recovery under load stress. in case of short circuit of phase's, a and b to ground, the proposed model is used.

The detection results are processed in the control circuit. If a sag occurs, the control circuit will generate an error signal. Furthermore, the error signal is fed to the PWM to produce a modulated signal as the input of the VSI circuit. The output of this circuit is the injection voltage which will be passed through the injection transformer.

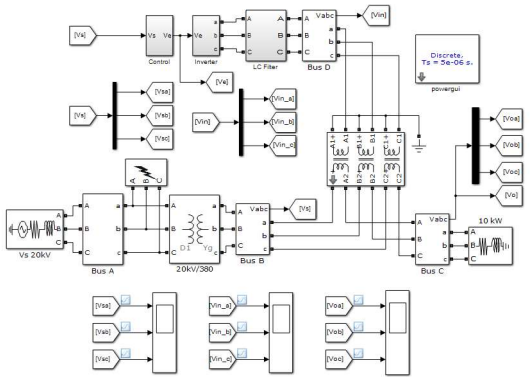

Figure 6: Proposed Research Model

The principle of voltage injection is that if there are two voltage sources with the same frequency and phase connected in series, it will produce a large voltage which is equal to the number of series voltage sources. The load stress can be expressed in Eq. (7).

$$V_L = V_{sag} \sin\theta + V_{inj} \sin\theta \qquad (7)$$

where VL is the load voltage, V_{sag} is the sag, and V_{inj} is the injection voltage

To get the expected results, mitigating the magnitude of the voltage and phase angle, the steps that must be taken are determined according to the diagram as shown in Figure 7.

Based on the research model as shown in Figure 6 and the flow chart shown in Figure 7, simulations were carried out with the parameter values as listed in Table 2.

Table 2: Research Model Parameters.

Parameter	Value
3-phase supply voltage	20 kV
Frequency	50 Hz
Distribution Transformer	10 MVA; 20 kV/380 V
Voltage Source Converter	IGBT 3 arms
DC source voltage	500 V
Injection Transformer	100 MVA; 380 V/570 V
Load	10 kW; Q_C 100 var;

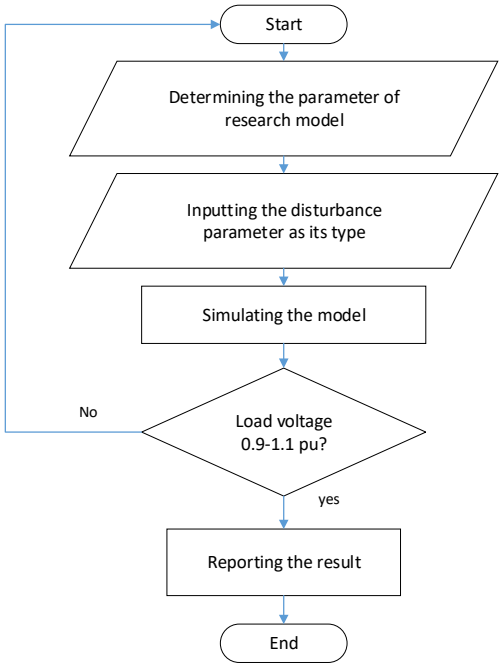

Figure 7: Research Flowchart Diagram

3. RESULTS AND DISCUSSION

The system parameters are listed in Table 2. During the voltage sag condition, it is assumed that the magnitude of the sensitive load voltage is maintained at 0.9-1.1 pu. Each error type starts at 40 ms and will stay up to 140 ms for a total duration of 100 ms. The line fault model consists of a 20 kV 50 Hz three-phase source block fed through a 20 kV/380 V, 100 MVA, Yg/Yg transformer to a 10-kW resistive inductive load. There is a fault block located in the source line on bus A which is used to simulate various types of transformer winding connections.

The simulation results are presented in a graph of voltage (pu) as a function of time. Each type of fault is displayed in six graphs consisting of three phase graphs of the sag abc voltage and three phase graphs of the abc load voltage.

3.1. Fault Type 1ST: Transformer Yg/Yg

The type 1 fault simulation is shown in the first simulation. Starting with providing a disturbance in the form of a short circuit of phase A and phase B to ground. The simulation results are shown in Figures 8, 9 and 10.

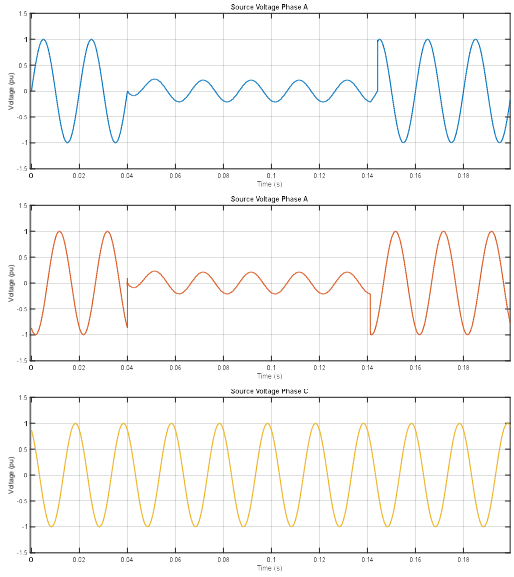

Figure 8. Source Voltage (a) Phase A, (b) Phase B, (c) Phase C

The source voltage of phase A decreased by 0.8 pu with a duration of 100 ms starting from 40 ms as shown in Figure 8. While Figure 8 (b) is for phase B voltage. In addition, phase C voltage is not affected by the disturbance.

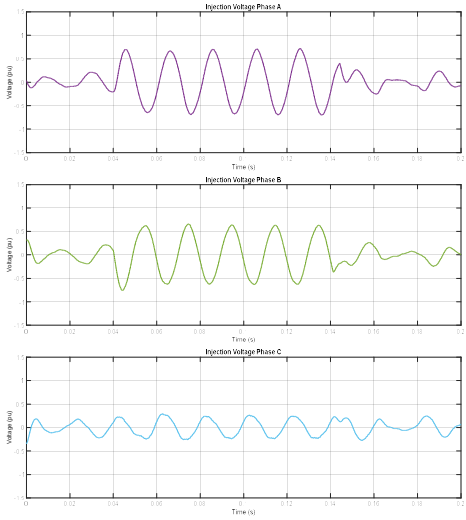

Figure 9: Injection Voltage (a) Phase A, (b) Phase B, (c) Phase C

Figure 9 illustrates the injection voltage at each phase used to mitigate the load voltage.

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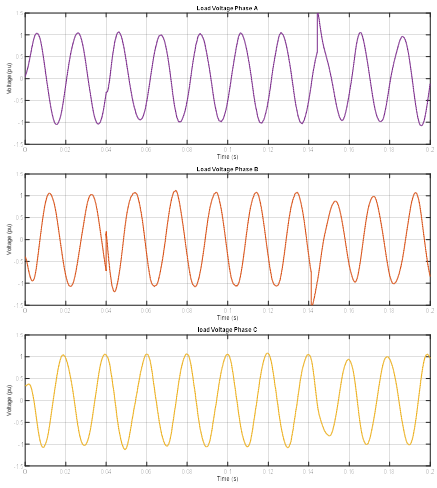

Figure 10: Load Voltage (a) Phase A, (b) Phase B, (c) Phase C

The results of the Type 1 mitigation are shown in Figure 10. A decrease in the magnitude of the source voltages of phase A and B by 0.8 pu could recover, so that the load voltage returns within 0.9-1.1 pu.

3.2. Fault Type 2ND: Transformer ϒG/Δ

The type 2 fault has been demonstrated in the second simulation. Starting with providing a disturbance in the form of a short circuit of phase A and phase B to ground. The simulation results are presented in Figures 11 until 13.

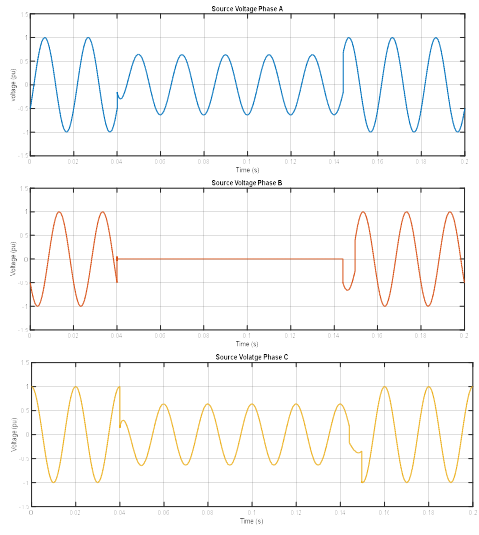

Figure 11: Source Voltage (a) Phase A, (b) Phase B, (c) Phase C

As shown in Figures 11 (a) and 11 (c), the source voltage in phase A and phase C decreased by 0.36 pu with a duration of 100 ms starting from 40 ms. While the source voltage in phase B is reduced by 1 pu along with the other phases shown in Figure 11 (b).

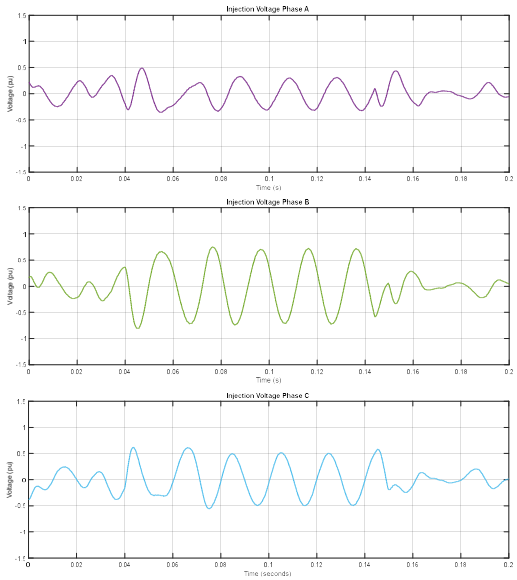

Figure 12: Injection voltage (a) Phase A, (b) Phase B, (c) Phase C

The injection voltage at each phase illustrated in Figure 12 is used to mitigate the load voltage.

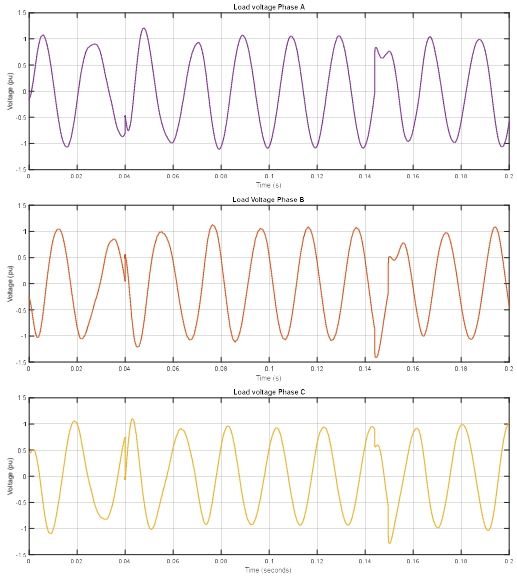

Figure 13: Load Voltage (a) Phase A, (b) Phase B, (c) Phase C

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The results of the type 2 mitigation are shown in Figure 13. The reduction in the magnitudes of phases A and C of 0.36 pu and Phase B of 1 pu can be recovered so that the load voltage returns in the range of 0.9-1.1 pu.

3.3. Fault Type 3RD: Transformer Δ/Δ

The third type of error has been demonstrated in the third simulation. Starting with providing a disturbance in the form of a short circuit of phase A and phase B to ground. The simulation results are presented in Figures 14, 15, and 16.

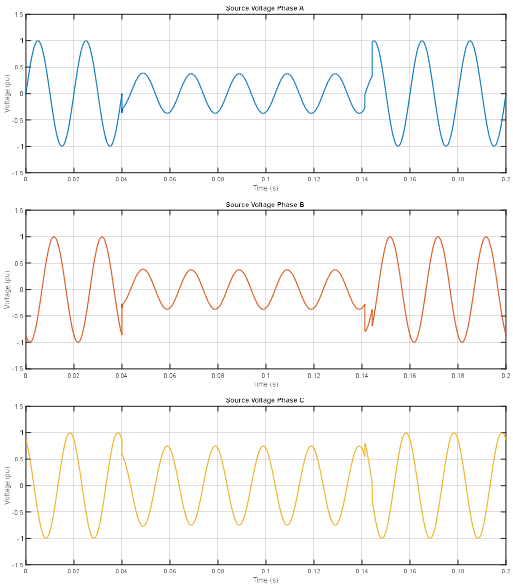
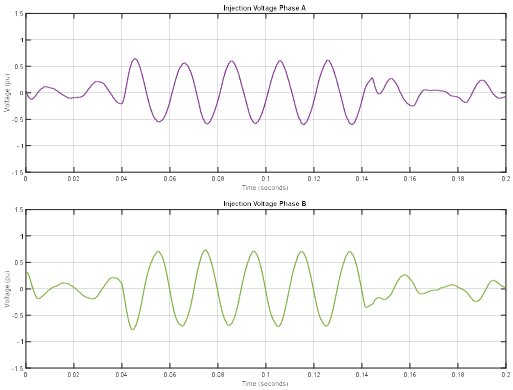


Figure 14: Source Voltage (a) Phase A, (b) Phase B, (c) Phase C

It was shown in Figures 14 (a) and 14 (b), the source voltage in phase A and phase B has decreased by 0.62 pu by duration of 100 ms starting from 40 ms. While the source voltage in phase C has decreased to 0.25 pu along with other phases as shown in Figure 14 (c).



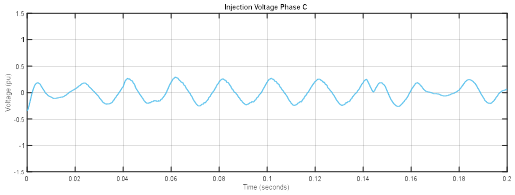


Figure 15: Injection Voltage (a) Phase A, (b) Phase B, (c) Phase C

The injection voltage of each phase is shown in Figure 15, which is used to mitigate the load voltage. The load stress mitigation is shown in the following graph:

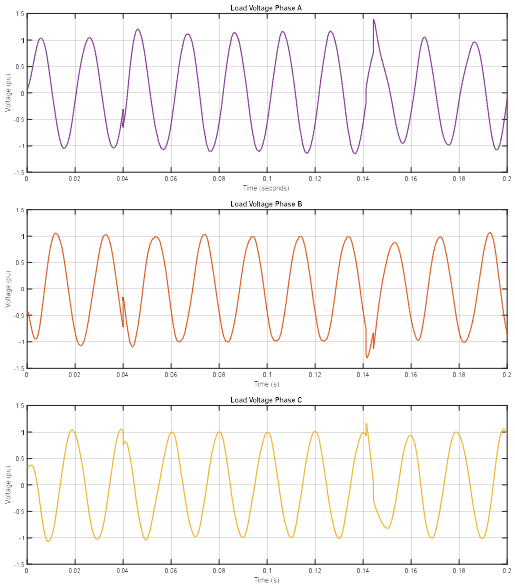


Figure 16: Load Voltage (a) Phase A, (b) Phase B, (c) Phase C

The analysis of the results of the 3rd fault mitigation is shown in Figure 16. The decrease in the magnitude of the source voltage of phase A and phase B of 0.62 pu and Phase C of 0.25 pu can be recovered so that the load voltage returns in the range of 0.9-1.1 pu.

3.4. Fault Type of 4TH: Transformer Δ/YG

The fourth type of error has been demonstrated in the 4th simulation. Starting with providing a disturbance in the form of a short circuit of phase A and phase B to ground. The simulation results are presented in Figures 17, 18, and 19.

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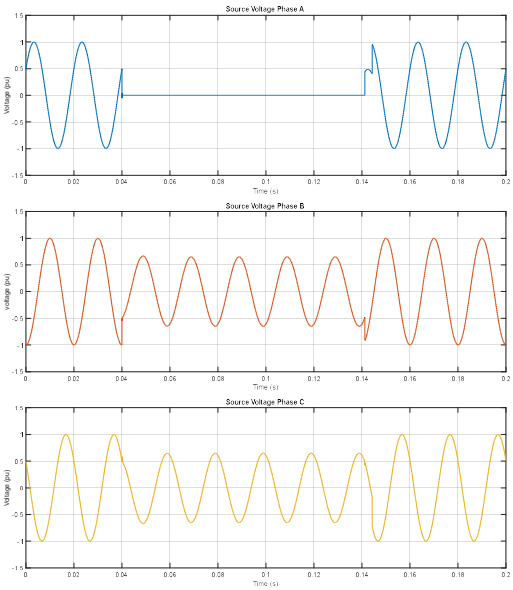

Figure 17: Source Voltage (a) Phase A, (b) Phase B, (c) Phase C

It was shown in Figures 17 (a), the source voltage in phase A and phase B has decreased by 1 pu by duration of 100 ms starting from 40 ms. While the source voltage in phase C has decreased to 0.35 pu along with another phase's as shown in Figure 17 (b) and 17 (c).

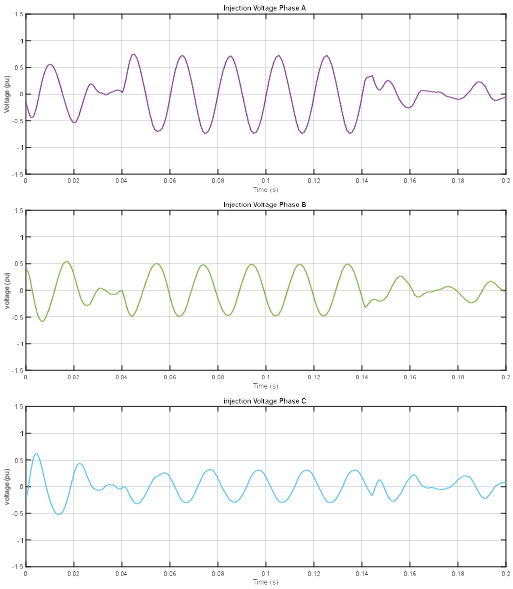

Figure 18: Injection Voltage (a) Phase A, (b) Phase B, (c) Phase C

The injection voltage of each phase is shown in Figure 18, which is used to mitigate the load voltage. The load stress mitigation is shown in the following graph:

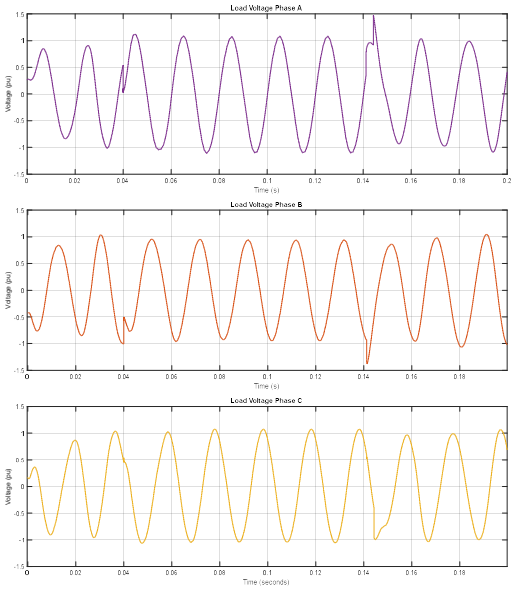

Figure 19: Load Voltage (a) Phase A, (b) Phase B, (c) Phase C

The analysis of the results of the 4th faults mitigation is shown in Figure 19. The decreased of the magnitude of source voltage of phase A is 1 pu and phase B Phase C are 0.35 pu could recovered therefore the load voltage was returns in the range of 0.9–1.1 pu.

Table 3: the results of mitigation of four types of faults using pre-sag-based DVR method.

Type	Voltage Sag (pu)			Mitigation (pu)			Impuls (pu)
	A	B	C	A	B	C	
1	0,8	0,8	0	1	1,08	1,03	Ph a = 1,5 Ph b = 1,5
2	0,36	0,36	1	1.02	1.06	0,95	Ph b = 1,45 Ph c = 1,3
3	0,62	0,62	0,25	1,1	1	1	Ph a = 1,4 Ph b =1,3
4	1	0,35	0,35	1,02	0.98	1	Ph a = 1,5 Ph b = 1,45

Four types of faults had been presented and the results analysis has shown in Table 3. It's shown that the pre-sag based DVR able mitigate load voltage in the range of 0,98 pu up to 1,1 pu. The simulation results showed that all types of faults

resulted sag duration of 100 ms at the same time, and produced a different sag characteristic.

To overcome the drawbacks of the DVR, a modular multilevel converter (MMC) is used to ensure effective power delivery at nominal power in the absence of a transient voltage change during a sag [1].

To overcome voltage sag with a more accurate and faster future database-based DVR, adaptive neuro-fuzzy inference systems (ANFISs), and fuzzy logic controllers based on DVR to mitigate voltage sag can be implemented for better results.

4. CONCLUSION

The proposed pre-sag-based DVR method can reduce the four types of voltage sag from the tested disturbance. Timing recovery to mitigate stress loads has a performance of 0.9 - 1.1 pu which is the same as a disturbance duration of 100 ms. Therefore, the phase shifted that occurs can be mitigated by 1200 in phases A and B.

This study has proven that the application of DVR can overcome various kinds of disturbances that occur in the transformer and can reduce voltage sag well. So, it's recommended for use in transformer networks with large loads, thus power quality will be maintained in accordance with established standards.

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