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# FPGA IMPLEMENTATION OF OPTIMIZED FIR FILTER FOR ECG DENOISING USING PERES REVERSIBLE LOGIC GATE

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**ABSTRACT**

In recent days, the Finite Impulse Response (FIR) filter plays a crucial role in denoising Electro Cardiogram (ECG) signals in an effective way. In this paper, an efficient Vedic multiplier-based 8-tap FIR filter architecture with a Carry Save Adder using Peres reversible logic gate is proposed for ECG signal denoising with low power, area and delay. The low power consumption is achieved by the incorporation of Vedic multiplier and Carry Save Adder architectures, whereas the delay is reduced by the incorporation of reversible logic gate-based realization of filter architecture and the Urdhva Tiryagbhyam Sutra based Vedic multiplication process. Further in this work, the FIR filter is first designed using the MATLAB filter design & analysis (FDA) tool, then with the corresponding filter coefficients, the filter is implemented in FPGA using Verilog Hardware description language (HDL). The implemented FIR filter architecture for ECG signal denoising performs the noise reduction with a better Mean Square Error (MSE) of 0.41 and a Signal Noise Ratio (SNR) of 22.36 dB which is better than the other reported filter's performance in the literature. Also, the proposed FIR filter FPGA implementation using the Xilinx tool in the Virtex6 xc6vcx75t family consumes 41 LUTs & 46 slices, 21 no. of. flip flops with a delay of 5.19ns and 0.081 mW power. Thus, the proposed Architecture results, in a 30% reduction in power, 20% reduction in area and more than 15% improvement in delay than the reported Filter structures in the literature.

**Keywords:** *FIR Filter, Reversible Logic Gate, Peres Gate, 8-Tap, ECG Signal Denoising, Low Power, Reversible Gate, Peres Gate, Vedic Multiplier, Carry Save Adder.*

## 1. INTRODUCTION

FIR filter is one of the important building blocks in all signal denoising applications because of its high stability, accuracy, and versatile nature when compared with IIR and analog filters [1,2]. Generally, the transposed form FIR filter is used in most of the FPGA-based implementations wherein the adder and multiplier play a significant role in all the designs [3,4]. Also, the usage of the FIR filter in signal processing applications leads to very good linear phase response with precision and fractional arithmetic in multirate signal processing [5,6]. Though the FIR filter has many advantages in signal processing systems, the usage of multipliers and adders in the Very Large-Scale Integrated (VLSI) Architecture requires more computation, area, and power [7-9].

Numerous FIR filter design FPGA implementation architectures like FIR filter architecture using common subexpression elimination (CSE) [10], Optimized Higher-order FIR filter using LUT & DSP reduction [11], High throughput architecture [12], GA based FIR filter [13], Energy Efficient FIR filter [13], Reconfigurable block-based FIR filter [15] and optimized Multiplier based FIR filter [16] have been proposed over the decades in the literature to perform effective filtering operations on the signal. However, the aforementioned FIR filter implementation mainly focuses on the hardware utilization aspect and not on the efficiency part [17-22]. Moreover, only a few of the aforesaid architectures are intended for ECG signal denoising. To overcome this gap, in this research work, a Carry Save Adder (CSA) and Vedic multiplier-based FIR filter design is proposed, wherein the input coefficients of the filter are decided using the MATLAB FDA tool. Thus, the incorporation of the Vedic multiplier and Carry Save Adder in the proposed work improves filter performance, which

is comparatively better than the conventional FIR filter design implementations. Furthermore, it is also more suitable for ECG signal denoising applications effectively.

This research paper is organized as follows, Section-2 elaborates on the existing FIR filter architectures with their advantages and disadvantages, and Section-3 briefly discusses the problem statement and solution to existing architectures discussed in the literature. Section-4 presents the proposed methodology of the FIR filter architecture for ECG signal denoising, and Section-5 explains the experimental results and performance comparison of the proposed FIR filter with conventional multiplier adder-based FIR filter architectures reported in the literature. Finally, Section-6 concludes the proposed FIR filter design with its advantages.

## 2. RELATED WORK

Various FIR filter architectures have been reported over the decades, but only a few are focused on ECG signal denoising applications [23-29]. This section elaborates on the few noteworthy FIR filter architectures. For instance, the FIR filter architecture proposed by Sudipta. et.al [11] involves a common subexpression elimination by the grouping of the common coefficient terms to achieve logic operator & depth minimization. Though the algorithm consumes less area and power, it has less efficiency in filtering. Later Maamoun. et.al [12] improve the FIR filter architecture using simultaneous DSP and LUT utilization for high order filtering of the signal but is not suitable for ECG applications. Subsequently, Patali. et.al [13] proposed a high throughput FIR filter structure with modified CSLA adders, which performs comparatively better than the aforesaid architectures. On the other hand, it filters the ECG signal poorly in the presence of noise. Following the above architectures, Patali. et.al [14] and Shrivastava et al [15] proposed a linear phase energy efficient FIR filter architecture and block-based reconfigurable architecture respectively. Even though the aforesaid algorithms consume less area, delay and power don't intend to the ECG signal filtering effectively. Thus, from the analysis of the merits and demerits of the above-presented architectures, the problem statement and solution for ECG signal denoising are presented in section-3.

## 3. PROBLEM STATEMENT

This section explains the problem statement of the FIR filter architecture for ECG signal denoising and its solution to seal the identified research gap respectively. During the design of the FIR filter for ECG signal denoising, the following concerns are to be addressed by the architecture as below

i. The FIR filter architecture has to consume less power, area and delay.
ii. The FIR filter has to denoise the signal effectively with higher values of performance metrics SNR, and lower values of BER & MSE.
iii. Also, the Architecture should involve less computational complexity.
iv. Additionally, the Architecture should maintain accurate precision i.e., it should produce output without any loss in data signal values during the processing and implementation.

*Solutions:* This section explains the solution to the problem statement of the FIR filter architecture implementation. In this research work, to meet the aforesaid requirements during the FIR filter design, Urdhva Tiryagbhyam Sutra-based Vedic multiplication process and Peres reversible logic gate-based realization is incorporated which in turn improves the delay of the FIR filter architecture. Additionally, the Urdhva Tiryagbhyam Sutra Vedic multiplier (VM) structure and Carry Save Adder (CSA) structure-based FIR filter design are proposed, which leads to low power, less area and high-speed FIR filter architecture. Moreover, in the proposed methodology, Urdhva Tiryagbhyam Sutra-based Vedic multiplier and CSA adder-based realization preserve the data precision without any loss in signal values and also effectively does the ECG denoising with good performance metrics.

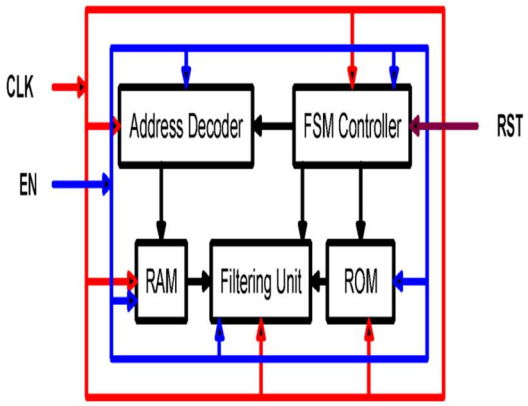


*Figure 1: Proposed FIR Architecture for ECG signal Denoising applications*

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## 4. PROPOSED FIR FILTER ARCHITECTURE

The proposed architecture of the Vedic Multiplier and Carry Save Adder-based FIR filter is given in Fig.1. It consists of an Address decoder, Random Access Memory (RAM), FSM Controller and the main FIR Filtering unit. For each clock cycle, the address decoder generates the address and then from the respective address location, the ECG signal data values are read from the RAM and processed using the FIR filtering unit. The filtering operation is controlled by the FSM controller, and the same is iteratively repeated for the successive samples of the ECG signal data. The entire architecture is implemented in 16-bit precision, therefore the Vedic multiplier, Carry Save Adder and RAM used are of 16-bit precision [20-39]. Also, in the main filtering unit, the filter coefficients are stored in ROM wherein the values of the coefficients are determined using the MATLAB FDA tool.

In the proposed architecture, the RAM used to store the noisy ECG signal values is of 16-bit width and its depth is selected based on the number of samples present in the ECG signal. Further, the address decoder is an up-counter that produces the respective address for the stored location of ECG signal data in RAM. Then, using the generated address, the FSM controller fetches the ECG signal values and carries out the filtering operation in the main filtering unit.

### 4.1 Proposed FIR Filtering Unit & Operation

For an input signal x(n), the filtering operation is defined as the weighted sum of the most recent input signal values. The above-said filtering operation is given by equation-1.

$$y(n) = \sum_{k=0}^{n} h(k)x(n-k) \quad (1)$$

Here the signal y(n) indicates the filtered output of the input signal x(n), h(k) indicates the FIR filter transfer function and x(n-k) represents the shifted version of the input sequences. Here, the 'n' varies from 0 to n, wherein the n values primarily depend on the number of samples in the input signal. Further, the values of the h(k) are decided based on the filter coefficients obtained using the MATLAB FDA tool. Thus, from the above equation, the FIR filter structure is constructed, which primarily consists of a delay element, multiplier, and adder for carrying out the filtering operation.

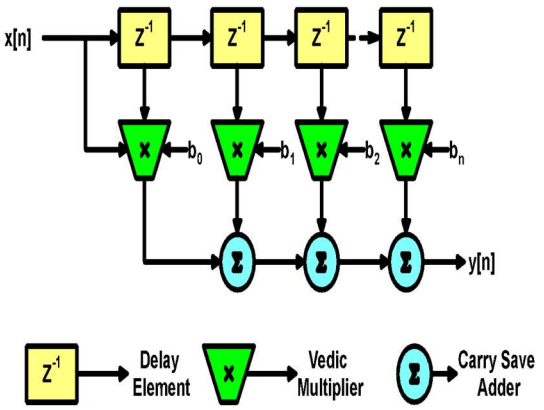


*Figure 2: Internal Architecture of the Proposed FIR Filtering Unit using Vedic Multiplier and Carry Save Adder*

Therefore, in this research work, based on the basics of FIR filter operation the proposed FIR filter structure is constructed using Vedic Multiplier, Carry Save Adder and Delay element in 16-bit precision. The sample proposed n-tap FIR filter structure used in this research work is shown in Fig.2. Here, the input signal x(n) and its shifted values x(n-k) using delay element $Z^{-1}$ are multiplied with filter coefficients b0 to bn respectively, using a Vedic Multiplier. Then the multiplied output values are added by the Carry Save Adder to produce the filtered output.

### 4.2 Proposed Vedic Multiplier

In the FIR filtering operation, multiplication plays a vital role. Henceforth, in the proposed FIR filter architecture, the multiplier is designed using the Urdhva Tiryagbhyam Vedic Sutra to achieve less low power and less delay. Generally, the aforesaid Vedic sutra involves vertical and crosswise multiplication of multiplicand and multiplier as shown in Fig.3. For example, the multiplication of the 2-bit binary number a1a0 x b1b0 involves the first vertical multiplication of the least significant bits (LSB) a0 and b0. Then the LSB of the multiplicand is multiplied with the higher-order bits and vice versa in a cross-wise manner i.e., a1b0 x a0b1. Thus, from the vertical and crosswise operations, the final sum output LSB bit and higher-order bits are produced, respectively. The entire operation of the Urdhva Tiryagbhyam Vedic Sutra using vertical and crosswise multiplications is given by the below equations 2 & 3.

$$S0 = a0b0 \quad (2)$$
$$C1S1 = a1b0+a0b1 \quad (3)$$
$$C2S2 = C1 + a1b1 \quad (4)$$

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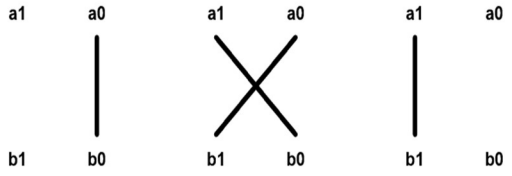


*Figure 3: Urdhva Tiryagbhyam Sutra based 2 x 2 Vedic Multiplication*

Thus, in this research work, based on the Urdhva Tiryagbhyam Vedic Sutra, the multiplier is designed and implemented. In the proposed multiplier, further to achieve the low power and delay, the Peres Reversible logic gate-based Carry Save Adder is incorporated into the multiplier design. For easy understanding of the proposed Vedic Multiplier architecture, a 4 x 4 Vedic multiplier structure is illustrated in Fig.4. The same structure is extended for 16-bit in the proposed works and implemented effectively in FPGA. In the multiplier architecture, vertical and crosswise multiplication is performed in the lower order multipliers and the result of each is successively added by the Carry Save Adder to produce the output. In the proposed ECG signal FIR filter architecture, a 16-bit Vedic Multiplier and Carry Save Adder is designed and implemented for effective filtering.

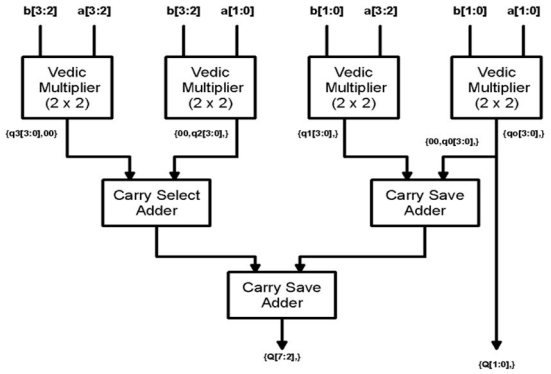


*Figure 4: Architecture of Urdhva Tiryagbhyam Sutra 4 x 4 Vedic Multiplier*

### 4.3 Proposed Carry Save Adder

Additionally, in the proposed FIR ECG signal filter, to achieve high speed, a Peres reversible logic gate-based Carry Save adder is proposed and implemented. The Carry Save Adder involves the switching of the output calculation for a fixed value of carry input (i.e., for the input values of carry '1' and '0', the output sum and carry out are calculated parallelly). Finally, the output is selected based on the carry values using a multiplexer logic. The proposed Carry Save Adder architecture for 4-bit addition is illustrated pictorially in Fig.5 for easy understanding, wherein the proposed work, a 16-bit Carry Save Adder is designed and implemented using Peres Reversible logic gates.

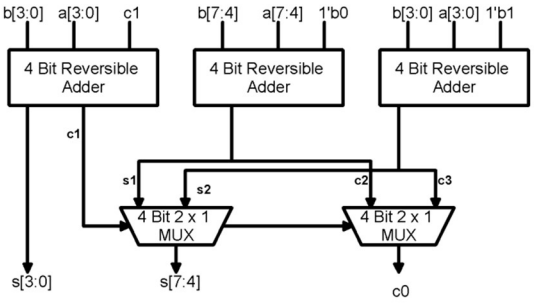


*Figure 5: Architecture of 4-bit Carry Save Adder.*

### 4.4 Peres Reversible Logic Gate & Single bit Full Adder

The reversible logic gate has gained more attention in most applications like quantum computing, low-power CMOS design, signal processing, and nanotechnology due to its minimum energy conservation and reduced delay with high performance. In logic gates and circuits, energy loss is an important consideration that leads to a loss of information, whereas the same circuit is constructed using reversible logic gates to recover and restore the information. Therefore, the reversible logic gate-based design is likely to have a high demand in high-speed power-aware circuits. Therefore, in the present research work, the Peres Reversible logic gate is considered for the design of entire architectural units. The functionality and structure of the Peres reversible logic gate are shown in Fig.6, which consists of three inputs and outputs. Also, in this gate, the first output is maintained as a garbage value, and the remaining two outputs are considered as the primary outputs. Further in this research work, using the reversible logic circuit, the one-bit full adder shown in fig.7 is constructed and it is used in the construction of the Carry Save Adder and Vedic multiplier. Thus, the reversible logic gate-based FIR filter architecture improves the overall performance when compared with the conventional logic gate-based designs.

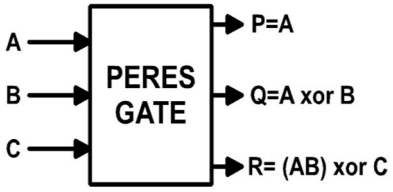


*Figure 6: Peres Reversible Logic Gate.*

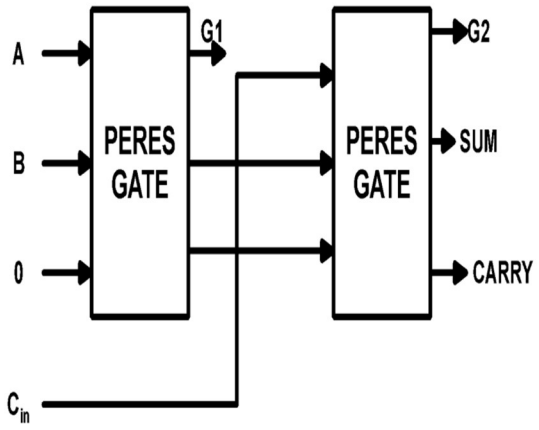


*Figure 7: Single bit full adder using Peres Reversible Logic Gate.*

## 5. EXPERIMENTAL RESULTS AND DISCUSSIONS

This section discusses the experimental results of the proposed FIR filter design using MATLAB and Verilog Hardware Description Language (HDL) based FPGA implementation. Initially, the entire system is modeled in MATLAB and simulated for the noisy ECG data values. Then the efficiency of the filtering is analyzed with the parameters Signal to Noise Ratio (SNR), Mean Square Error (MSE), and Bit Error Rate (BER). The values of the MSE, SNR and BER are calculated using the below equations.

$$MSE = (1/n)\sum_{i-1}^{n} Ai - Ai' \quad (5)$$

$$SNR = 10\ log\ 10\ \frac{(Output\ Signal)}{(Input\ \ Signal)} \quad (6)$$

$$BER = \frac{Number\ of\ Errors}{Total\ Number\ of\ Bits} \quad (7)$$

Generally, the MSE & SNR is the difference & ratio between the output and input signals. Here Ai' and Ai indicate the denoised signal and noisy signal, whereas the BER is the number of errors in the filtered output. Following the MATLAB implementation and analysis, the proposed system is modeled using Verilog HDL and then simulated & synthesized. For the Verilog implementation, the Xilinx Vivado Electronic Design Automation (EDA) tool is used with the device family Virtex6 xc6vcx75t.

Then in the Verilog simulation and implementation, for each clock cycle, the noisy ECG signal values are fetched from the RAM's corresponding locations and processed by the FIR filtering unit and produce the filtered ECG signal output. The Verilog simulation is carried out with a clock of 100 MHz frequency. The respective filtered output response of the Verilog simulation is shown in Fig.9. For the Verilog simulation and functional verification of the proposed FIR filter design, 3000 samples of the noisy ECG signal data are considered and for each sample value, the filtering operation is performed.

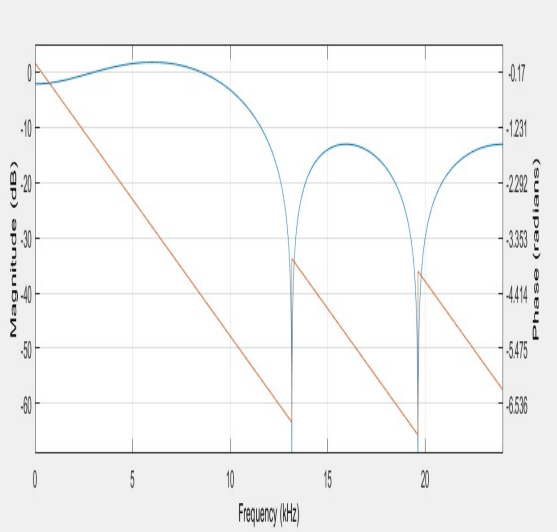


*Fig. 8 Magnitude and Phase Response of the Proposed FIR filter in MATLAB.*

For this HDL implementation, the noisy ECG signal data values are stored in RAM of 16-bit precision and the filter coefficients (-0.45, -0.17, 0.07, 0.31, 0.45, 0.31, 0.07, -0.17 and -0.45) are stored in ROM memory. The Filter is designed using the filter design FDA tool in MATLAB with the following specifications i) sampling frequency of 48000 Hz, ii) passband frequency FPASS 9600 Hz and iii) stop band frequency FSTOP 12000 Hz. The magnitude and phase response of the designed FIR filter is given in Fig.8.

The proposed simulation and implementation are carried out using an 8 GB RAM and 1Tb hard disk Intel core i5 10th gen system. For effective comparison, the proposed FIR filter for ECG signal denoising is compared with the other reported architectures in the literature and a valid performance comparison is made in terms of a lookup table (LUTs), Slices, Number of Flip Flops and frequency of operation. The values of the quantitative comparison are given in Table-1. For this effective comparison, an 8-tap filter is considered and all the reported architectures are

implemented in the Xilinx Virtex6 XC6VCX75T family. From the synthesized, it is inferred that the proposed technique is having an 80% to 10% reduction in LUTS with an average of 27% reduction in the number of flip flops utilized. Then for the slices, it consumes as low as 25% a smaller number of slices as compared to other reported architectures in the literature. Then from the synthesized results, it is found that there are no timing violations i.e., both the setup and hold timings are satisfied which is primarily identified by the positive values of the slack. Further, the synthesized RTL netlist view of the proposed FIR filter for ECG signal denoising, RTL view of the proposed Vedic multiplier using Peres Reversible logic gate and RTL schematic of the Carry Save Adder are given in Fig 9 to 11 respectively. Thus, from the above valid performance comparison, we can strongly conclude that the proposed FIR filter consumes less area when compared to the other reported FIR architectures in the literature.

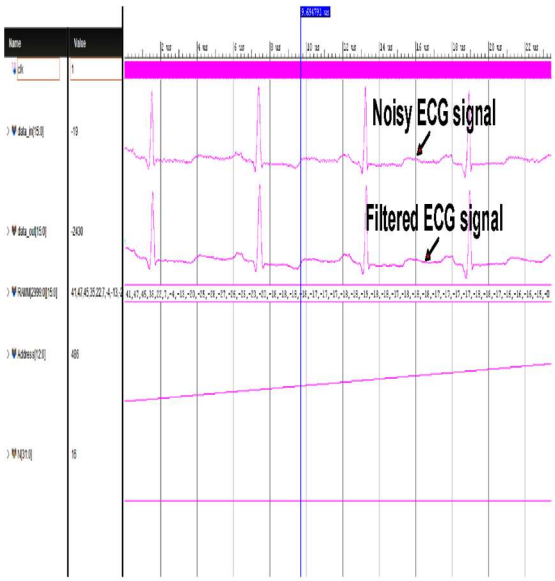


*Fig. 9 Functional Verification and Output waveform of the Proposed ECG denoising FIR filter.*

*Table 1: Fpga Performance Comparison Of The Proposed Fir Architecture With Other Reported Architectures In The Literature Using The Device Family Xc6vcx75t*

| FIR ARCHITECTURES | LUTS | FLIPFLOPS | SLICES | RAM | ROM | FREQUENCY (MHz) |
|---|---|---|---|---|---|---|
| EXISTING -I [30] | 345 | 54 | 125 | 1 | 2 | 107.56 |
| EXISTING -II [31] | 325 | 50 | 117 | 1 | 2 | 127.67 |
| EXISTING -III [32] | 305 | 44 | 98 | 1 | 2 | 115.6 |
| LC-CSLA-FIR [33] | 125 | 34 | 53 | 1 | 2 | 115.39 |
| R8-CLA-FIR [34] | 46 | 21 | 21 | 1 | 1 | 177.98 |
| VD-CLA-FIR [35] | 34 | 24 | 24 | 1 | 1 | 234.73 |
| PROPOSED | 41 | 15 | 46 | 1 | 1 | 100/250 |

*Table 2: Performance Comparison Of The Proposed Fir Filter Using Matlab And Verilog Hdl Simulations*

| PARAMETER | MATLAB OUTPUT WITHOUT NOISE | HDL SIMULATION OUTPUT WITHOUT NOISE | MATLAB OUTPUT WITH NOISE | HDL SIMULATION OUTPUT WITH NOISE |
|---|---|---|---|---|
| BER | 0.21 | 0.25 | 0.25 | 0.29 |
| SNR | 25.61 | 23.27 | 22.89 | 22.36 |
| MSE | 0.33 | 0.39 | 0.38 | 0.41 |

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*TABLE 3: Quantitative Performance Comparison Of The Proposed FIR Filter With Other Reported FIR Filter Architectures [30-35] Reported In The Literature*

| FIR ARCHITECTURES | AREA Sq.µm | POWER mW | DELAY ns | MSE | SNR dB | BER | COMPUTATIONAL COMPLEXITY | ECG DENOISING |
|---|---|---|---|---|---|---|---|---|
| EXISTING -I [30] | 524 | 0.393 | 29.85 | 0.91 | 14.84 | 0.67 | HIGH | POOR |
| EXISTING -II [31] | 492 | 0.369 | 28.12 | 0.85 | 12.83 | 0.68 | HIGH | POOR |
| EXISTING -III [32] | 447 | 0.336 | 25.6 | 0.89 | 15.68 | 0.71 | HIGH | POOR |
| LC-CSLA-FIR [33] | 212 | 0.159 | 13.8 | 0.65 | 18.61 | 0.54 | HIGH | MODERATE |
| R8-CLA-FIR [34] | 88 | 0.096 | 6.83 | 0.42 | 19.25 | 0.43 | MODERATE | GOOD |
| VD-CLA-FIR [35] | 82 | 0.091 | 6.715 | 0.49 | 20.38 | 0.42 | MODERATE | GOOD |
| PROPOSED | 102 | 0.081 | 5.19 | 0.41 | 22.36 | 0.29 | LOW | EXCELLENT |

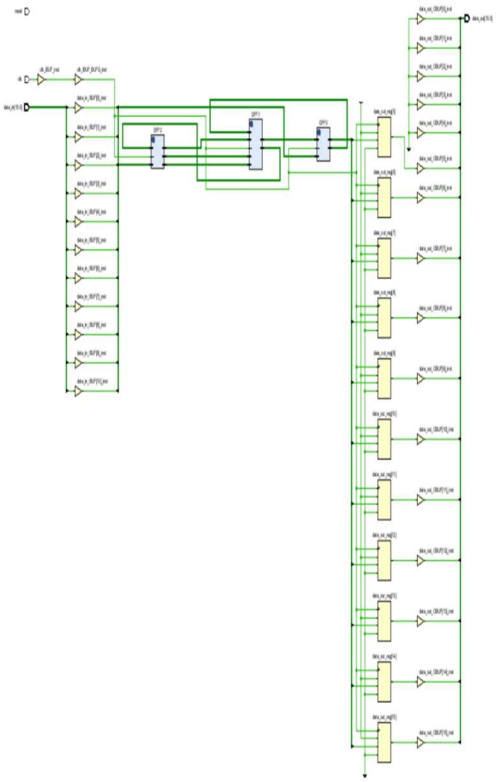

*Fig. 10 RTL synthesized Netlist view of the proposed FIR filter.*

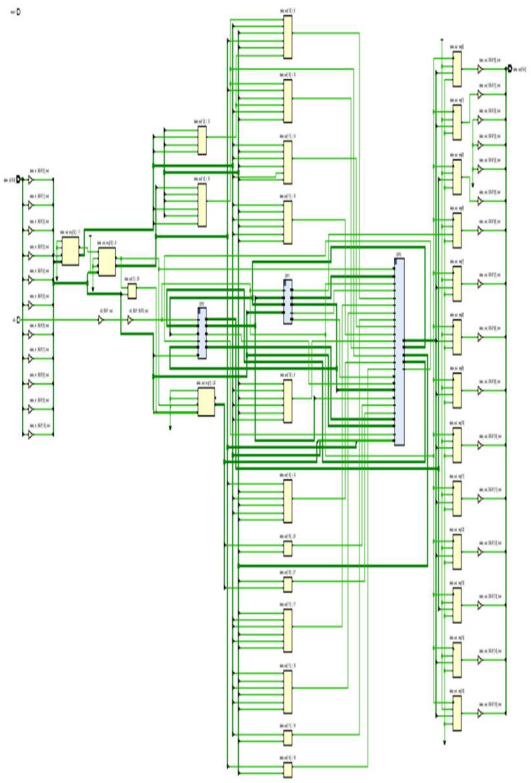

*Fig. 11 RTL synthesized Netlist view of the proposed Vedic Multiplier.*

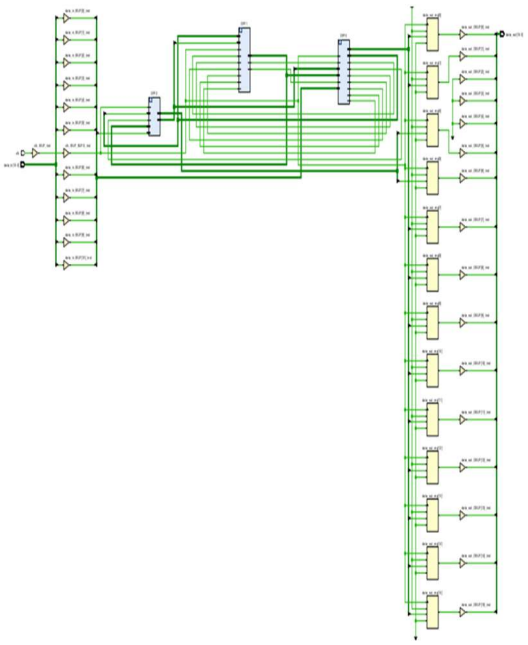

*Fig. 12 RTL synthesized Netlist view of the proposed Carry Save Adder.*

To illustrate the performance of the proposed FIR architecture qualitative comparison is carried out with the other reported architectures in the literature and the results of the comparison are given in Table - 3. In this comparison, for VLSI performances, the area, delay and power metrics are used and then for evaluating the efficiency of the filtering operation, the MATLAB-based analysis I carried out using the metrics MSE, BER and SNR. In the VLSI architecture performance analysis, the area of the filter is primarily calculated using the following equation

$$Area_{(FIR)} = No.of\ (LUTs+FF+Slices) \quad (8)$$

Therefore, based on the above equation, the area of the respective filters is calculated after the FPGA implementation and the respective values are given in table-3 and also plotted as a graph in Fig. 13(a). The respective values of the LUTs, FF and slices are calculated from the implementation summary from the Xilinx tool for each of the reported architectures From the graph, it is inferred that the proposed architecture has a 20% reduced area when compared to the other reported architectures in the literature [30-33]. The prime reason for this reduction for the reduction in area is due to the incorporation of Urdhva Tiryagbhyam Sutra-based Vedic multiplier and CSA adder-based in the FIR filter architecture (i.e., the proposed Vedic multiplier and CSA adder-based FIR implementation involves fewer components when compared to the traditional multiplier and adder structures). Also, from the graph it is inferred that the proposed architecture has a slight increase in are when compared to the architectures [34] and [35], however, the proposed architectures outperform those architectures in terms of delay and power.

Following the area analysis, the delay analysis of the FIR filer is carried out for the reported architectures in the literature in comparison with the proposed FIR filter structure, the respective values of delay for each of the architecture is given in table-3 and drawn as a graph in Fig-13(b). In the delay analysis, the delay of each filter architecture is calculated from the Xilinx EDA tool after implementing the design at a synchronized clock frequency of 100 MHz. From the delay analysis, it is strongly concluded that the proposed FIR filter structure has very less delay when compared to the other reported architectures in the literature. Normally the delay of the filtering mechanism is calculated by adding the respective delay of the multiplier, adder and D flipflops in the filter architectures. In the proposed work, due to the incorporation of Urdhva Tiryagbhyam Sutra Vedic multiplication, the partial products are calculated very fast when compared to normal multiplier structures, also in the CSA based adder structure, the carry is predicted before the sum using a MUX, which in turn once again improves the speed of addition operation, thereby reducing the processing time for the FIR filtering operation in multiplication and addition operations. Furthermore, the Peres reversible logic-based realization also improves the speed of the FIR filter structure at a little extra cost to the area. Thus, in the proposed architecture with the combinations of Vedic multiplier, CSA and Reversible logic gate-based realization the delay is improved by 15% when compared to the other reported architectures in the literature [30-35].

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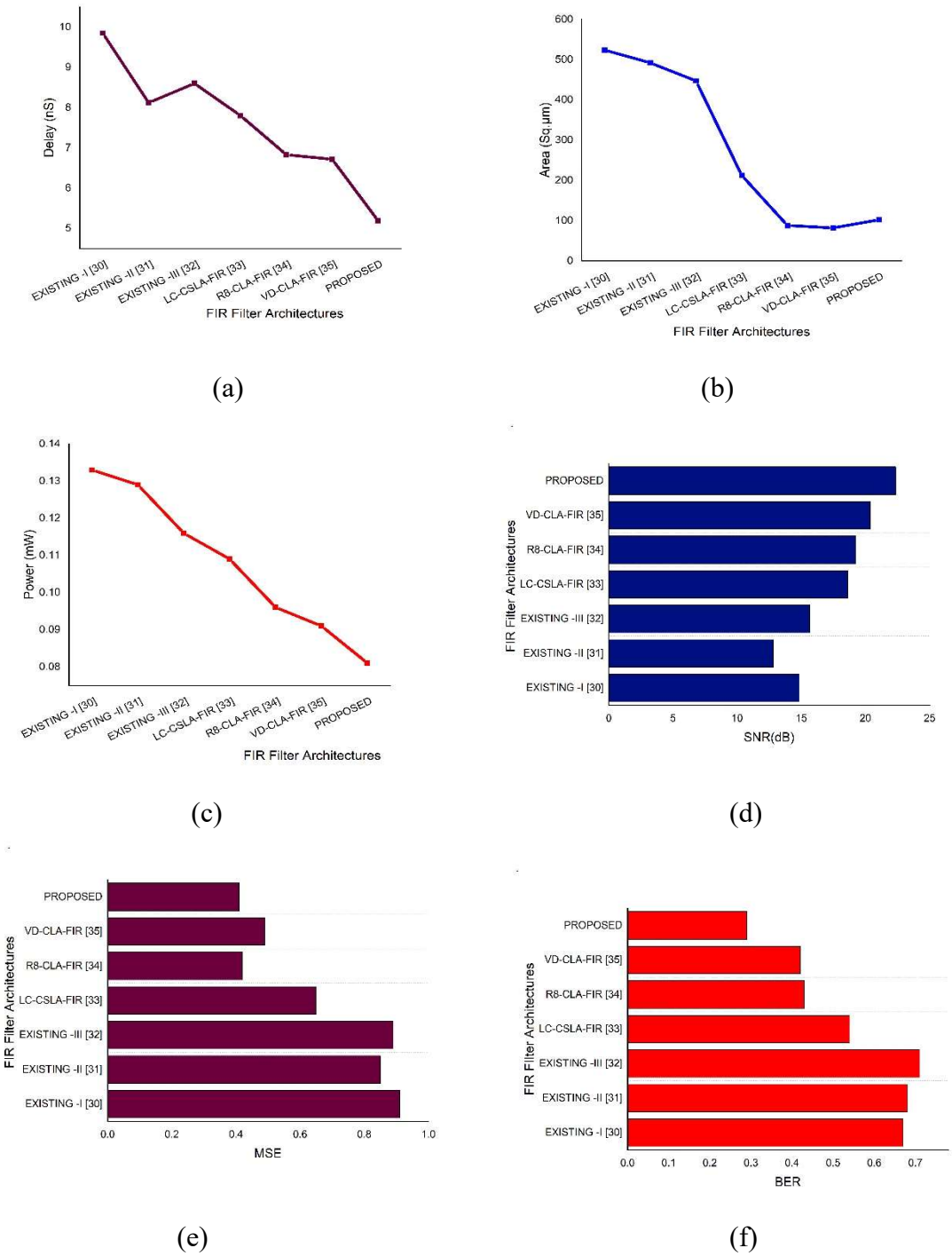


*Fig. 13 Performance Comparison of the Proposed FIR filter Architecture using quality metrics with the other reported architecture in the literature [30-35] a) Delay Comparison, b)Area Comparison c)Power Comparison, d)SNR comparison, e)MSE Comparison and f)BER Comparison.*

Subsequently, after the delay analysis, the power analysis is carried out in the Xilinx EDA tool using the power estimator during the implementation. The respective values of the power for each of the architectures are tabulated in table-3 as well as represented as a graph in Fig-13(c). Also, from the inference of the power analysis values, it is inferred that the proposed FIR filter architecture has a 30% reduction in power when compared to the other reported architectures [30-35] in the literature. The reason for the power reduction is primarily due to the Vedic Multiplier and CSA adder block (i.e., this block is implemented with fewer components compared to traditional structures, which leads to area reduction and herby reduces the total power consumption). Further, in the other reported architectures [30-35], the implementation of filter structures includes DSP logic blocks along with RAM, which leads to increased power consumption than the proposed FIR filter structure. Further, the architectures [30-35] include traditional multiplier and adder block whereas the proposed architecture involves Vedic structure and CSA addition which leads to power reduction together with the reduction in area. Therefore, in this power analysis, it is strongly concluded that the proposed technique has very low power consumption when compared to the power consumption of other reported architectures.

Then the FIR filter efficiency is evaluated for ECG signal denoising application using the quality metrics SNR, MSE and BER for all the reported architectures in comparison with the proposed architectures. The corresponding quantitative comparison of the quality metrics is furnished as a graph in Fig.13(d-e) and the calculated values are presented in table-3. From this quantitative analysis, it is inferred that the proposed FIR filtering architecture has the highest SNR value of 22.36 dB with lower values of MSE (0.41) & BER (0.29) respectively. This is due to the reason that the proposed Vedic multiplier and CSA adder-based FIR filter structures preserve the data precision without any loss (i.e the during the multiplication and addition of ECG signal values with coefficients there is no loss in the signal data due to saturation and rounding off operation) when compared to other reported architectures in the literature [30-35]. Also, the computational complexity of the proposed FIR filter structure is very low and also does the ECG signal denoising effectively, thereby ensuring that the proposed FIR filter structure is well suited for ECG denoising applications.

Additionally, a valid quantitative comparison is made between the MATLAB and HDL implementation with and without noise. The performance metrics MSE, SNR and BER and the respective values of the metrics are given in Table-2. From the tabulated values, it is identified that the proposed techniques perform well even in the presence of noise (i.e., the even in the presence of noise filtered signal has SNR value greater than 20 with a BER and MSE less than 4% only. Thus, with these high values, we can strongly conclude that the proposed FIR filter structure is well suited for ECG signal denoising.

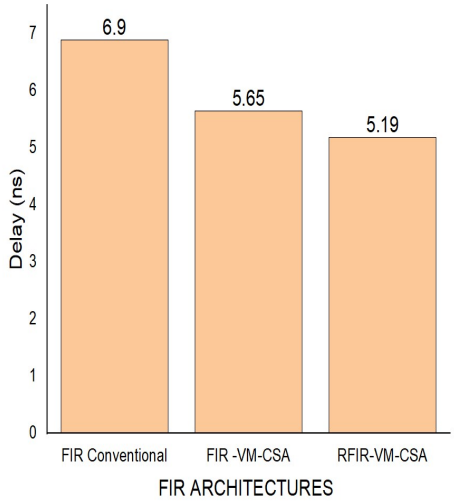


*Fig. 14 Delay Comparison of different FIR Architecture with proposed FIR implementations.*

Furthermore, to illustrate the performance of the proposed FIR filter architecture a valid quantitative comparison is carried out between the FIR conventional architecture (FIR Conventional), FIR filter using Vedic Multiplier-Carry Save Adder without

Reversible gate (FIR-VM-CAS) and Reversible Logic gate-based FIR filter using Vedic Multiplier-Carry Save Adder (RFIR-VM-CSA) in terms of delay and power. The respective values of the comparison are pictorially plotted as the graphs in Fig.14 & 15 respectively.

From the graphs, it is inferred that the proposed RFIR-VM-CSA is having less delay of 5.19ns when compared with the conventional (6.9 ns) and FIR-VM-CSA (5.65 ns) with reversible logic gates. Following the Delay comparison, the power of the aforesaid architectures is evaluated and compared, the findings are also plotted as a graph. From the power comparison graph, it is strongly concluded that the proposed RFIR-VM-CSA consumes a very low power of 0.081mW, whereas the conventional FIR and RFIR-VM-CSA consume 0.112 mW & 0.128 mW respectively. Thus, from the delay analysis and power analysis, we can once again strongly decide that the proposed FIR filter using the reversible logic gate, Vedic multiplier and Carry Save Adder performs comparatively better than the other reported architectures.

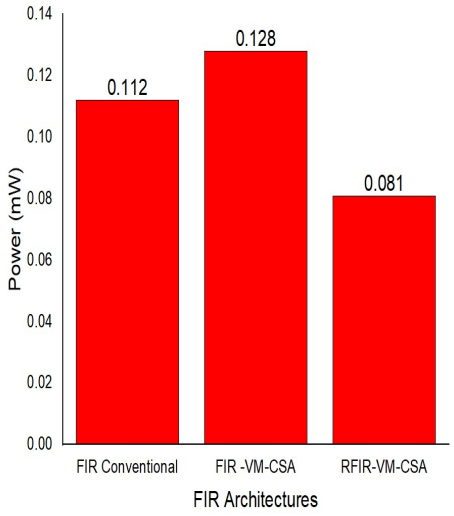


*Fig. 15 Power Comparison of different FIR Architecture with proposed FIR implementations.*

## 6. CONCLUSION

In this research work, the Peres Reversible logic gate-based 8-tap FIR filter using Vedic multiplier and Carry Save Adders is proposed and implemented in the FPGA Virtex6 xc6vcx75t family. The proposed architecture using Urdhva Tiryagbhyam Sutra-based Vedic multiplication process and Peres reversible logic gate-based realization improves the speed of the architecture (i.e., able to achieve minimum delay). Also, in the proposed FIR architecture, the Vedic Multiplier Structure and Carry Save Adder-based implementation consumes comparatively low power and area when compared with the other reported FIR filter structures reported in the literature. Then from the MATLAB analysis, the proposed FIR filter performs well even in the presence of noise with higher values of SNR (22 dB) and lower values of BER (0.29) & MSE (0.49) thereby ensuring the effectiveness of ECG signal denoising operation. Then using the Xilinx EDA tool, the FPGA implemented Peres Reversible Logic Gate-based FIR filter using Vedic multiplier and Carry Save Adder consumes 41 LUTS, 46 Slices, 21 no. of. flip flops with a delay of 5.19 ns at 0.081 mW power. Thus, from the FPGA implementation, it is identified that the proposed FIR filter structure has a 30% reduction in power, 20% reduction in area and more than 15% improvement in delay when compared with the reported Filter structures in the literature.

## 7. LIMITATIONS AND FUTURE SCOPE

In this section, the limitations and future research directions of the presented FIR filter for ECG signal denoising are explained in detail

**Limitations:**

Though the proposed FIR filter filters the noise effectively with the high values of quality metrics, SNR, BER & MSE, the performance of the filter can be further improved by incorporating a window-based methodology design of FIR filter coefficients (i.e., for FIR filter coefficients Rectangular and Kaiser windowing techniques). Also, the order of the filter is very minimal which also can be extended for numerous real-time applications of wireless sensor networks.

**Future Scope:**

Further in the future, the delay of the filter architecture can be improved further by incorporating the pipeline mechanism and parallel prefix adder tree structure in the FIR filter. Additionally, the power consumption of

the FIR filter is further reducible by low power gating and synthesis techniques, also the proposed work is implementable as an FIR ASIC chip which will act like a signal filtering coprocessing chip for real-time applications.

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